11.12.

CG-273-81 VOLUME I

TECHNICAL MANUAL

for

LORAN RECEIVING SET AN/SPN-30

Sections 1 through 4

COLLINS RADIO COMPANY
TEXAS DIVISION
DALLAS, TEXAS

UNITED STATES COAST GUARD

CG-273-81

VOLUME I

TECHNICAL MANUAL

for

LORAN RECEIVING SET AN/SPN-30

Sections 1 through 4

COLLINS RADIO COMPANY
TEXAS DIVISION
DALLAS, TEXAS

UNITED STATES COAST GUARD

Contract: Tcg-40907

Approved by U. S. Coast Guard
November 1961

RECORD OF CORRECTIONS MADE

CHANGE NO.	DATE	FIELD CHANGE NO.	SIGNATURE

UNITED STATES COAST GUARD

ADDRESS REPLY TO:
COMMANDANT
U.S. COAST GUARD
HEADQUARTERS
WASHINGTON 25, D.C.

•EEE
20 November 1961

LETTER OF PROMULGATION

1. CG-273-81 is the Technical Manual for Loran Receiving Set Type AN/SPN-30 and is effective upon receipt. The two copies furnished with the equipments are parts thereof and shall accompany the basic equipment.

2. Extracts from this publication may be made to facilitate the preparation of other technical manuals and handbooks.

3. Copies of this publication may be obtained by requisition to Commanding Officer, U. S. Coast Guard Supply Center, Brooklyn, New York.

4. Corrections to this publication will be made by serially numbered amendments. They shall be entered promptly by responsible personnel.

J. A. ALGER, JR.
Chief, Office of Engineering

LIST OF EFFECTIVE PAGES

PAGE NUMBERS	CHANGE IN EFFECT	PAGE NUMBERS	CHANGE IN EFFECT
Volume I		Volume II	
Title Page	Original	Title Page	Original
ii to xii	Original	ii	Original
1-i	Original	5-i to 5-v	Original
1-0 to 1-8	Original	5-0 to 5-270	Original
2-i	Original	6-i to 6-viii	Original
2-0 to 2-10	Original	6-1 to 6-258	Original
3-i to 3-ii	Original	i-1 to i-18	Original
3-1 to 3-30	Original	Volume III	
4-i to 4-v	Original	Title Page	Original
4-0 to 4-130	Original	ii	Original
		7-i to 7-ii	Original
		7-1 to 7-506	Original

LIST OF SECTIONS

INDEX OF ILLUSTRATIONS

Loran Receiving Set AN/SPN-30
(Illustrations of general application to the system)

Antenna Coupler CU-793/SPN-30

Loran Indicator IP-532/SPN-30

Loran Indicator IP-532/SPN-30 (Cont)

INDEX OF ILLUSTRATIONS (Cont)

INDEX OF ILLUSTRATIONS (Cont)

INDEX OF ILLUSTRATIONS (Cont)

INDEX OF ILLUSTRATIONS (Cont)

INDEX OF ILLUSTRATIONS (Cont)

INDEX OF ILLUSTRATIONS (Cont)

LIST OF TABLES

SECTION 1 — GENERAL INFORMATION

SECTION 3 — OPERATOR'S SECTION

LIST OF TABLES (Cont)

SECTION 3 — OPERATOR'S SECTION (Cont)

SECTION 4 — PRINCIPLES OF OPERATION

SECTION 5 — TROUBLE SHOOTING

SECTION 5 — TROUBLE SHOOTING (Cont)

SECTION 6 — SERVICE AND REPAIR

SECTION 7 — PARTS LIST

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

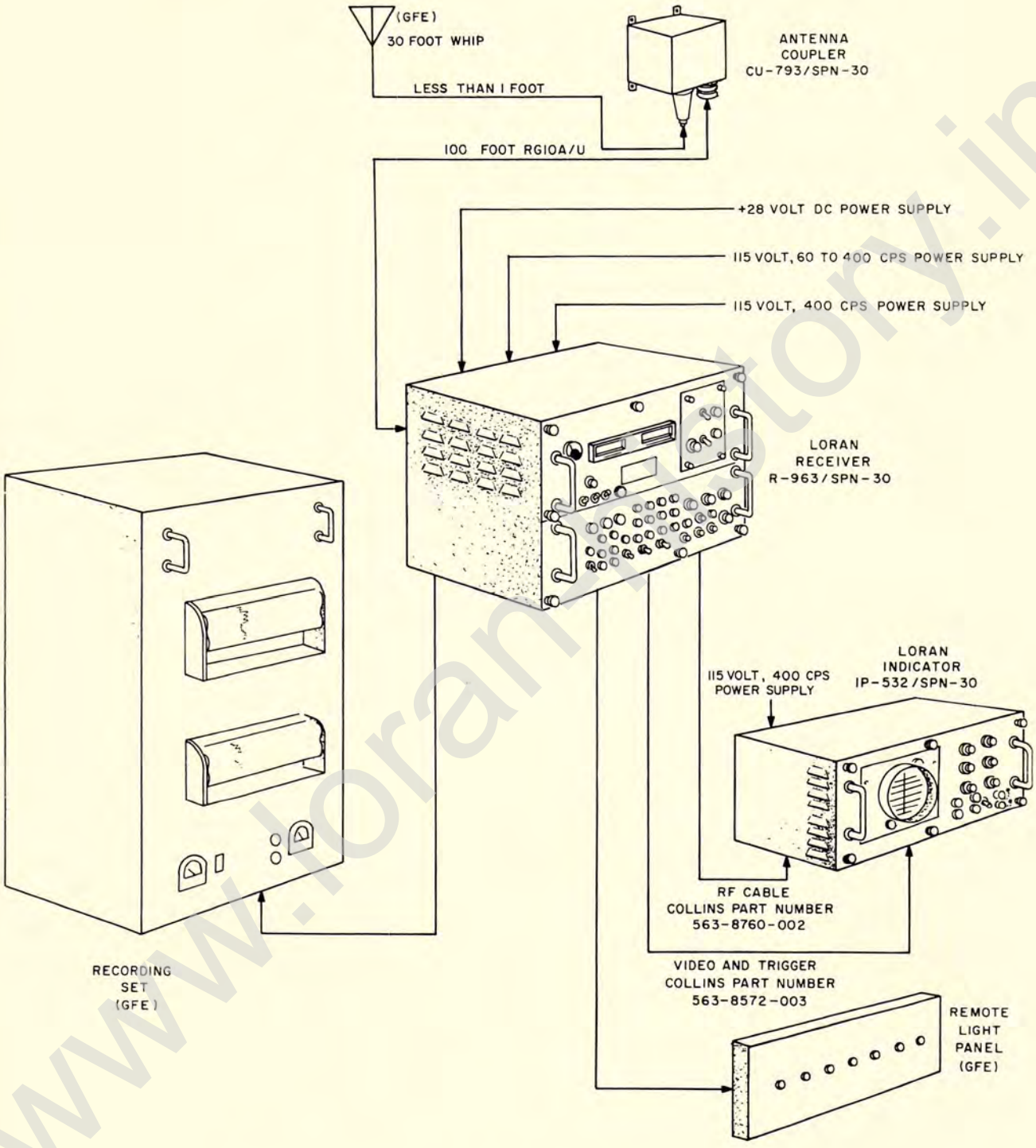


Figure 1-1. Loran Receiving Set AN/SPN-30, Relationship of Units

SECTION 1
GENERAL INFORMATION

1-1. INTRODUCTION.

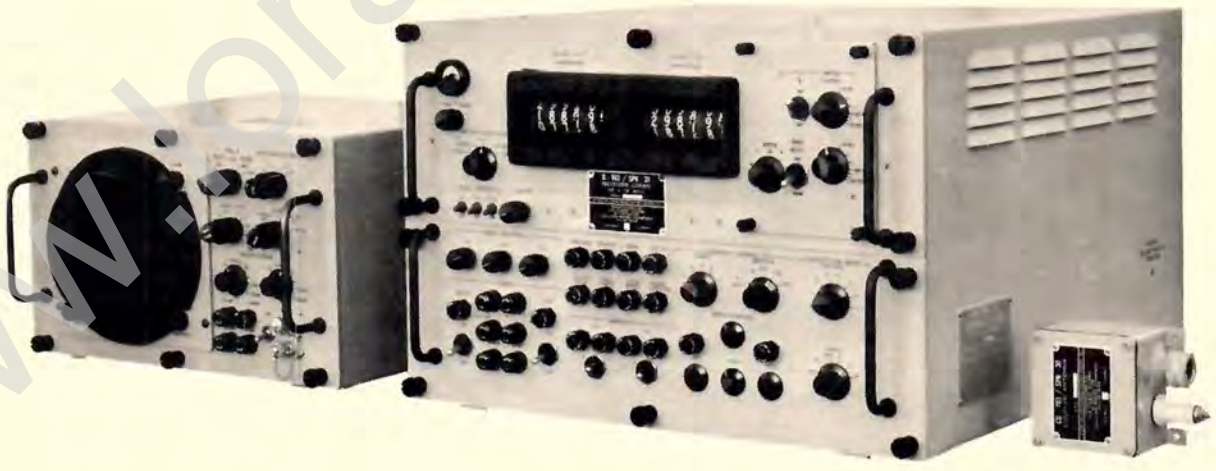
This publication contains operating and servicing instructions for Loran Receiving Set AN/SPN-30. In a condition preparatory to being transported, the AN/SPN-30 is a self-contained Loran-C navigational receiver capable of operating with any group of Loran-C stations for accurately determining precise position location by use of standard Loran-C charts. The relationship of units of the complete receiving set is illustrated in figure 1-1. Loran Receiver R-963/SPN-30 and Loran Indicator IP-532/SPN-30 are shown in figure 1-2.

1-2. LORAN-C SYSTEM.

Loran-C is a precision, long-range, hyperbolic navigational system employing automatic envelope and r-f cycle comparison techniques. It operates in the frequency band of 90 to 110 kc with a carrier frequency of 100 kc. Loran-C utilizes group pulsing; eight pulses per group at each slave station and nine pulses per group at the master station. The pulses of the group are phase coded. That is, the carrier frequency-cycle phase relationship with respect to the envelope is changed from pulse to pulse in a group as prescribed by a stipulated code. The use of synchronous detection and post-detector narrow banding reduces the effect of noise and interference and, in conjunction with the use of phase coding, virtually eliminates the effect of skywave contamination. In addition, phase coding provides signal identification required for automatic search operation. One master and either two or three slaves occupying a single specific repetition rate comprise a Loran-C station group.

a. REPETITION RATES.

(1) BASIC REPETITION RATE. - The basic repetition rate is the approximate rate at which a



LORAN INDICATOR
IP-532 / SPN-30

LORAN RECEIVER
R-963 / SPN-30

ANTENNA COUPLER
CU-793 / SPN-30

Figure 1-2. Loran Receiving Set AN/SPN-30, Overall Oblique View

Loran-C transmitter is single or group pulsed. There are six basic rates as follows:

SS - 10 pulses per second
SL - 12-1/2 pulses per second
SH - 16-2/3 pulses per second
S - 20 pulses per second
L - 25 pulses per second
H - 33-1/3 pulses per second

(2) SPECIFIC REPETITION RATES. - The specific repetition rate is the precise rate at which a Loran-C transmitter is single or group pulsed. Specific rates are identified by a letter or letters followed by a number. The letter or letters signify the basic repetition rate, and the number indicates the number of hundreds of microseconds that the specific period is less than the basic period. Eight specific rates numbered 0 to 7, inclusive, are provided. Repetition periods in microseconds for each of the six basic and eight specific rates are shown in table 1-1.

b. PULSE PHASE CODING. - Phase coding is a method of changing the r-f cycles relative to the envelope of each pulse in the Loran-C pulse group. All cycles within each pulse have the same phase. The phase is varied from pulse to pulse in accordance with the fixed program shown in table 1-2.

1-3. FUNCTIONAL DESCRIPTION.

a. RECEIVER. - Loran Receiver R-963/SPN-30 is a transistorized navigational receiver. The operation is relatively simple, and accurate readings can be obtained by persons having only limited training. The Loran-C receiver (R-963/SPN-30) is capable of simultaneous automatic track of two Loran-C station pairs (master and any two slave stations). Semi-automatic search techniques are incorporated, and the Loran-C receiver will successively locate and track the master and each of two slave signals with the operator furnishing only a limited amount of logic in programming the search operation. The Loran-C receiver is capable of utilizing Loran-C information transmitted in the form of a group of eight phase-coded pulses (nine for the master) from each station. The circuitry required for phase-coding and for performing the multipulsed triggering functions is in a single module. If more sophisticated and complex codes are subsequently employed, modification of the receiver can be accomplished by substitution of the module. The receiver has a visual alarm to indicate when synchronization with the sky-wave occurs. The receiver has provisions for remote indication of the two time differences being tracked as well as all necessary failure indications.

(1) DETECTION. - The r-f detector is a synchronous type. The received Loran-C signals are cross-correlated against the r-f reference signal (timing standard) derived from the 100-kc oscillator. The group-pulsed and phase-coded Loran-C signals are decoded by appropriately decoding the reference signals in accordance with the phase code.

Quadrature (cycle) and in-phase (envelope) synchronous detection is employed in the receiver. The output of the detectors is strobed or sampled at times of signal coincidence. The output of the cycle detector drives the servoloop that maintains phase-lock of the reference signal. The output of the envelope detector is the video envelope. Strobing of the derived video pulse permits servocontrol of the strobe timing circuits to maintain video and strobe lock. Measurement of the time difference between master and slave envelope signals will indicate coarse time difference. Fine time difference is obtained by measurement of the phase difference between the master and slave cycle signals (after they have been phase-locked to the respective Loran-C signals). Time difference is indicated in microseconds.

TABLE 1-1. REPETITION PERIODS

SPECIFIC RATE	BASIC REPETITION RATE					
	SS	SL	SH	S	L	H
0	100,000	80,000	60,000	50,000	40,000	30,000
1	99,900	79,900	59,900	49,900	39,900	29,900
2	99,800	79,800	59,800	49,800	39,800	29,800
3	99,700	79,700	59,700	49,700	39,700	29,700
4	99,600	79,600	59,600	49,600	39,600	29,600
5	99,500	79,500	59,500	49,500	39,500	29,500
6	99,400	79,400	59,400	49,400	39,400	29,400
7	99,300	79,300	59,300	49,300	39,300	29,300

TABLE 1-2. LORAN-C STANDARD PULSE CODING

CODE GROUP	PULSE PHASE IN DEGREES							
	1	2	3	4	5	6	7	8
M-1	0	0	180	180	0	180	0	180
M-2	0	180	180	0	0	0	0	0
S-1	0	0	0	0	0	180	180	0
S-2	0	180	0	180	0	0	180	180

(2) DERIVATION OF TIMING SIGNALS. - Highly stable, binary-type frequency dividers are utilized to derive the various Loran-C repetition rates from the timing standard. Timing waveforms are continuous over the entire pulse repetition intervals. Discontinuity in the timing waveforms necessary to obtain specific pulse repetition intervals occurs only at the end of an interval.

(3) RESOLVERS. - A continuous rotating-type resolver is used as the final stage in the measurement of the time difference between master and slave pulse envelopes. It is possible to measure time delay from a minimum of 9200 microseconds to a maximum of the pulse repetition period minus 9200 microseconds (for 8-pulse, 1000-microsecond spacing operation). It is possible to slew each indicated time delay 20,000 microseconds within 60 seconds. A vernier reading of the envelope time difference is obtained by phase measurements of the difference between the rf of the master and each slave pulse.

(4) AFC CIRCUITRY. - Afc circuitry is provided such that, after the automatic search operation for the master, the output of the afc circuitry is locked with respect to the r-f phase of the master pulse. The afc circuitry has a capability of ±6 parts in 10^7 frequency difference. The output of the afc circuitry is the timing standard used in the remainder of the Loran-C receiver.

(5) SEARCH. - The equipment is capable of automatic signal search and synchronization and has circuitry incorporated to indicate that synchronization is on the groundwave and not on a skywave. The clear guard operates properly in the event of large amplitude differentials between groundwave and skywave signals. The equipment is capable of automatic search and synchronization under extremes of signal amplitude conditions, signal-to-noise ratios, and velocities. Provisions are incorporated for slewing in either direction at five rates of speed to allow minimum search time for the different conditions. It is possible to search using either of the selectivities provided in the receiver. Maximum automatic search time for all signals under worst conditions does not exceed 3 minutes. A station selector switch is used to select the station (M, X, Y, or Z) which is being slewed.

(6) MECHANICAL READOUTS. - The time difference between received pulses from the master and each of the two slaves is indicated by direct reading of mechanical counters. The indicators are easily read at a distance of 2 feet and at any angle up to 30° from normal to the face of the indicator. The envelope (coarse) and cycle (vernier) indicators are the integrated display type to give an overall time-difference reading.

(7) BLINK INDICATOR. - The receiver has an indicator to warn the operator when the time difference readings are unreliable because of transmitter blink.

(8) SIGNAL MONITORING. - The receiver provides signal for three auxiliary units: the indicator, the recording set, and the remote readout panel. The pertinent signals necessary to achieve and maintain lock-on and to perform basic servicing of the equipment are supplied to the indicator. Useful signals may be recorded by a recording set. Signals for this purpose are conveniently available at a connection on the back of the receiver. Another outlet provides signals for an optional remote readout panel.

(9) NOISE GENERATOR. - A white noise generator is provided to facilitate adjustment and testing of the receiver.

b. INDICATOR. - The indicator is an oscilloscope with appropriate slow and fast sweep speeds to permit operational observation of video or r-f Loran-C signals. Two continuously and separately adjustable notch filters are provided to filter the visual r-f presentation without affecting the signal voltages applied to the synchronous detector of the receiver. The notch filters are in addition to and similar to those used in the receiver. In addition, a selective bandpass filter which has a bandwidth considerably smaller than that required for system performance is provided to improve the visual signal-to-noise ratio for signal search.

c. ANTENNA COUPLER. - The antenna coupler is used to couple a 30-foot whip antenna to the receiver input. A coaxial cable up to 100 feet long may be used to connect the antenna coupler to the receiver.

1-4. QUICK REFERENCE DATA.

Modulation:
  Pulse modulation on a 100-kc carrier
Sensitivity:
  10 microvolts
Maximum Signal Input Before Saturation:
  10 volts
Overload Recover Time:
  Less than 50 microseconds following saturation
Bandwidth:
  Normal-
    27 kc at -3 db
    89 kc at -20 db
  Narrow-
    5 kc at -3db
    24 kc at -20 db
Frequency Standard:
  100 kc, tunable ± 1 cps
Frequency Stability:
  1 part in 10^7
Indicator Sweep Rates:
  Fast - 100 to 1000 microseconds
  Medium - 1000 to 10,000 microseconds
  Slow - 1/2 recurrence interval

Power Applied:
R-963/SPN-30-
Operate- 105, 115, or 125 volts rms, 380-420 cps, single phase
Standby- 105, 115, or 125 volts rms, 380-420 cps, single phase
or
105, 115, or 125 volts rms, 50-60 cps, single phase
or
+28 volts dc

IP-532/SPN-30-
105, 115, or 125 volts rms, 380-420 cps, single phase

Power Requirements:
R-963/SPN-30-
Operate- 250 watts maximum at a power factor of not less than 0.95
Standby- 25 watts maximum at unity power factor

IP-532/SPN-30-
45 watts at a power factor of not less than 0.85

Ambient Temperature Range:
R-963/SPN-30- 0° to +50°C (+32° +122°F)
IP-532/SPN-30- 0° to +50°C (+32° +122°F)
CU-793/SPN-30- -28° to +65°C (-18° +149°F)

Ambient Humidity Range:
R-963/SPN-30- 0 to 95%
IP-532/SPN-30 0 to 95%
CU-793/SPN-30- 0 to 100%

Operational Altitude Range:
0 to 10,000 feet above nsl

1-5. EQUIPMENT LISTS.

a. EQUIPMENT SUPPLIED. - Equipment supplied for Loran Receiving Set AN/SPN-30 is listed in table 1-3.

b. EQUIPMENT REQUIRED BUT NOT SUPPLIED. - Equipment required for an installation of Loran Receiving Set AN/SPN-30, but not supplied, is listed in table 1-4.

c. SHIPPING DATA. - Shipping data for the items specified in table 1-3 are provided in table 1-5.

d. ELECTRON TUBE AND SEMICONDUCTOR COMPLEMENT. - Table 1-6 lists the electron tube and semiconductor complement of Loran Receiving Set AN/SPN-30.

TABLE 1-3. LORAN RECEIVING SET AN/SPN-30, EQUIPMENT SUPPLIED

QUANTITY PER EQUIPMENT	NOMENCLATURE		**OVERALL DIMENSIONS			**VOLUME	**WEIGHT
	NAME	DESIGNATION	HEIGHT	WIDTH	DEPTH		
1	Loran Receiver	R-963/SPN-30	13-35/64	20-1/2	26-11/16	4.4	160
1	Loran Indicator	IP-532/SPN-30	9-1/4	15-29/32	19-31/32	1.8	42.5
1	Antenna Coupler	CU-793/SPN-30	2-61/64	3-45/64	5-61/64	.03	1.5
1	Signal Cable Assembly	*563-8572-003					
1	No. 1 Cable Assembly	*563-8571-002					
1	Accessory Kit	*563-9378-00					

* Designates Collins Part Number

** Dimensions are in inches, volume in cubic feet, and weight in pounds.

TABLE 1-4. LORAN RECEIVING SET AN/SPN-30, EQUIPMENT REQUIRED BUT NOT SUPPLIED

QUANTITY PER EQUIPMENT	NOMENCLATURE		REQUIRED USE	REQUIRED CHARACTERISTICS
	NAME	DESIGNATION		
1	Antenna		Receives r-f signals	30-foot whip
1	R.F. Cable Assembly		Connects antenna coupler to receiver	RG10A/U cable

TABLE 1-5. LORAN RECEIVING SET AN/SPN-30, SHIPPING DATA

BOX NO.	NOMENCLATURE		*OVERALL DIMENSIONS			*VOLUME	*WEIGHT
	NAME	DESIGNATION	HEIGHT	WIDTH	DEPTH		
1	Loran Receiver	R-963/SPN-30	19	26	30	8.6	205
2	Loran Indicator	IP-532/SPN-30	15	22	23	4.5	83
3	Antenna Coupler Signal Cable Assembly No. 1 Cable Assembly Accessory Kit Instruction Book	CU-793/SPN-30	12	12	15	1.25	20

* Unless otherwise noted, dimensions are in inches, volume in cubic feet, and weight in pounds; equipment crated and ready for shipment.

TABLE 1-6. LORAN RECEIVING SET AN SPN-30, ELECTRON TUBE AND SEMICONDUCTOR COMPLEMENT (Sheet 1)

UNIT	NUMBER OF UNITS	DIODES																											TRANSISTORS																								ELECTRON TUBES						
		1N91	1N276	1N538	1N540	1N588	1N645	1N647	1N649	1N661A	1N702	1N720	1N721A	1N751A	1N753A	1N756	1N758	1N758A	1N761	1N816	1N1200	1N1202	1N1357A	1N1363A	1N1595A	1N1771	1N1781	1N1781A	1N1791	1N1834A	1N2041	1S6322	SV627	4D26-MX0142	2N138	2N174	2N264	2N277	2N328A	2N333	2N338	2N384	2N404	2N444A	2N447A	2N467	2N526	2N527	2N540	2N585	2N697	2N1038	2N1041	2N1049	2N1247	5670	5687	5749	6005	6977	5BPT1
Receiver R-963/SPN-30	1	6	714	2	5		5	1		147	2		1	1	6	2	2	11		22	15	2	1	1		2	1			2	1	12	1	2	8	3	1	6	6	4	2		295	46	6	6	41	1	3	21	2	14		3	20	5	1	4	2	39	
R-F Selectivity - A201	1																																																						3					
R-F Amplifier - A301	1									1																																												1		4	2		
Detector-Strobe - A401	1									68																																												4				2					
Envelope Deriver - A501	1																																																					1	1				
Guard Strobe Amplifier - A601	1		4																																																			6				2				2	
100-Kc Oscillator - A701	1	2											1																						8		1											1	3								
100-Kc Driver - A801	1																																								2							3			2						
Toggle-A901-A930;A1301-A1310;A1501-A1503	43		430																																									86															
Specific Gate - A931	1		8																																																	3					
Reset Blocking Oscillator - A932; A1312	2		4																																									6															
10-Kc Filter - A933	1																																																									
10-Kc Resolver Driver - A934	1																																									1			2						2								
Squaring Amplifier - A935-A938	4		4																																								12															
Slew Gate - A939	1		6																																								1							2					
Monostable Multivibrator - A940; A1313	2		4																																									4															
Chassis Assembly	1		51				5			6														1									2																											
Comparator - A1201-A1213	13		26																																								52														39	
Coincidence Output - A1214	1		4																																									4															
Encoder Driver - A1215	1																																										8															
Diode Matrix - A1314	1		36																																																							
Code Logic - A1315	1		6																																									5															
Phase Code Driver - A1316	1		6																																									4															
Strobe Timing Gate - A1317	1		9																																																							
Pulse Group Timing Gate - A1318	1		6																																									3															
Skywave Time-Sharing Gate - A1319	1		11																																									3															
Slew Limit - A1320	1																																										6	3														
Polarity Encoder - A1321	1		7																																									4															
Fox-Trpt Generator - A1322	1		14																																									4															
Strobe Blocking Oscillator - A1401-A1404	4		20																													12												8		4													
Strobe Amplifier - A1405-A1407	3									72																																		21				9							9					
Operational Amplifier - A1451-A1453	3																																										9			3	3							3					
AGC Driver - A1504	1																																												1	1	2												
Noise Rectifier - A1505	1																																											3		1												

TABLE 1-6. LORAN RECEIVING SET AN/SPN-30, ELECTRON TUBE AND SEMICONDUCTOR COMPLEMENT (Sheet 2)

UNIT	NUMBER OF UNITS	DIODES																															TRANSISTORS																								ELECTRON TUBES						
		1N91	1N276	1N538	1N540	1N588	1N645	1N647	1N649	1N661A	1N702	1N720	1N721A	1N751A	1N753A	1N756	1N758	1N758A	1N761	1N816	1N1200	1N1202	1N1357A	1N1363A	1N1595A	1N1771	1N1781	1N1781A	1N1791	1N1834A	1N2041	P6032	SY627	4D20-MX0042	2N128	2N174	2N264	2N277	2N328A	2N333	2N338	2N384	2N404	2N444A	2N447A	2N467	2N526	2N527	2N540	2N585	2N697	2N1038	2N1041	2N1049	2N1247	5670	5687	5749	6005	6977	5BPT1
AGC Gate - A1506	1		9																																							3																							
AGC Integrator - A1507-A1509	3		3												6																												3																							
AGC Monitor - A1510	1		4																																							8																							
Error Threshold Detector - A1601-A1610	10		10															10		20																																																
Error Amplifier - A1613-A1619	7		21																																								21				10																			
Receiver Overload - A1620	1		1											1						2																								1	1																							
Blink Light Amplifier - A1621	1																																																																		
Master Cycle Servo - A1801	1																																																																	
Master Envelope Servo - A1901	1																																																																	
Slave Delay Servo - A2001; A2101	2			2												2																																																		
Dither Oscillator - A2002; A2003	2																																																																		
Low Voltage Power Supply - A2201	1										2									12						2													5		4																							
High Voltage Power Supply - A2301	1				5													1											2						1																													
28-Volt Power Supply - A2401	1																			3	2	1													2			1																												
Cycle Time Constant - A2501	1		2																																																																	
Noise Generator - A2601	1																																1																																	
Line Polarity Coder - A2701	1	4						1									2										1																3																							
Chopper Driver - A2702	1		2																											1												1	2																							
Reference Driver - A2703	1		6																																																																	
Indicator IP-532/SFN-30	1		43		8	11			4	1		2			2			2	3					3			3	1	4											2	12	18				1								1	1		2					1
Chassis Assembly	1		6																																							2																							
Selective Amplifier - A3101	1																																									2																							
Vertical Amplifier - A3121	1																																									5																							
Vertical Deflection Amplifier - A3151	1		2																																								2																							1
Notch Filter - A3201; A3202	2																																									2	2																							
Sweep Generator SA1 - A3301	1																																																																	
Sweep Generator SA2 - A3341	1		1																																								4				1																			
Sweep Generator SA3 - A3401	1		19																1																									6																							
Sweep Generator SA4 - A3441	1		13																																								1	2																							
Horizontal Deflection Amplifier - A3471	1																		2																									3																							1
15-Volt Power Supply - A3501	1				4																				3			3																																					
6-Volt, 300-Volt Power Supply - A3601	1				4				4						2			2											4																																				
High Voltage - CRT Assembly - A3801	1		2			11				1		2																	1														1																							1
Antenna Coupler CU-793/SPN-30																																																																			
Totals of Each Type		6	757	2	13	11	5	1	4	148	2	2	1	1	8	2	2	13	3	22	15	2	1	1	3	2	1	3	1	6	1	12	1	2	8	3	1	6	6	4	4	12	313	46	6	6	42	1	3	21	2	15	1	3	20	7	1	4	2	39	1

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

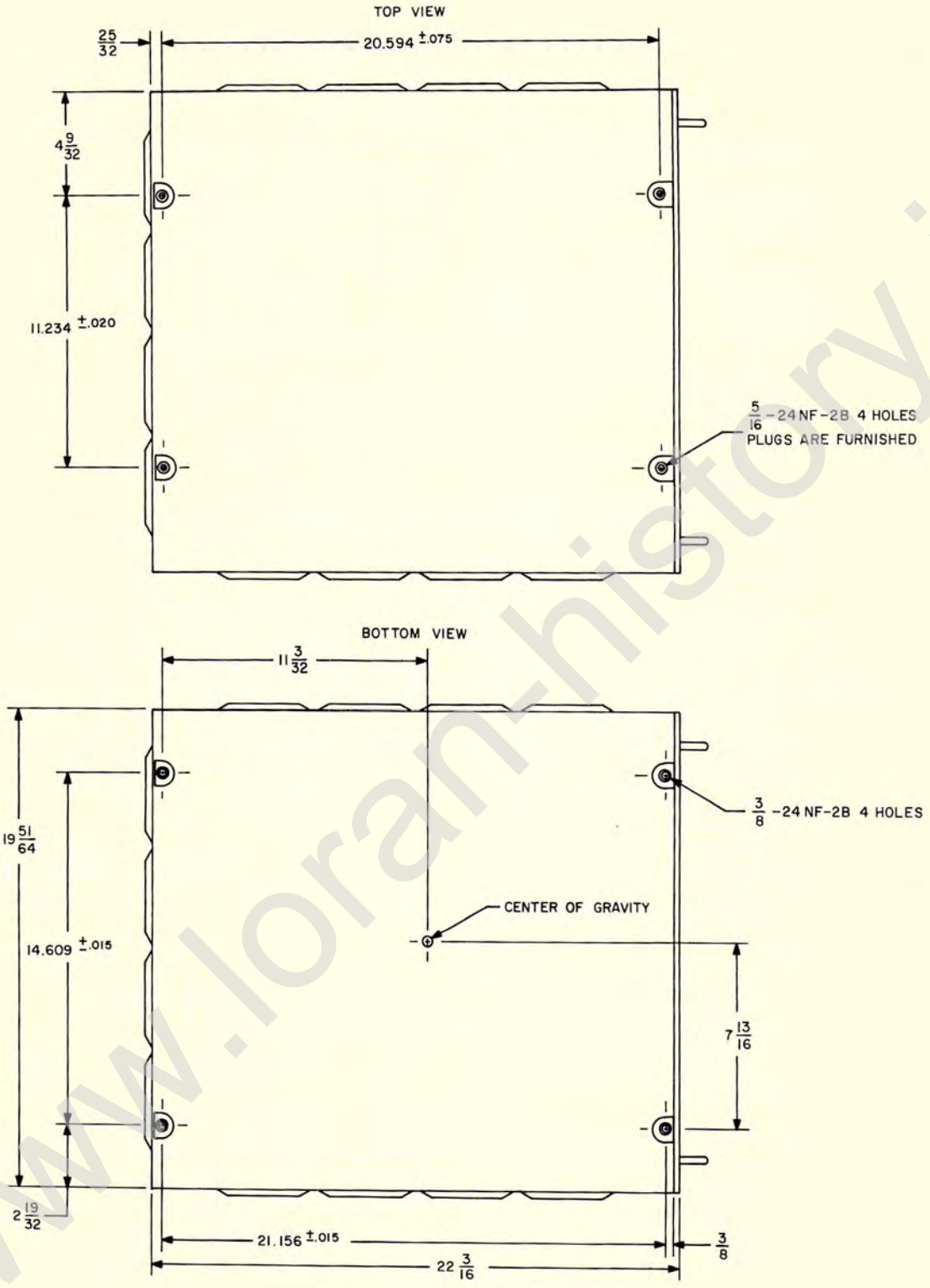


Figure 2-1. Loran Receiver R-963/SPN-30, Top and Bottom Views of Cabinet

SECTION 2
INSTALLATION

2-1. UNPACKING AND HANDLING.

Loran Receiving Set AN/SPN-30 includes the following equipment:

Loran Receiver R-963/SPN-30 (CPN 522 6071 005)
Loran Indicator IP-532/SPN-30 (CPN 522 6106 005)
Antenna Coupler CU-793/SPN-30
(CPN 522 6109 004)
Signal Cable Assembly (CPN 563 8572 003)
No. 1 Cable Assembly (CPN 563 8760 002)
Accessory Kit (CPN 563 9378 00)

The containers should be checked for visible damage before opening them. Boxes containing the R-963/SPN-30 and IP-532/SPN-30 equipments should be in the UP position before unpacking. Care should be taken when unpacking or handling the equipment. The crate or box containing the receiver (R-963/SPN-30) should be dismantled by removing the top and four sides of the crate. This procedure will leave the receiver in an upright position. Eyebolts (threaded 5/16-24NF-2B for 9/32 inch) may be placed in the four threaded holes provided in the topside of the receiver cabinet to facilitate lifting and mounting the equipment at the installation point. See figure 2-1.

Each unit should be carefully inspected for damage incurred in shipment and for loose parts. Knobs, switches, and controls on each unit should be checked for freedom of movement.

All units should be checked for internal damage. Tubes and plug-in components should be properly seated. All units should be checked for broken or loose wires, bits of solder, and loose or missing hardware. The modules should be checked for proper seating in their respective mating jacks. However, the modules should not be removed except to replace units which appear to be damaged. The multiwafer switch labeled SEARCH SELECTOR CONTROL should be examined for bent wafer switching contacts, broken insulation, and loose wires.

2-2. POWER REQUIREMENTS AND DISTRIBUTION.

The power consumption of the receiver (R-963/SPN-30) is 275 watts under operating conditions and 25 watts under standby conditions. The power consumption of the indicator (IP-532/SPN-30) is 45 watts under operating conditions. The antenna coupler (CU-793/SPN-30) has no power requirements.

The primary power requirement for the AN/SPN-30 is 115 volts ac, single phase, 400 cps. When both 115-volt a-c, 400-cps, and 115-volt a-c, 60-cps power are available, and it is not desired to use the 115-volt a-c, 400-cps power except during actual operating time, the 115-volt a-c, 60-cps power may be used for standby 100-kc reference oscillator oven heater operation.

When +28-volt d-c and 115-volt a-c, 400-cps power are available and 115-volt a-c, 60-cps power is not available; and it is not desired to use the 115-volt a-c, 400-cps power except during actual operating time, the +28-volt d-c power may be used for standby 100-kc reference oscillator oven heater operation. See figure 2-2.

The primary power distribution in Loran Receiving Set AN/SPN-30 is shown in figures 5-13 and 5-14.

2-3. INSTALLATION LAYOUT.

Layout and positioning of the equipment will vary with the type of shipboard or airborne installation housing the equipment. See figure 1-1 which illustrates the functional interconnection of the units. The AN/SPN-30 receiver and indicator units are designed for table or bulkhead mounting with not more than 100 feet of coaxial cable connecting the antenna coupler to the receiver.

The receiver unit should be located near a primary power outlet. If the receiver is located against a bulkhead, free circulation of the exhaust air from the blower at the rear of the equipment should be assured.

The receiver is serviceable in its mounted position. However, since a slide-track arrangement permits forward withdrawal of the panel chassis assembly and a chassis tilting arrangement is provided, sufficient space should be allowed in front of the mounted receiver to utilize the slide-track and the tilting provisions. See figure 2-3 for exact dimensions of space needed.

The indicator equipment should be mounted near the receiver unit for efficient use of the indicating devices. If the indicator unit is located against a bulkhead, free access of air should be provided around the mounted equipment to assure proper ventilation.

If the receiver and indicator units are table-mounted special ventilation precautions will probably not be required.

The antenna coupler should be installed within 1 foot of the base of the antenna. The coupler is a watertight, all-weather device with input and output connections on the outside of the case.

2-4. INSTALLATION REQUIREMENTS.

a. LORAN RECEIVER R-963/SPN-30. - Overall unit and mounting dimensions are shown in figures 2-1 and 2-3. Four threaded holes (5/16 inch-24NF-2B) are provided on the topside of the equipment cabinet for insertion of threaded eyebolts or mounting bolts. On the underside of the cabinet, four threaded holes (3/8-inch-24NF-2B) are provided for attachment of the equipment to a table or mounting frame in a bulkhead.

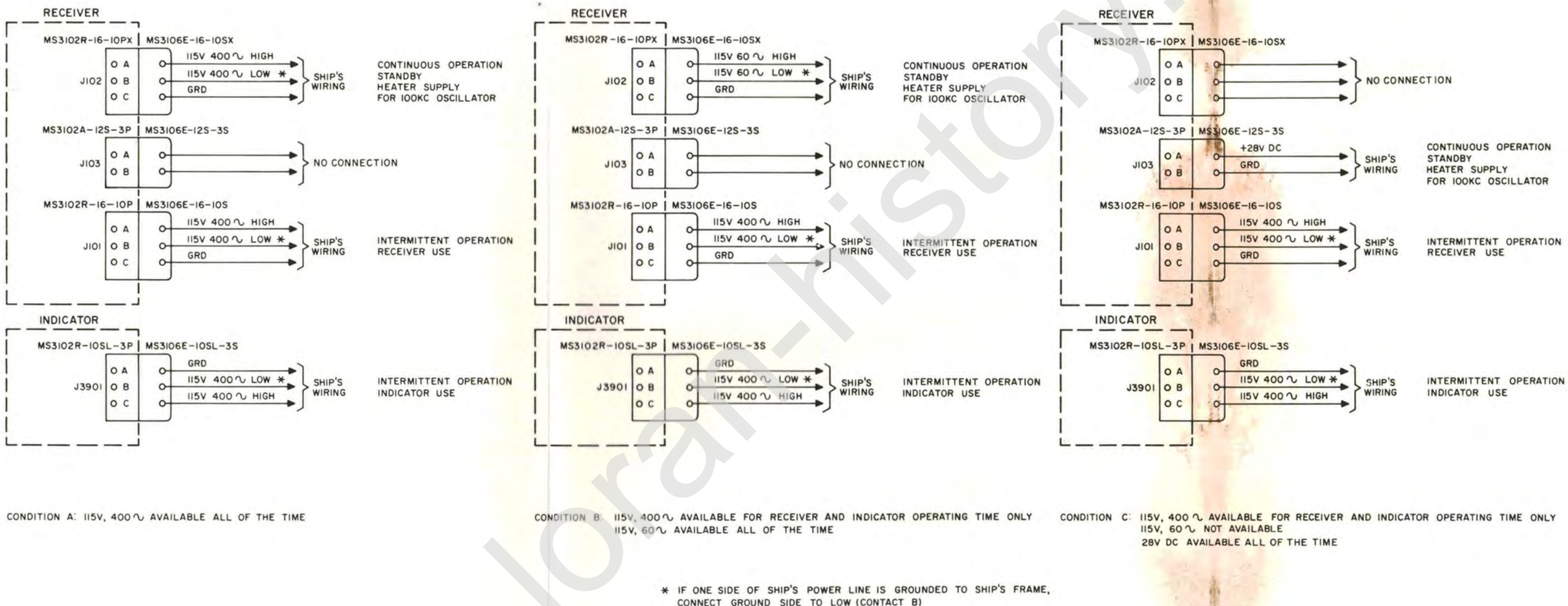


Figure 2-2. Loran Receiving Set AN/SPN-30, Alternate Primary Power Connections

The equipment should be located with free space in front of the unit for servicing and personnel clearance. The chassis may be withdrawn from the cabinet on a slide track and tilted in several planes parallel with the base of servicing and inspection. Therefore, there is an unobstructed space requirement directly in front of the equipment of approximately 33 inches from the front edge of the unit, of 6 inches up from the top edge, and of 14-1/2 inches down from the base edge (see figure 2-3). An additional working area should be provided at the top front, and sides of the withdrawn chassis for personnel clearance.

Provisions for space between the sides and rear of the unit and an adjoining structural member of equipment must also be considered. At least 5 inches of space should be allowed for connector clearance at the rear of the unit. The air from the blower is directed at the equipment inside the cabinet for maximum cooling effect and for removal of dust. The exhaust air escapes through the louvers on the back and sides of the cabinet. At least 1 inch of air space on each side of the unit should be allowed for this air circulation. Table-mounted units do not require special ventilation precautions but do have tilting clearance requirements when the chassis is withdrawn on the slide track. See figure 2-3 for tilting clearance dimensions. In effect, this requirement means that the front panel must line up with the forward edge of the table or shelf on which the unit is mounted.

b. LORAN INDICATOR IP-532/SPN-30. - Overall unit and mounting dimensions are shown in figures 2-4 and 2-5. Four threaded holes are provided on the underside of the cabinet for mounting purposes (see figure 2-5).

The equipment should be located with free space in front of the unit for servicing and personnel clearance. The chassis of the indicator may be withdrawn from the cabinet on a slide track and tilted in several planes parallel with the base for servicing and inspection. Therefore, at least 17 inches of free space are required in front of the indicator equipment, 6 inches are required up from the top edge of the unit, and 3 inches are required down from the base edge (see figure 2-4). An additional working area should be provided at the top, front, and sides of the withdrawn chassis for personnel clearance.

Space allowances should be provided between the sides and rear of the unit and adjacent equipment or structures. At least 5 inches of space should be allowed for connector clearance at the rear of the unit. For a bulkhead installation, air space of 2 inches around the sides of the unit should be provided for free circulation of air. A provision of 1 inch of free space between the top of the cabinet and adjacent structures will permit heat radiation from the metal cabinet to the circulating air. If the indicator unit is installed in a closed air space, air outlets should be provided so that circulation of air may occur.

Table-mounted units do not require special ventilation precautions but do have tilting clearance requirements when the chassis is withdrawn on the slide track. See figure 2-4 for tilting clearance dimensions. In effect, this requirement means that the front panel must line up with the forward edge of the table or shelf on which the unit is mounted.

c. ANTENNA COUPLER CU-793/SPN-30. - Overall unit and mounting dimensions are given in figure 2-6. The antenna coupler is used to couple the antenna to the receiver input and should be mounted within 1 foot of the base of the antenna. The lead-in wire from the antenna to the antenna standoff connector on the coupler should not be more than 1 foot in length and should be mounted away from ground surfaces to minimize shunt capacity. The CU-793/SPN-30 has a watertight case with a sealed lid which may be removed for servicing. Consequently, sufficient free space in front of the sealed lid should be allowed as a work area for maintenance personnel.

A coaxial cable (RG10A/U) up to 100 feet in length may be used to connect the antenna coupler to the receiver (R-963/SPN-30). At the antenna coupler end of the connecting cable, a stuffing tube is used to connect the RG10A/U coaxial cable. See figure 2-7. At the receiver end of the connecting cable, strip the cable armor back approximately 6 inches from connector US-21D/U. Care should be taken not to ground this connector at the receiver.

d. INTERCONNECTIONS OF UNITS. - Interconnections between units contained in Loran Receiving Set AN/SPN-30 are made by means of cabling. These cables are not supplied by the contractor, but are fabricated by the installing activity. All cable connectors to the receiving set units, however, are supplied by the contractor. Cabling interconnections between units of Loran Receiving Set AN/SPN-30 are shown in figure 2-8.

NOTE

Before connecting equipment to primary power source or sources, refer to paragraph 2-2, figure 2-2, and figure 5-13.

The antenna is a separate item not included with Loran Receiving Set AN/SPN-30. The type of antenna used is not critical, but must be supplied by the installing activity. A 30-foot whip antenna is recommended. The antenna is connected to Antenna Coupler CU-793/SPN-30 as described in paragraph 2-4*c*.

e. AIRBORNE INSTALLATION REQUIREMENTS. - In addition to the previously mentioned requirements and typical aircraft installation precautions, two internal changes in Loran Receiver R-963/SPN-30 must be made if the receiver is to be installed in an aircraft. These changes allow the receiver to operate more rapidly in the aircraft while maintaining the same range of servo motor speed used in a shipboard installation. Refer to paragraphs 6-5*c* (31) and 6-6*b* for the procedures to be used in converting from shipboard to airborne configurations. The gain of the cycle portion of the slave delay servo modules must be adjusted for the maximum tracking speed of 60 microseconds per minute for airborne use. This adjustment procedure is presented in paragraph 6-5*c* (43).

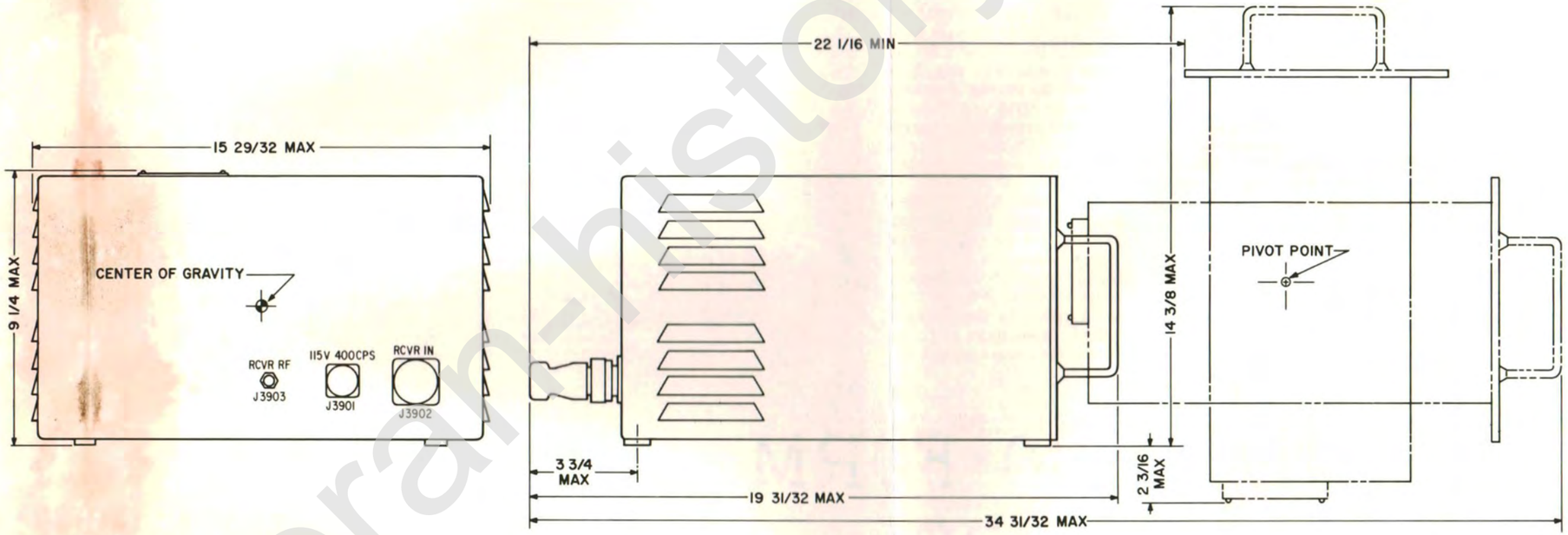


Figure 2-4. Loran Indicator IP-532/SPN-30, Outline Drawing

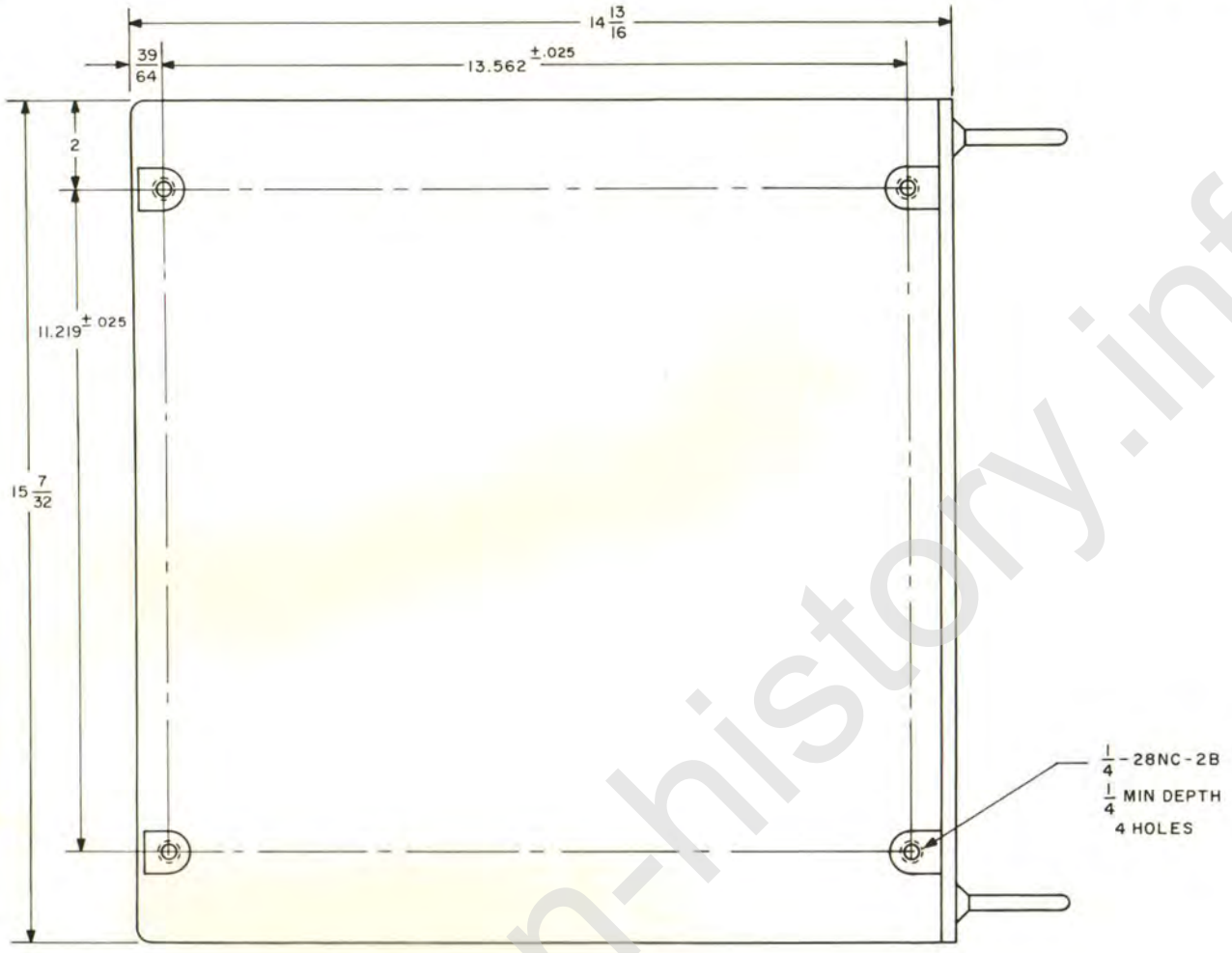


Figure 2-5. Loran Indicator IP-532/SPN-30, Installation Diagram, Bottom View of Cabinet

f. SINGLE PULSE OPERATION. - The following modifications must be made to the receiver to modify it for single-pulse operation.

Step 1. In the noise rectifier module, remove the wire from position 1 shown on the schematic diagram and put it at position 2. This establishes R13 as the output control.

Step 2. Move wire from XA1318-14 and connect it to XA1308-11. This effectively grounds the anode of diode CR1064 (located at XA1317-14) through XA1318-11 and XA1308-11.

Step 3. After the receiver has locked onto a Loran signal, adjust R13 in the noise rectifier module (A1505) until the output of the r-f amplifier (A301) at TP301 measures 0.25 volts rms on a true rms voltmeter.

2-5. INSPECTION AND ADJUSTMENTS.

a. POST INSTALLATION INSPECTION. - Before applying primary power to the equipment, the following inspections should be made:

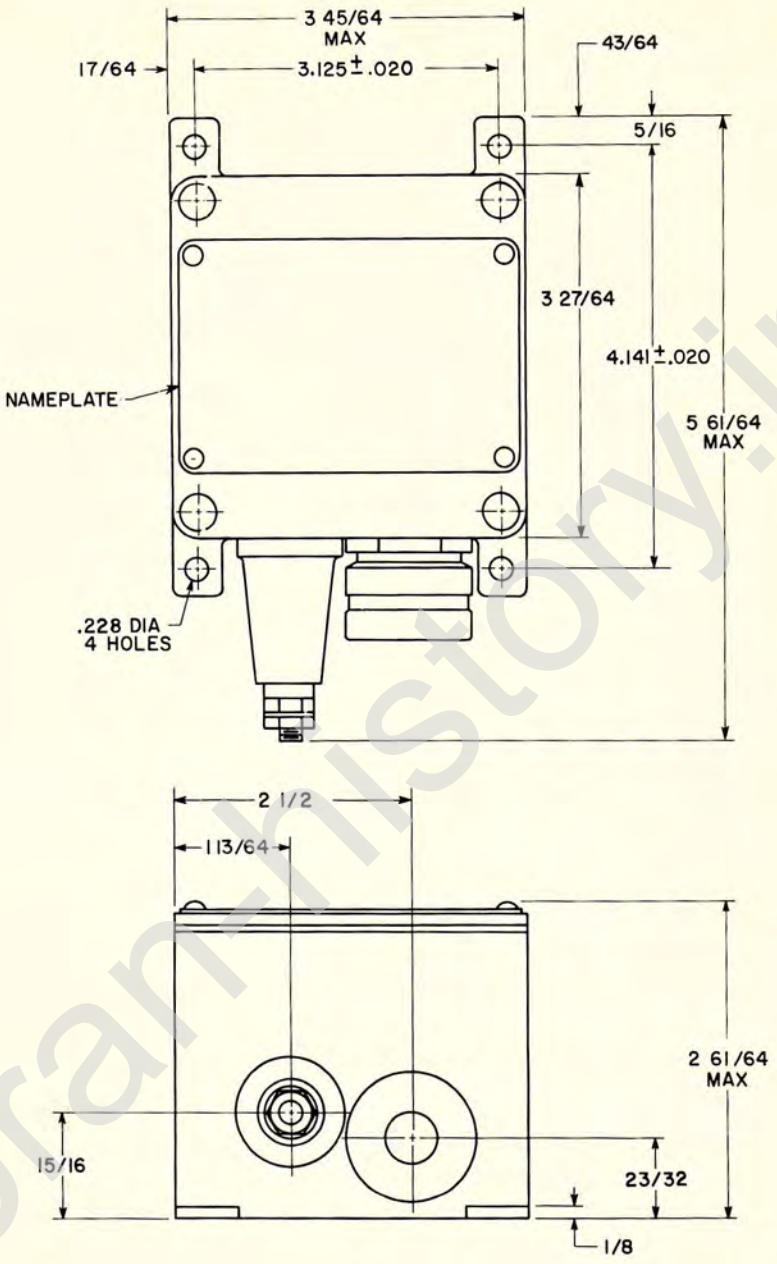
Step 1. Check each cabinet of the equipment for a firm mounting attachment before attempting to slide the chassis from the cabinet on the slide tracks.

Step 2. Ensure that all interconnecting cables are connected in accordance with figure 2-8 and that all cabinet cable plug connectors are properly mated and have tight connections.

Step 3. Review paragraph 2-2 and figure 5-13 and check primary power connections to the receiver and indicator units. Measure the primary power line voltage at the cable connector to be certain that the line voltage is in the range of 105 to 125 volts.

b. POST INSTALLATION ADJUSTMENTS.

(1) ANTENNA COUPLER CU-793/SPN-30. - Check that Antenna Coupler CU-793/SPN-30 has been mounted within 1 foot of the antenna base mount. Connect the antenna to the coupler antenna post with a heavy gauge (No. 14 or 16) self-supporting wire. Ensure that the wire is well clear of grounding surfaces. The housing of the antenna coupler should be grounded to the ship's frame either through the mounting bolts or by means of a heavy gauge (No. 14 or 16) wire connection. Remove the sealed lid from the antenna coupler. Check the



6. AMBIENT TEMPERATURE RANGE: -28°C (-180°F) TO +65°C (+149°F)
5. NO POWER REQUIRED
4. CRATED VOLUME: 1.25 CU FT
3. CRATED DIMENSIONS:
   12 INCHES HIGH
   12 INCHES WIDE
   15 INCHES DEEP
2. 20 POUNDS CRATED WITH SIGNAL CABLE ASSEMBLY, NO. 1 CABLE ASSEMBLY, ACCESSORY KIT, AND INSTRUCTION BOOK
1. 1.5 POUNDS UNCRATED

Figure 2-6. Antenna Coupler CU-793/SPN-30, Outline Drawing

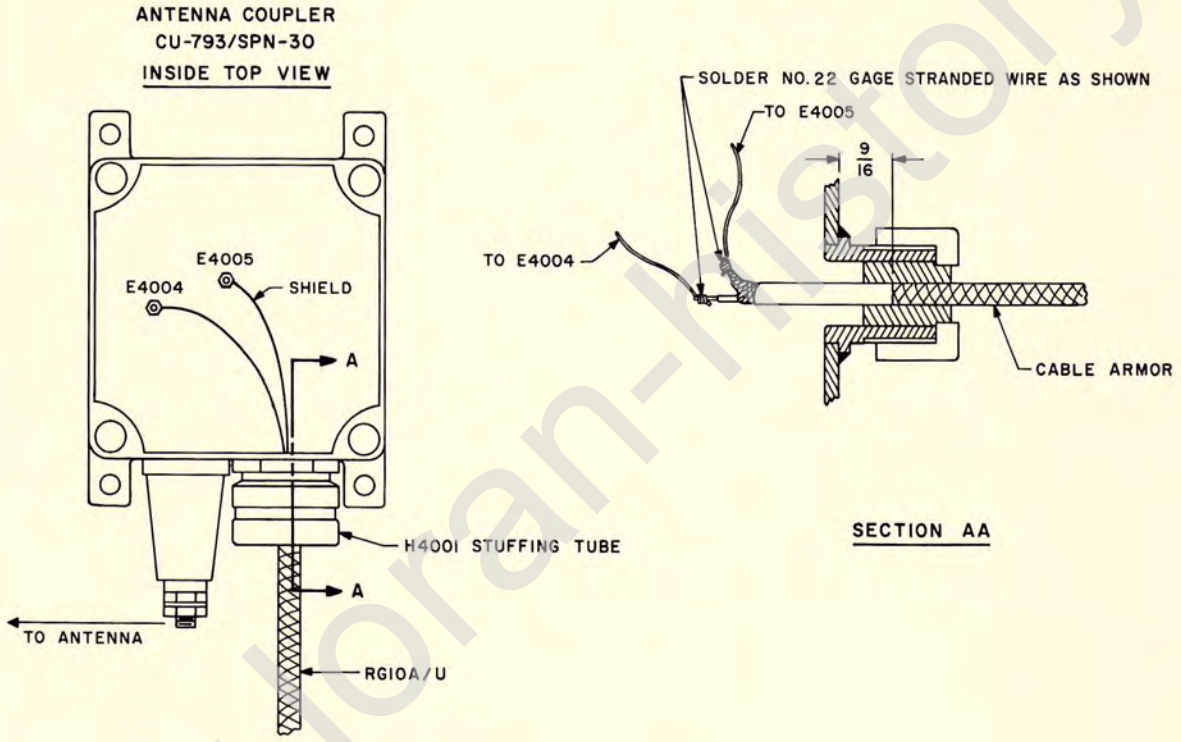


Figure 2-7. Antenna Coupler CU-793/SPN-30, Stuffing Tube, Receiver, Cable Connection

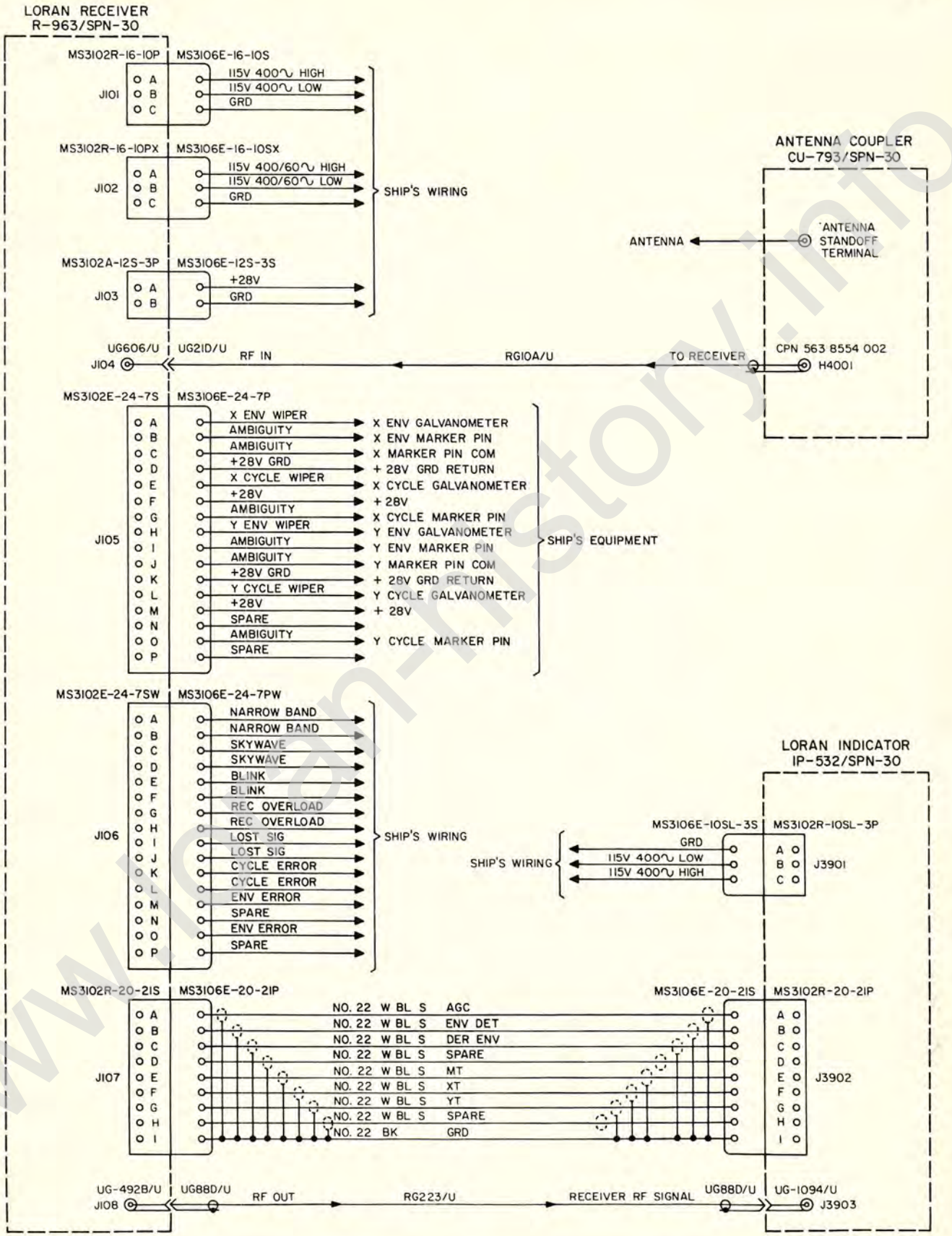


Figure 2-8. Loran Receiving Set AN/SPN-30, Interconnecting Diagram

printed circuit board ground connection to the antenna coupler housing for a firm electrical ground.

NOTE

The antenna coupler housing and the ship's metal frame to which it is connected (either by mounting bolts or by wire connection) form a part of the antenna system for Loran Receiving Set AN/SPN-30. Consequently, clean and firm connections must be assured for proper operation of the receiving set.

Inspect the lead-in cable (RG10/U) from the antenna coupler to the receiver at the antenna coupler end for proper connection. See figure 2-7. Replace the lid on the antenna coupler and check the installation of the lead-in cable to the receiver installation point. Since coaxial cable is easily damaged by undue strain and is subject to pressure flow of the inner dielectric, inspect all bends and clamp attachments. At the receiver end of the connecting cable, check that the cable armor has been cut back approximately 6 inches from receiver connector UG-21D/U. Ensure that connector UG-21D/U is not grounded to the receiver chassis or to adjacent structures.

(2) LORAN RECEIVER R-963/SPN-30. - The following procedures should be followed to make Loran Receiver R-963/SPN-30 operational.

Step 1. Apply primary power to the receiver by moving HEATER power switch to ON and receiver POWER switch to ON (left lower front panel). The green lamps labeled HEATER and RCVR should light.

Step 2. Measure the line voltage at the front panel in the following manner. Locate the two receiver power fuseholders (lower left front panel). Find the recessed test points in the middle of the fuseholder caps. Apply the test leads of an a-c voltmeter, with an accuracy of at least 5 percent, to these points and read the voltage. Turn POWER switches to their OFF positions.

Step 3. Remove the chassis from the cabinet by loosening the knurled knob panel connectors (10 knobs) on the perimeter of the front panel and sliding the chassis forward on the slide track.

Step 4. Unlock the upper chassis and tilt it to expose the power line voltage adjustment taps and the associated plug. Remove the two screws which lock the plug to the chassis.

Step 5. If the voltmeter reading was 105 ±5 volts, attach the line power plug to jack J1006; if the voltmeter reading was 115 ±5 volts, attach the line plug to J1007; if the voltage reading was 125 ±5 volts, connect the line plug to jack J1008.

Step 6. Fasten the line plug to the chassis securely, lock the two chassis assemblies together, and slide them back into the cabinet.

(3) LORAN INDICATOR IP-532/SPN-30. - The following procedures should be followed to make Loran Indicator IP-532/SPN-30 operational.

Step 1. After POWER toggle switches on the receiver are turned to the ON positions, apply primary power to the indicator by moving the POWER switch to the ON position (lower right front panel). The green light labeled POWER should light.

Step 2. Measure the line voltage at the front panel in the following manner. Locate the two indicator power fuseholders (to the right of the INTENSITY control). Find the recessed test points in the middle of the fuseholder caps. Apply the test leads of an a-c voltmeter, with an accuracy of at least 5 percent, to these points and read the voltage. Turn the POWER toggle switch to the OFF position.

Step 3. Remove the chassis from the cabinet by loosening the six knurled knob panel connectors on the perimeter of the front panel and sliding the chassis forward on the slide track. Tilt the chassis forward.

Step 4. Locate the power line voltage adjustment taps at terminal board TB3003.

Step 5. If the voltmeter reading was 105 ±5 volts, attach wire WS-48A (see figure 5-13) to pin 2 of terminal board TB3003; if the voltmeter reading was 115 ±5 volts, attach wire WS-48A to pin 3 of terminal board TB3003; if the voltmeter reading was 125 ±5 volts, connect wire WS-48A to pin 4 of terminal board TB3003.

Step 6. Replace the chassis in the cabinet and tighten the panel connector knobs.

Step 7. Apply power to the receiver and indicator units. Watch the indicator scope face for the appearance of two horizontal sweep lines. Adjust, if necessary, the INTENSITY and FOCUS controls for sharp definition of the sweep lines.

Step 8. Turn the SIGNAL switch to the RF position.

Step 9. Turn the M, X(Y), AND Y(Z) GAIN CONTROL on the receiver fully clockwise. Watch for static-type noise deflections on both sweep lines on the scope face of the indicator unit.

Step 10. Turn POWER switches on the receiver and the indicator to their off positions.

Step 11. Check each unit to be certain that the panels can be secured to the cabinets by the knurled-knob front panel locking bolts.

Step 12. For adjustment procedures of the receiver and the indicator, refer to section 6, Service and Repair.

2-6. PREPARATION FOR SHIPMENT.

Loran Receiving Set AN/SPN-30 should be prepared for reshipment according to the latest issue of specification MIL-P-17555D (SHIPS). Particular attention is called to provisions 3.12.1 and 3.12.1.1 of this specification which concerns the R-963/SPN-30 and IP-532/SPN-30 units of Loran Receiving Set AN/SPN-30.

Packaging method IIb (provision 3.1.4.4.4) of specification MIL-P-17555D(SHIPS) is recommended for Loran Receiving Set AN/SPN-30.

Signal Cable Assembly (A5012) and Cable Assembly No. 1 (A5013) should be coiled without sharp bends and packaged in accordance with provisions 3.10 of specification MIL-P-17555D(SHIPS).

The box containing the technical manuals should be marked "TECHNICAL MANUALS INSIDE."

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont)

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION 3
OPERATOR'S SECTION

3-1. FUNCTIONAL OPERATION.

The AN/SPN-30 is a highly accurate, ship- or aircraft-installed, Loran-C navigational system. Position fixes obtained through the use of the Loran-C system are extremely accurate because of several factors inherent in the system. These factors are discussed fully in subsequent sections of the book.

Components of the basic Loran-C system include a transmitting group made up of a master and two or more slave stations and a receiver to digest and correlate information received from the transmitting stations. Since all Loran-C transmitting stations have a common carrier frequency of 100 kc, it becomes necessary to select a desired transmitting group so that the receiver position may be determined. The position of the receiving point is determined by comparison of time delays between the master station signal and its associated slave station signals.

The receiver (R-963/SPN-30) may be broken down to basic groups as outlined in figure 3-1. It consists of an r-f unit, a reference oscillator, timing circuits, data correlation circuits, a master station information block, and two slave readout blocks. The associated indicator unit (IP-532/SPN-30) consists of sweep circuits, video amplifiers, and a cathode ray tube for visual presentation.

The operator determines the ship's position by selecting the transmitting group most suitable for that service area. When the group is selected, the operator knows the signal repetition rate. The operator adjusts the Loran-C receiver to produce internally a repetition rate close to that of the transmitting group being received. The operator then searches with the locally generated signal that has a repetition rate slightly different from that of the master station of the group. Since there is a difference between the repetition rates, it is possible to cause the locally generated signal to become coincident from time to time with the transmitted signal.

When the transmitted and locally generated master signals are exactly coincident, a function of the receiver causes the locally generated master signal to lock-in and remain coincident with the transmitted master signal. The data correlation circuits accomplish and maintain synchronous alignment of the transmitted and locally generated signals.

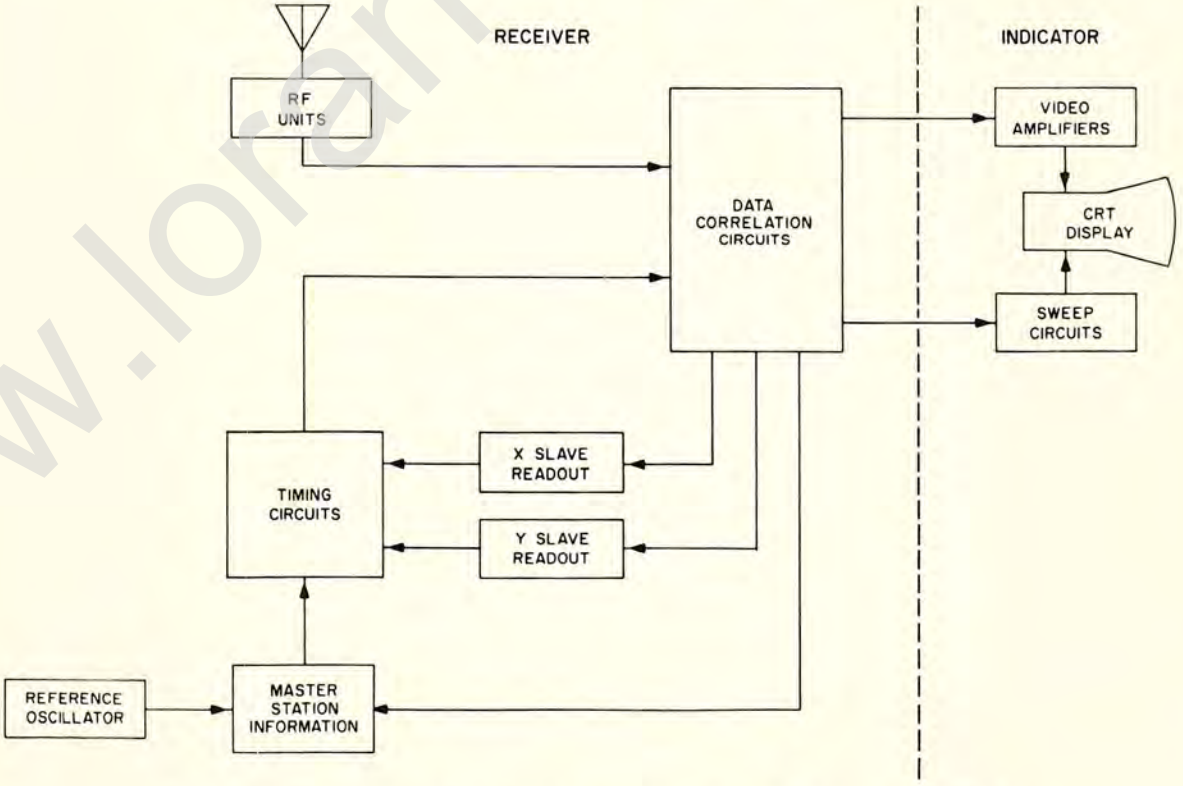


Figure 3-1. Loran Receiver R-963/SPN-30, Simplified Functional Block Diagram

The operator then searches for coincidence between one of the slave transmitting stations and a locally generated slave signal. This searching consists of matching the transmitted time delay with the locally generated time delay between the master signal and the slave signal. When these two slave signals become coincident, a function of the receiver locks in on the transmitted slave signal. The first slave readout gives the operator a dial indication calibrated in microseconds.

To complete a position fix, the operator then searches for coincidence between a second slave transmitting station and a second locally generated slave signal. When coincidence is obtained, the second readout indicates a second time delay in microseconds.

By using these two time delay indications, it is possible to obtain two lines of position and then to correlate this information into coordinates of latitude and longitude through the use of tables and charts.

Facilities are provided to rapidly lock-on the stations while viewing the action on the associated indicator. If the receiver conditions are poor because of generally noisy conditions, large electrical disturbances of frequencies near that of operation, or other interference, special provisions are included in the equipment to assist the operator in minimizing these difficulties.

After lock-on is achieved, the receiver monitors the tracking operation. Indicators will show the operator when anything is interfering with the normal tracking operation. In addition, the indicator may be used to help examine both searching and tracking conditions.

The indicator may, within its capabilities, be used for general testing of the receiver as an all-purpose oscilloscope. It may even be used as a general oscilloscope with other equipment, so long as the range of the indicator is not exceeded.

3-2. PREPARATION FOR USE.

The receiver and indicator are permanently installed and immediately operational. The only preparatory requirement for the equipment if it has been shut-off for some time is the stabilization of the 100-kc reference oscillator frequency. This is accomplished by placing the HEATER ON-OFF switch to ON. The receiver must be allowed to warm up for about 15 minutes before the frequency has completely stabilized. Quicker use of the equipment may be made by following the procedures described in paragraphs 3-3 and 3-4.

CAUTION

Loran Receiver R-963/SPN-30 should be operated either entirely within its cabinet or entirely withdrawn so that the fan can be fully functional. Adequate cooling will be provided only in these two positions.

3-3. OPERATING PROCEDURES.

a. DESCRIPTION OF CONTROLS. - The controls and indicators of Loran Receiver R-963/SPN-30 are illustrated in figure 3-2.

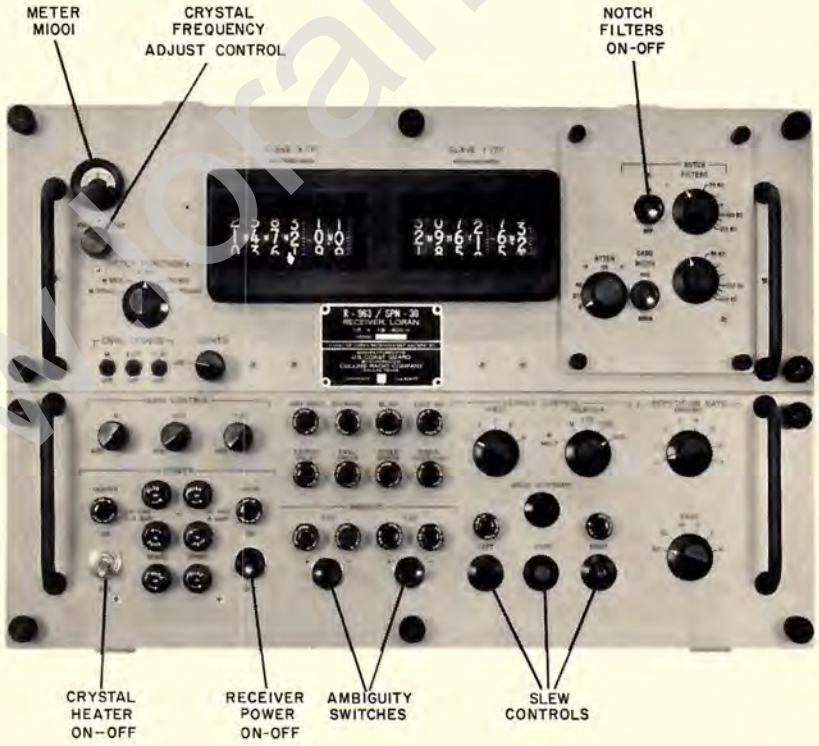


Figure 3-2. Loran Receiver R-963/SPN-30, Controls and Indicators

(1) RECEIVER.

(a) METER AND METER FUNCTION SWITCH. - The METER FUNCTION switch selects the circuit that is monitored by the meter on the front panel of the top drawer of the receiver. The following positions may be selected:

1. MU CYCLE. - In this position, the error in the master cycle loop (output of the magnetic amplifier following the master cycle strobe amplifier) is detected. Before lock-on, there will be no error in the loop and the meter will be in the center position. During lock-on, the meter will reflect the error between the center position and the right side of the meter. After lock-on, with no error, the meter should be centered. If an error exists when the signal is locked on, the frequency of the 100-kc reference oscillator has drifted. The frequency may be corrected by turning the FREQ ADJUST control to center the meter. The cycle loop error will then be zero.

2. MU ENVL. - In this position, the error in the master envelope loop (output of the magnetic amplifier following the master envelope strobe amplifier) is detected. As in the MU CYCLE position, the meter will be centered (no error) when there is no lock-on or when the signal has been completely locked on. However, in this position the meter will remain centered as long as lock-on is maintained, even when the reference frequency has drifted off considerably.

3. M AGC, X(Y) AGC, Y(Z) AGC. - When one of these positions is selected, the meter will monitor the corresponding agc integrator output. Agc action is automatic when the manual GAIN CONTROL knobs (on the bottom drawer) are in their AGC positions. Without lock-on, the gain of the receiver will be maximum and the meter will be all the way to the right. When a signal is locked on, the meter reading will be somewhere between center and full left. Although the meter is not calibrated, a three-quarter left deflection means the received signal is approximately 100 millivolts; and maximum agc voltage is being generated. The meter will become stable and will not fluctuate when the signal is locked on regardless of the strength of the signal and the resulting agc action.

When the manual gain controls are used and a signal is locked on, the meter will monitor the corresponding gain control voltage as selected by the METER FUNCTION switch.

(b) SLAVE DELAY COUNTERS. - Both slave delay counters operate identically. Each indicates in microseconds the time delay between the master signal and the respective slave signal.

1. FIRST FOUR DIGITS. - The first four digits of either dial reading indicate the time delay to the nearest 10 microseconds and are controlled by the envelope loop servos.

2. LAST TWO DIGITS. - The last two digits indicate the reading to the nearest 0.1 microsecond and are controlled by the cycle loop servos. Notice that there is a decimal point on the counter in front of the last digit. If there is an ambiguity indication of + (AMBIGUITY lights on the bottom drawer), the next higher tens digit (fourth drum) should be read. If there is a - ambiguity light, the reading should be the lower reading on the fourth drum. Refer to paragraph 3-3*a* (1) *(i)* 8 for a further explanation of ambiguity.

3. LIGHTS. - The LIGHTS switch on the top drawer is a 6-position detent switch used to change the brightness of the slave delay readouts. The lights become progressively brighter as the switch is turned from detent to detent in a clockwise direction from the OFF position.

(c) R-F SWITCHES.

1. ATTEN CONTROL. - With a normal signal, the ATTEN control should be placed to the 0 DB position. If one of the received signals is in excess of 100,000 microvolts so as to saturate the r-f amplifier, the 20 DB or the 40 DB position must be selected. When this is done, all of the signals received will be attenuated an equal amount. However, it should be noted that this action may attenuate the weaker signals below the usable receiver level.

2. BAND WIDTH CONTROL. - The BAND-WIDTH CONTROL is a 2-position toggle switch. In the NORM position, a 20-kc bandwidth is permitted. The NORM position of the switch is always used when the receiver is tracking (after lock-on) and may or may not be used when it is searching. The NAR position of the switch limits the bandwidth to only approximately 6 kc. The signal-to-noise ratio is improved by reducing the bandwidth, but the input signal also becomes distorted. Switching transients may cause the addition or subtraction of time so that the local signal will have to resettle on the transmitted signal when the control is switched from either position to the other after lock-on.

3. NOTCH FILTER CONTROLS.

a. ON-OFF. - The NOTCH FILTERS ON-OFF control merely places the notch filters in the circuit or omits them.

b. NOTCH FILTERS CONTROLS. - There are two narrow-band notch filters, each with a depth of approximately 30 decibels. The notches may be placed at any position from 70 KC to 130 KC to block out unwanted, interfering signals. Before they are first switched in, they should be tuned to one end of the range and not centered near 10 KC. The notches may be stacked, if desired, to produce one 60-db notch.

(d) ENVL SERVOS. - There are three manual envelope servo switches: M, X(Y), Y(Z). When the receiver is used for tracking (after lock-on has been accomplished), the envelope servos may be turned off without affecting the slave delay readings. The cycle servos will drive the envelope digits as well as the cycle digits to maintain all of the dial indications at their proper values.

(e) GAIN CONTROL. - There are three identical manual gain controls: M, X(Y), Y(Z). Each control determines the amount of agc action for the particular gate to which it corresponds. In the AGC position

of the control for that gate, the receiver will operate on agc. The strength of the gain for the corresponding gate will be determined manually if a control is taken off the AGC position. Full gain is the maximum clockwise position (before the AGC detent) and fully counterclockwise is maximum agc (minimum gain).

(f) POWER CONTROLS.

1. HEATER ON-OFF. – This toggle switch turns on the oven for the crystal in the 100-kc reference oscillator circuit. If the receiver is off, but kept in a standby condition, the oven should remain on. Otherwise, a warmup time of approximately 15 minutes will be required for the crystal frequency to stabilize. The HEATER green light indicates that the oven is on.

2. RCVR ON-OFF. - This toggle switch places the receiver in the operational state. Little warmup time is required if the HEATER ON-OFF control has been on a sufficient time for the crystal frequency to achieve a stable condition. The RCVR green light indicates operating voltages have been applied to the receiver.

(g) REPETITION RATE CONTROLS.

1. BASIC. - The Loran-C repetition rates consist of six basic rates and eight specific rates. The BASIC control selects the proper basic repetition rate for the receiver application.

2. SPECIFIC. - The SPECIFIC control selects the proper specific repetition rate for the receiver application. Together, the two switches determine the repetition rate for the internally generated pulses in the receiver to correspond with the received signal transmitted from the master and slave stations.

(h) SEARCH CONTROLS.

1. SEARCH SELECTOR CONTROL. - The SEARCH SELECTOR CONTROL selects the mode of operation for the receiver.

a. OPR. - The OPR (operate) position is used after lock-on has been accomplished and the receiver is successfully tracking the transmitted signals. The indicator lights monitor all three lock-on actions (master and both slaves) so that if lock-on is lost, or some other malfunction occurs, there will be the proper indication on the front panel. It is important to place the switch in the OPR position after the lock-on has been accomplished and the receiver is tracking.

b. M. - The master signal is always sought first when searching for initial lock-on. In the M position, the receiver will attempt to match the internally generated master signal with the transmitted master signal. The indicator lights also will only monitor the master signal action.

c. X(Y), Y(Z). - These two positions are used when attempting to lock on the slave stations. After the master has been locked on, the X(Y) position should be used next to seek the first slave station following the master station in time. The indicator lights on the front panel will only monitor the selected signal during the time of search. The Y(Z) position should then be selected to search for the remaining slave.

d. M MULT. - The M MULT (master multiple) position of the switch is used to rapidly search for the master station. All of the internally generated signals (the master and both slaves) will simulate the master signal; therefore, the likelihood of being close to the transmitted signal is increased 3-to-1. When the transmitted signal comes into any of the received gates, the master is ready for lock-on.

2. SEARCH SPEED CONTROL. - The SEARCH SPEED CONTROL determines the slew rate of the receiver. The fastest rate is 5. In this position, the internally generated signal varies from the selected repetition rate by approximately 10,000 microseconds per minute. This position is used by the operator to rapidly slew the receiver gates to the approximate position when the operator suspects what this position should be. The 3 and 4 positions are used when the transmitted signal is extremely clean and there is little interference. The 1 and 2 positions are used when noise accompanies the signal. The 1 position is the slowest, with the internally generated signal varying from the selected repetition rate by approximately 1000 microseconds per minute.

3. LEFT, RIGHT. - These controls are used to manually slew the internally generated signals either to the left or to the right. The buttons need only be depressed and then released to initiate slewing action. For the particular mode of operation (as determined by the SEARCH SELECTOR CONTROL), the internal signal will slew over its entire range. The internal signal will automatically reverse, and the opposite slew indicator will light when the extreme range of the gate is reached without encountering a signal. Slew will continue until a signal is locked on or until the slew is manually stopped. The light indicating slew action will go out when the slew is stopped.

If there is an indication of a skywave after lock-on, the proper signal should be selected by the SEARCH SELECTOR CONTROL, the SEARCH SPEED CONTROL set to position 1, and the LEFT slew button depressed to lock on the ground wave.

4. STOP. - The STOP control is used to manually terminate the slewing action when it has not stopped by locking on a signal.

5. GROUP ALTERNATE. - When the Loran-C indicator scope presentations are being used as an aid to achieve lock-on, the operator can observe when the coding is 180° out-of-phase (when the M2 code group is over the M1 code group). Instead of having the slew through half of a complete repetition cycle, the operator can accomplish the same result by depressing the GROUP ALTERNATE button.

(i) INDICATOR LIGHTS.

1. SKYWAVE. - This light may come on while the receiver is being locked on, but it is only meaningful after the receiver has locked on to the transmitted signal. The SKYWAVE light is a time-shared monitor when the SEARCH SELECTOR CONTROL is

placed in the OPR position. If any of the stations are not locked on, the light will blink and the M, X(Y) Y(Z) positions must be selected to find which skywave has been locked on.

2. BLINK. - The BLINK light will indicate when the time sequence of the slave transmitters is not accurate. A BLINK light indication is a warning that the slave readings are no longer dependable.

3. LOST SIG. - The LOST SIG light is an indication that the receiver has not locked on to the transmitted signal. The LOST SIG light will light when the SEARCH SELECTOR CONTROL is in the OPR position and any one of the signals (master or either slave) is lost. The selector switch must be placed to the M, X(Y), or Y(Z) position to determine which signal is not locked on.

4. ENVL ERROR, CYCLE ERROR. - These lights monitor the error signal in the respective servo-loops. These lights are out during search until the internal and external signals begin to coincide. The lights will go out when lock-on has been completely accomplished and there is no error in the respective loops.

5. EXCESS DELAY. - This indicator light will light when the slew action of the receiver moves one gate into the one next to it. When this happens, slew action automatically reverses and one of the gates will disappear until there is no longer an overlap. The light will go out when the signal has been slewed away from contact, and the missing gate reappears.

6. SIGNAL OVERLOAD. - This light indicates that one of the received signals is too strong and is beyond the limits of the agc circuit. The ATTEN control on the top drawer must be set to the proper position to attenuate the received signal to a proper level when this occurs.

7. NARROW BAND. - This light is on when the BAND WIDTH control on the top drawer is placed in the NAR (6 kc) position. After lock-on, the switch must be returned to the NORM position before the SLAVE DELAY reading is accurate.

8. AMBIGUITY. - There are four lights and two switches for use in resolving ambiguous readings between the envelope delay readout and the cycle delay readout inherent in the Loran-C system. Two lights and one switch are used for each SLAVE DELAY readout. Each SLAVE DELAY readout has two groups of digits from which the seven digits of the SLAVE DELAY can be read in microseconds to the nearest hundredth. The first group is read from the first four dials, the fifth digit being read from the vernier scale on the fourth dial. These five digits indicate the time delay to the nearest 10 microseconds and are controlled by the envelope loop servos. The second group is controlled by the cycle loop servos. It has two dials; the first reads out the fifth digit of the delay as determined by the cycle loop servos, the second reads out the tenths place and the vernier on this tenths place dial indicates the hundredths place.

These two groups are independent of each other and since each group reads out the fifth digit of the delay some ambiguity can develop. After complete lockon, the cycle delay readout is the more accurate readout. The envelope delay readout is not as accurate as the cycle delay readout. It is used to resolve ambiguity with the help of the AMBIGUITY lights when the difference in the dial readings is more than 4 microseconds. Following is a discussion of how the ambiguity is resolved.

First, the receiver must be set up on good information from the transmitter. The information is good if the envelope dials and the cycle dials agree within two microseconds. If they do not, unreliable information (weak signals, high interference, etc.) was used to set up the receiver and ambiguous readings between the dials later on can never be resolved until the receiver locks on good information.

If one of the ambiguity lights comes on after lock-on under the condition of good information only, it is turned off. If it lights at some later time, this is an indication of ambiguity. Ambiguity is indicated by the lights if the envelope delay readout and the cycle delay readout become more than approximately 4 microseconds apart.

In all the examples below, the tenths and hundredths places will arbitrarily read 0.

Example 1A - no ambiguity (figure 3-3). The first four digits are 1505 and the vernier on the fourth dial reads 1. This means the envelope delay readout is 15051. But the cycle delay readout is 9.00. Since no ambiguity light is on, the true readout must be 15049.00. The cycle delay readout was below the envelope delay readout less than 4 microseconds.

Example 1B - no ambiguity (figure 3-4). The first four digits are 1505 and the vernier on the fourth dial reads 0. This means the envelope delay readout is 15050. But the cycle delay readout is 2.50. Since no ambiguity light is on, the true readout must be 15052.50. The cycle delay readout was above the envelope delay readout less than 4 microseconds.

Example 2 - ambiguity (figure 3-5). The first four digits are 1505 and the vernier on the fourth dial reads 5. This means the envelope delay readout is 15055. But the cycle delay readout is 0.00, which is 5 above or 5 below the envelope delay readout. If the + AMBIGUITY light is on, the true readout is 15060.00. If the - AMBIGUITY light is on, the true readout is 15050.00.

For ambiguity more than 10 microseconds, special precautions must be taken in interpreting the slave delay readouts and the AMBIGUITY lights. After ambiguity is observed and the direction the cycle reading varies from the envelope reading is determined by the AMBIGUITY lights, the ambiguity condition can become worse. When the ambiguity reaches approximately 10 microseconds the original light will go out and the opposite light will go on.

Example 3A - ambiguity of more than 10 microseconds in the positive direction (figure 3-6). The first four digits are 1505 and the vernier on the fourth dial reads 1. This means the envelope delay readout is 15051. The cycle delay readout is 6.00, and the + AMBIGUITY light is on. This indicates the true readout is 15056.00, or +5 microseconds above the envelope readout. It is assumed that the course of the ship is regular and readings are being taken at regular intervals. At the next reading the operator observes a difference in the true and envelope readouts of +6 microseconds. On the successive regular readings the difference is observed to be increasing to +7, +8, and +9 microseconds. At the next reading, the - AMBIGUITY light is on and the dials exactly agree. An ambiguity light being on should tell the operator

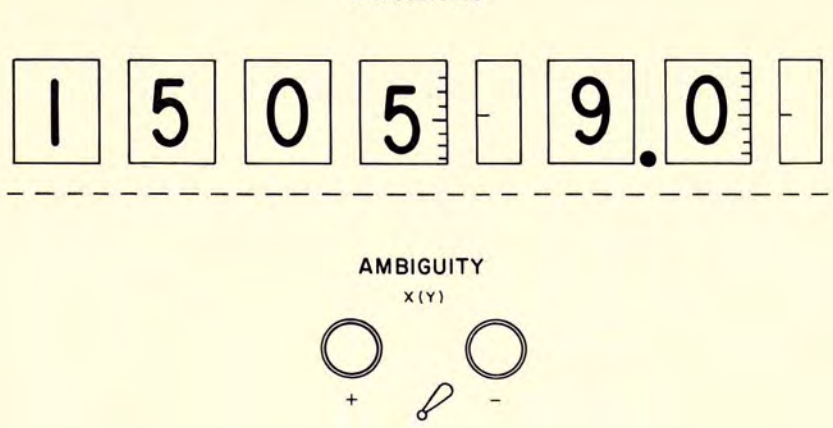


Figure 3-3. Loran Receiver R-963/SPN-30, Ambiguity Indication, Example 1A

Figure 3-4. Loran Receiver R-963/SPN-30, Ambiguity Indication, Example 1B

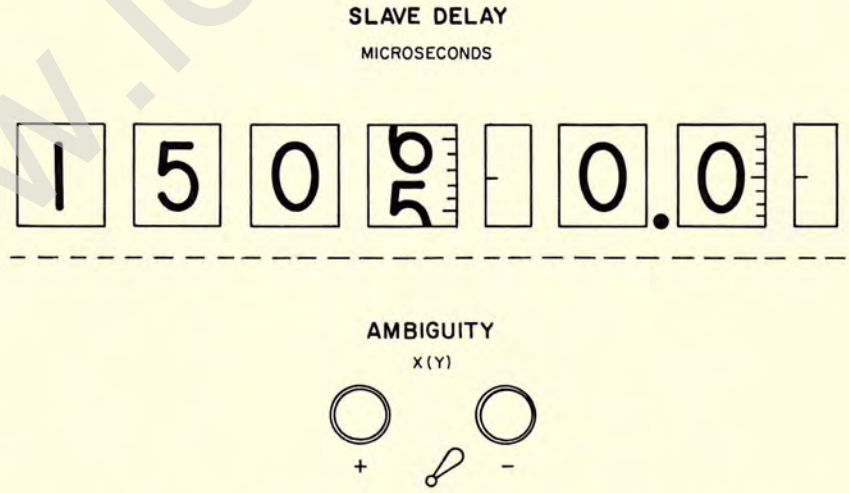


Figure 3-5. Loran Receiver R-963/SPN-30, Ambiguity Indication, Example 2

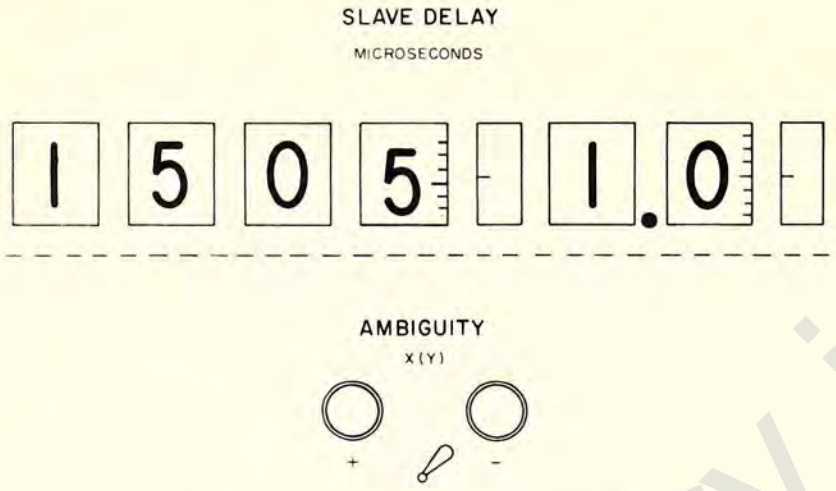


Figure 3-6. Loran Receiver R-963/SPN-30, Ambiguity Indication, Example 3A

that the readings still must be resolved. It might seem that a minus ambiguity would be suspected. However, the history of the previous readings should indicate to the operator that the ambiguity is still positive, but has reached the 10-microsecond point.

Example 3B - ambiguity of more than 10 microseconds in the negative direction (figure 3-7). It is assumed that the receiver has been setup on good information and has been left unattended for a period of time. The first four digits are 1505 and the vernier on the fourth dial reads 1. This means the envelope delay readout is 15051. The cycle delay readout is 1.00, but the + AMBIGUITY light is on. It can be suspected that the cycle delay readout differs from the envelope readout in the negative direction by more than 10 microseconds (up until 10 microseconds, the - AMBIGUITY light was lighted). The true reading will then be 15041. This is not conclusive, but the most probable true reading. If it is possible to check the fix by other navigational means, it should be done to give the operator confidence in his reading.

(2) INDICATOR. - Loran Indicator IP-532/SPN-30, Controls and Indicators, are shown in figure 3-8.

(a) POWER ON. - This switch applies power to the indicator circuits. The indicator is operational after the indicator tube warms up. There is an associated indicator light that lights when the power is on.

(b) FOCUS. - The FOCUS control regulates the sharpness of the trace.

(c) ASTIGMATISM CONTROL. - This screwdriver control is located inside the case at the back of the indicator tube section. The control should be adjusted so that ghosts do not appear on the tube face.

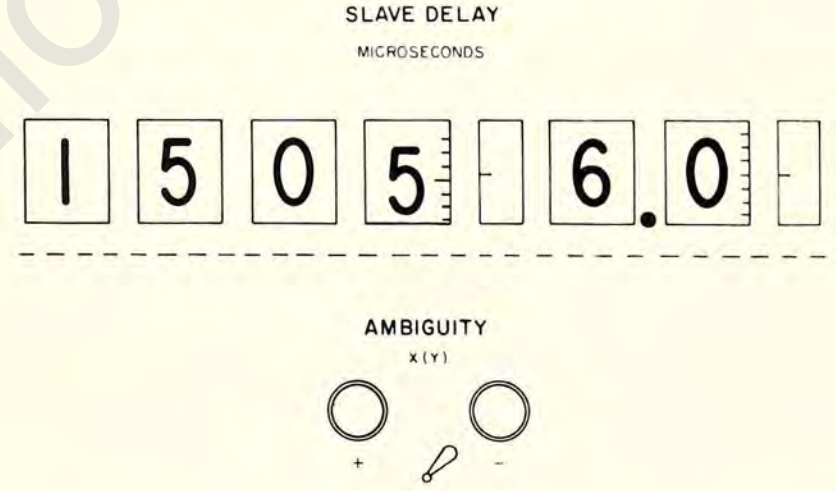


Figure 3-7. Loran Receiver R-963/SPN-30, Ambiguity Indication, Example 3B

(d) INTENSITY. - This control regulates the brightness of the signal traces.

(e) SCALE ILLUM. - This control varies the intensity of the grid scale.

(f) SIGNAL. - This control selects the input signal applied to the indicator. The following positions are available.

1. RF FIL. - The r-f signal detected by the receiver is applied to the indicator. The input attenuator, a narrow-bandpass filter, and two notch filters are inserted between the indicator input and the vertical amplifier section.

2. RF. - This applies the same r-f signal as for the RF FIL position, except the bandpass filter is omitted from the circuit.

3. ENV DET. - This position applies the output of the envelope detector within the receiver circuit to the indicator input.

4. DER ENV. - This position applies the derived envelope output from the detector circuit of the receiver to the indicator input.

5. AGC. - This position applies the pulse chains of the three stations within the set, in square-waveform, to the input of the indicator. The strength of the agc action may be observed by the relative height of the waveforms.

6. PROBE. - This position selects the input inserted at the external PROBE jack located on the face of the indicator.

(g) STROBE. - This control is concentric with the SIGNAL control and is a variable potentiometer used to enlarge the magnitude of the strobe point on the face of the scope. The display of the strobe point may be used as a visual aid to the operator in manually slewing the receiver rapidly to the lock-on position.

(h) VERT SENS (V/CM). - The detent switch attenuates the input signal so that the traces may be kept to a convenient scale on the face of the scope. The CAL knob must be fully clockwise for the scale to be correct as marked.

(i) CAL. - This control is concentric with the VERT SENS (V/CM) control and is used to vary the trace to a level between the detent positions of the VERT SENS (V/CM) control.

(j) R3107 (BANDPASS FILTER PAD). - This screwdriver control on the selective amplifier card (A3101) varies the output level of the bandpass filter.

(k) C3103, C3106, C3109 (TUNING CAPACITORS). - These screwdriver adjustable capacitors, located on the selective amplifier card (A3101), tune the bandpass filter.

(l) NOTCH FILTERS. - These controls each tune a notch filter over the frequency range from 70 kc to 130 kc. The two notch filters may be stacked for a particularly large, unwanted signal.

(m) R6, R7 (NOTCH FILTER ADJUSTMENT). - Each notch filter (A3201 and A3202) has an R6 and an R7 control that is screwdriver adjustable. The R6 control adjusts the width of the notch filter, and R7 adjusts the depth of the notch. Adjustment of either one will have an effect on the other.

(n) C6 (NOTCH FILTER TRIMMING CAPACITOR). - This tunable capacitor on each notch-filter card is a trimming capacitor for calibrating the notch.

(o) R3128 (VERTICAL CALIBRATE). - This control is a screwdriver adjustment on the vertical amplifier cards (A3121). It regulates the level of the output from the vertical amplifier into the vertical deflection amplifier.

(p) R3154 (VERTICAL POSITION). - This control is a screwdriver adjustment on the vertical deflection amplifier card (A3151). The adjustment moves both traces up or down together so that they may be centered on the scope face.

(q) R3168 (TRACE SEPARATOR). - This screwdriver adjustment is on the vertical deflection amplifier card (A3151). It is used to separate the traces or bring them closer together, as desired by the operator.

(r) BASIC PRR. - This is a front panel control for selecting a sweep rate which is compatible with the pulse chains in a Loran-C system. Besides the six basic repetition rate positions, this switch may choose a trigger for the horizontal sweep circuit. This may be either applied from outside the indicator set through the EXT TRIGGER connector or from an internal trigger. The internal trigger is derived from the vertical deflection amplifier.

(s) SPEC PRR. - This control is concentric with the BASIC PRR control. It is used to regulate the exact length of the sweep time for the pulse repetition rate selected when the SWEEP control is placed in the SLOW position.

(t) SWEEP. - This control selects the trace and trace sweep time. There are five positions of the switch.

1. SLOW. - When this position is chosen, all master and slave stations are displayed.

2. M + X(Y) MED AND M + Y(Z) MED. - When this position is chosen, the master group of pulses is presented on the top trace of the scope; and the selected slave station group of pulses is presented on the bottom trace of the scope.

3. M + X(Y) FAST AND M + Y(Z) FAST. - When this position is chosen, the top scope trace is used for display of a single slave pulse. For the top trace, the scope is triggered just prior to each pulse in the master chain of pulses. Therefore, the resulting presentation is a composite of all of the pulses in the chain superimposed on one another. The bottom trace is similarly a composite of all of the pulses in the selected slave chain.

(u) FINE. - This control is concentric with the SWEEP control and is operative when the SWEEP control is in a MED or FAST position. It is used to regulate the exact length of the sweep for its best presentation.

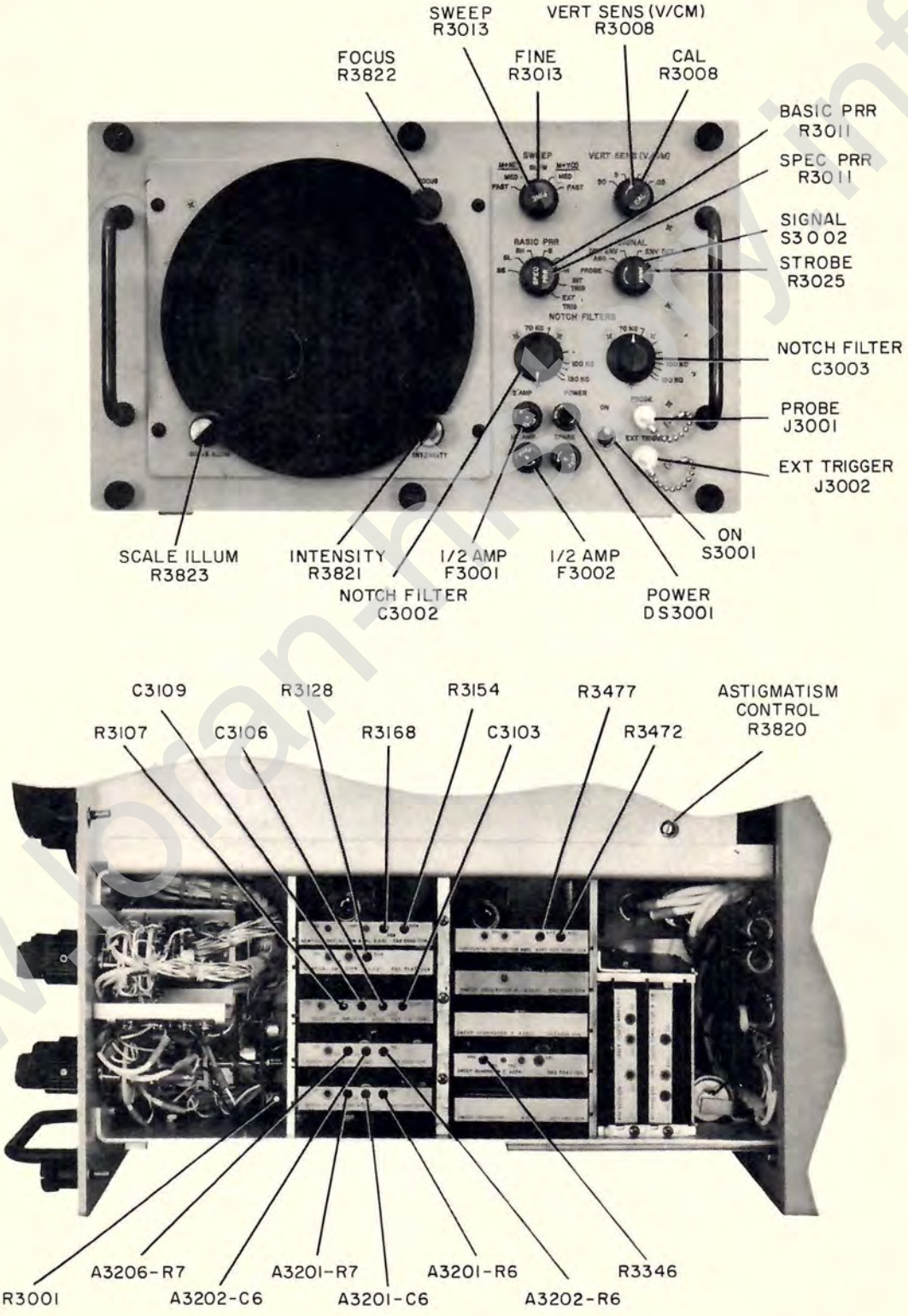


Figure 3-8. Loran Indicator IP-532/SPN-30, Controls and Indicators

(v) R3346 (THRESHOLD). - This is a screwdriver-adjusted control on the sweep generator SA2 card (A3341) for properly adjusting the voltage level at which the Schmitt level detector will trigger the main flip-flop.

(w) R3472 (HORIZONTAL GAIN). - This screwdriver-adjusted control is located on the horizontal deflection amplifier card (A3471). It is used to adjust the gain of the horizontal amplifiers.

(x) R3477 (HORIZONTAL POSITION). - This screwdriver-adjusted control, also located on the horizontal deflection amplifier card (A3471), is used to position the trace on the scope in a horizontal plane.

b. SEQUENCE OF OPERATION.

(1) LOCKING IN ON THE MASTER SIGNAL AUTOMATICALLY.

(a) NORMAL OPERATION PROCEDURES. - Although helpful, this operation does not require monitoring of the lock-on action with the indicator.

Step 1. Turn the HEATER ON-OFF switch to ON. The HEATER indicator light will light. Allow several minutes for warmup.

NOTE

The receiver may be used for locking on a signal after the HEATER light has been on approximately 5 minutes. However, approximately 15 minutes will be required before the frequency completely stabilizes.

Step 2. Turn the RCVR ON-OFF switch to ON. The RCVR indicator light will light. If the HEATER ON-OFF switch has been on a sufficient length of time for the master-crystal frequency to stabilize, the receiver is ready to operate without further warmup time.

Step 3. Place the METER FUNCTION switch on the top drawer to the M CYCLE position.

Step 4. Place the ATTEN switch to the 0 DB position.

Step 5. Place the BAND WIDTH switch to the NORM position.

Step 6. Place the NOTCH FILTERS ON-OFF switch to OFF.

Step 7. Place the ENVL SERVOS switches to their on positions.

Step 8. Place the three GAIN CONTROL switches (bottom drawer) in their manual positions and adjust until the error lights just flicker.

Step 9. Place the REPETITION RATE switches, both BASIC and SPECIFIC, to the desired position to correspond with the repetition rate of the stations with which the receiver is to operate.

Step 10. Place the SEARCH SELECTOR CONTROL to the M position.

Step 11. Place the SEARCH SPEED CONTROL to the 3 position.

Step 12. Depress and release the LEFT slew button. The LEFT indicator light will light.

(b) NORMAL OPERATION INDICATIONS. - The receiver should automatically lock-on to the master signal. Normally, the following indications will be observed as the receiver locks on.

1. The LOST SIG light will be on.
2. The CYCLE ERROR and ENVL ERROR lights will light. The meter will swing to the right or left of center. The LOST SIG light will go out. The LEFT slew light will go out.
3. The CYCLE ERROR light will go out and the meter indication will swing back to the center position.
4. The ENVL ERROR light will go out. If there were no irregularities encountered, no red lights will remain lighted; and the receiver is successfully locked on to the master signal.

(c) IRREGULARITIES. - The following irregularity conditions could occur during the procedure.

SIGNAL OVERLOAD

INTERFERENCE

FREQ ADJUST

SKYWAVE

INTERFERENCE AND SKYWAVE

1. SIGNAL OVERLOAD. - If a Loran-C transmitting signal is too strong for the r-f portion of the receiver, the r-f amplifier will saturate; and the SIGNAL OVERLOAD light will light. When this happens, place the ATTEN switch to 20 DB or 40 DB as required to turn out the SIGNAL OVERLOAD light.
2. INTERFERENCE. - The slew action may continue without result if the signal is extremely weak in proportion to the noise. When this happens, the signal-to-noise ratio may be enhanced by placing the BAND WIDTH control to the NAR position. The NARROW BAND indicator light will light when the switch is in this position. Set the SEARCH SPEED CONTROL to the 1 or 2 position when tracking through a noisy signal.
3. FREQ ADJUST. - After lock-on, the meter will still not be centered (when the METER FUNCTION switch is in the M CYCLE position) if the master oscillator within the receiver has drifted off frequency. Correct the frequency of the receiver by use of the FREQ ADJUST control until the meter is centered.
4. SKYWAVE. - If the receiver locks on a skywave, the SKYWAVE indicator light will light. To lock onto the ground wave signal, switch the SPEED switch to position 1. Depress and hold the RIGHT slew button until the CYCLE ERROR and ENVL ERROR lights come on and then go out. Release the RIGHT slew button. When the ground wave is locked on, the SKYWAVE light will go out. If the CYCLE ERROR and/or ENVL ERROR lights do not immediately relight, depress the STOP button and reverse slewing action by depressing the LEFT slew button.
5. INTERFERENCE AND SKYWAVE. - The SKYWAVE indicator alarm is not a reliable indication of skywave in the presence of noise. Therefore, to insure lock-on of the ground wave under noisy

conditions, the operator must take special precautions as outlined below:

Step 1. Place the METER FUNCTION switch to the M AGC position and the master GAIN CONTROL knob to the manual position.

Step 2. Before a signal is detected by the receiver, the meter on the front panel will point fully to the right.

Step 3. The signal should be slewed to the right by depressing the RIGHT slew button. When the signal is contacted the meter will go in a left direction.

Step 4. Slew right through the signal until the meter gives an indication which is again slightly less than a full left deflection.

Step 5. Depress the LEFT slew button to achieve lock-on, as indicated by a full left swing of the meter.

NOTE

This procedure assures that the receiver has locked on to the leading edge of the r-f waveform, which is the uncontaminated ground wave.

Step 6. Repeat steps 1 through 5 to lock on to each of the slave station signals.

(2) LOCKING IN ON THE SLAVE SIGNALS AUTOMATICALLY.

(a) NORMAL OPERATION PROCEDURES. - After the master signal has been locked on, lock-on of the slaves may be accomplished as follows:

Step 1. Ensure that the ATTEN switch is in the 0 DB position.

Step 2. Ensure that the BAND WIDTH switch is in the NORM position.

Step 3. Ensure that the notch filter ON-OFF switch is in the OFF position.

Step 4. Ensure that the GAIN CONTROL switches are placed in their manual positions.

Step 5. Ensure that the METER FUNCTION switch is in the X(Y) AGC position.

Step 6. Place the SEARCH SELECTOR CONTROL to the X(Y) position.

NOTE

If there are three slaves working in conjunction with the master station, navigation may be achieved by using any of these three combinations: X and Y, X and Z, or Y and Z. Of the pair used, the slave closer to the master signal in time sequence is sought first.

Step 7. Depress and release the LEFT slew button. The LEFT light should light.

(b) NORMAL OPERATION INDICATION. - The receiver should lock onto the first slave signal sought (X or Y) within about 2 minutes. The following indications will be observed as the receiver locks on if everything is functioning normally.

1. The LOST SIG indicator light will light.
2. When the receiver sampling gates and the slave receive signal come close to coincidence, the LOST SIG light and the LEFT slew light will go out; and the CYCLE ERROR and ENVL ERROR lights will light.
3. The ENVL ERROR light and then the CYCLE ERROR light will go out as lock-on is achieved.
4. All of the red lights should be out and the receiver successfully locked in on the first slave station if there have been no irregularities encountered.

The above procedure should be repeated for the second slave by switching the SEARCH SELECTOR CONTROL to the Y(Z) position.

(c) IRREGULARITIES. - The following irregularity conditions could occur during the procedure of locking onto a slave.

SIGNAL OVERLOAD
NARROW BAND
SKYWAVE
EXCESS DELAY
BLINK
AMBIGUITY
INTERFERENCE AND SKYWAVE

1. SIGNAL OVERLOAD. - The r-f amplifier will saturate and the SIGNAL OVERLOAD indicator light will light if a Loran-C transmitting signal is too strong for the r-f portion of the receiver. When this happens, place the ATTEN switch to 20 DB or 40 DB as required to turn out the SIGNAL OVERLOAD light.
2. NARROW BAND. - Slew action may continue without result if the signal is extremely weak in proportion to the noise. When this happens, the signal-to-noise ratio may be enhanced by placing the BAND WIDTH control to the NAR position. The NARROW BAND indicator light will light when the switch is in this position. Set the SEARCH SPEED CONTROL to the 1 or 2 position when the signal is noisy.
3. SKYWAVE. - The SKYWAVE indicator light will light if the receiver locks onto a slave station skywave. To lock onto the ground signal, set the SEARCH SPEED CONTROL to position 1 and hold the LEFT slew button until the CYCLE ERROR and/or ENVL ERROR lights go out. The SKYWAVE light will go out when the ground wave is locked on. If slewing has not automatically stopped after 45 microseconds, operate the STOP button and observe the lights and meter for indication of a ground wave.
4. EXCESS DELAY. - The EXCESS DELAY indicator light will light when the receiver slews to the extent of transgressing upon the preceding station gate without encountering the slave station sought. The LEFT slew light will go out and the RIGHT slew light will light. The EXCESS DELAY light will go out when the gates no longer overlap.
5. BLINK. - It is an indication of possible transmitter-timing trouble when the slave station is continuously locked on and the BLINK light is either flashing on and off or remaining on. The readout information on the SLAVE DELAY counter for the slave in question is unreliable. This is not a receiver

difficulty, but a transmitter warning signal that the transmitter timing relationships are not within allowable tolerances.

6. AMBIGUITY. - When the receiver has locked on a slave station, the strength of the signal can be determined by switching the METER FUNCTION switch on the top drawer to X(Y) AGC or Y(Z) AGC. The transmitted slave signal is strong if the indication is near the maximum left position. An AMBIGUITY light may still light if the meter indicates a strong transmitted signal and the envelope and cycle portions of the SLAVE DELAY counter agree very closely (the envelope vernier and the cycle digit readout are within 1 microsecond). If this happens, turn off the light by switching the associated AMBIGUITY switch to the opposite direction from the way it is set. If continuous lock-on (tracking) is maintained and an AMBIGUITY light comes on, the SLAVE DELAY reading is interpreted as explained in paragraph 3-3*a*(1)*(i)*8.

7. INTERFERENCE AND SKYWAVE. - The SKYWAVE indicator alarm is not a reliable indication of skywave in the presence of noise. Therefore, to insure lock-on of the ground wave under noisy conditions, the operator must take special precautions as outlined in paragraph 3-3*b*(1)*(c)*5.

(3) LOCKING IN ON THE MASTER SIGNAL VISUALLY.

(a) RECEIVER PREPARATION. - First, the receiver must be turned on.

Step 1. Turn the HEATER ON-OFF switch to ON. The HEATER indicator will light. Allow several minutes for warmup.

NOTE

The receiver may be used for locking on a signal after the HEATER light has been on approximately 5 minutes. However, approximately 15 minutes will be required before the frequency completely stabilizes.

Step 2. Turn the RCVR ON-OFF switch to ON. The RCVR indicator will light. If the HEATER ON-OFF switch has been on a sufficient length of time for the master-crystal frequency to stabilize, the receiver is ready to operate without further warmup time.

Step 3. Place the METER FUNCTION switch located on the top drawer to the M CYCLE position.

Step 4. Place the ATTEN switch to the 0 DB position.

Step 5. Place the BAND WIDTH switch to the NORM position.

Step 6. Place the NOTCH FILTERS ON-OFF switch to OFF.

Step 7. Place the ENVL SERVOS switches to their on positions.

Step 8. Place the GAIN CONTROL switches (bottom drawer) to their manual positions.

Step 9. Place the REPETITION RATE switches, both BASIC and SPECIFIC, to the desired position to correspond with the repetition rate of the stations with which the receiver is to operate.

Step 10. Place the SEARCH SELECTOR CONTROL switch to the M position.

Step 11. Place the SEARCH SPEED CONTROL switch to the 5 position.

(b) INDICATOR PREPARATION. - The indicator must be used when locking on to the master signal manually. Use the following procedure to place the indicator in an operational condition:

Step 1. Place the POWER switch to ON. The POWER indicator light will light.

Step 2. Turn the NOTCH FILTERS controls fully clockwise.

Step 3. Place the SIGNAL switch to the ENV DET position.

Step 4. Place the BASIC PRR switch to the basic pulse repetition rate of the receiver.

Step 5. Place the SWEEP control to the SLOW position.

Step 6. Place the VERT SENS (V/CM) switch to the .05 position (the most sensitive), and turn the CAL knob fully clockwise.

Step 7. When the indicator warms up and indicates a signal, adjust the FOCUS, INTENSITY, and SCALE ILLUM controls as suited.

Step 8. Place the STROBE control fully counterclockwise.

Step 9. The gates on the scope face are triggered such that the master is in the upper left corner (start of the top trace), the first slave gate is split between the last portion of the top trace and the first portion of the bottom trace, and the final slave gate is on the end of the bottom trace. However, the chain may be squeezed so that all of the scope face is not utilized or it may be spread so that part of the last slave gate runs off the scope. Obtain maximum utilization of the scope face by turning the SPEC PRR control.

(c) LOCK-ON PROCEDURES. - Use the following procedures to lock on a signal:

Step 1. Initiate slew action by depressing and releasing either the LEFT or RIGHT slew button. Observe the pulses of the stations as they come into the master gate. Three possible scope indications may be observed.

a. A slave station may come into the master gate. When this happens, the first two pulses will extend up, the next two will extend down, then two up, and finally two down.

b. Master M2 may come into the M1 gate. When this happens, the pulses observed will be alternately up and down.

c. Master M1 may come into the M1 gate. All of the pulses will extend in the same direction, either all up or all down.

Step 2. If condition a. occurs, continue slewing for the master signal.

Step 3. If condition b. occurs, depress the GROUP ALTERNATE switch on the lower drawer of the receiver and the M1 signal will immediately be in the M1 gate. Allow the receiver to lock on.

Step 4. If condition c. occurs, allow the receiver to lock-on. The pulses may rock between being all down and all up; but when the receiver has locked on, the pulses will all be up. To speed up lock-on, proceed with step 5.

Step 5. Place the SIGNAL control to the DER ENV position.

Step 6. Place the SWEEP control to a MED or a FAST position.

Step 7. Turn the STROBE control to a convenient position so that the strobe point will be displayed on the scope.

Step 8. Depress the appropriate slew button to move the slew point to the crossover point of the scope display.

(d) IRREGULARITIES. - The following irregular conditions could occur during the procedure of locking on to the master.

FREQUENCY ADJUSTMENT
TOO MUCH GAIN
NOISY CONDITIONS
SIGNAL OVERLOAD
SKYWAVE
INTERFERENCE AND SKYWAVE

1. FREQUENCY ADJUSTMENT. - The meter on the top drawer of the receiver will indicate off-center if the 100-kc reference oscillator has drifted slightly during the lock-on operation. Turn the FREQ ADJUST control to center the meter.

2. TOO MUCH GAIN. - If the pulses as they come into the gate are too large for the face of the scope, they may be attenuated by the VERT SENS (V/CM) control or the concentric CAL control.

3. NOISY CONDITIONS. - Place the BAND WIDTH control on the receiver to the NAR position if there is a general noisy condition. This distorts the information pulses slightly, but greatly improves the signal-to-noise ratio. If there is some identifiable noise in the vicinity of the frequency of the receiver, place the NOTCH FILTERS ON-OFF switch on the top drawer of the receiver to the ON position. Tune one of the controls over the undesirable signal. If there is another unwanted signal, it may be similarly blocked by the other NOTCH FILTERS control; or the NOTCH FILTERS controls may be stacked to block a large interfering signal.

4. SIGNAL OVERLOAD. - The SIGNAL OVERLOAD light on the receiver will light if the receiver is operating so close to a transmitting station that it overdrives the r-f amplifier. When this happens, turn the ATTEN control to the 20 DB position. This effectively alternates the entire input chain of signals, not just the master station input.

5. SKYWAVE. - The SKYWAVE indicator light on the receiver will light when the receiver locks onto a skywave. The skywave and the ground wave will probably both be visible on the scope when this occurs. To lock onto the ground wave, slew the receiver by depressing and releasing the LEFT slew button.

6. INTERFERENCE AND SKYWAVE. - The SKYWAVE indicator alarm is not a reliable indication of skywave in the presence of noise. Therefore, to insure lock-on of the ground wave under noisy conditions, the operator must take special precautions as outlined in paragraph 3-3*b*(1) *(c)*5.

(e) ALTERNATE INDICATOR VIEWS. -

1. SWEEP CONTROL POSITIONS. - Besides the SLOW SWEEP position on the indicator which shows the entire chain of three successive Loran-C gates, two expanded views may be observed.

a. M + X(Y) MED AND M + Y(Z) MED. - The entire master signal, including the ninth pulse, if desired, can be viewed on the top trace when the SWEEP control is placed in a MED position. It may be spread or narrowed as desired by the FINE control. The lower trace presents the entire gate of the selected slave station.

b. M + X(Y) FAST AND M + Y(Z) FAST. - When this position is chosen, the top scope trace is used for display of a single master pulse; and the bottom scope trace is used for display of a single slave pulse. For the top trace, the scope is triggered just prior to each pulse in the master chain of pulses. Therefore, the resulting presentation is a composite of all of the pulses in the chain superimposed on one another. The bottom trace is similarly a composite of all of the pulses in the selected slave chain.

2. SIGNAL CONTROL POSITIONS. - Ordinarily, the ENV DET position is used when manually locking in on the master signal. This presents the signals that come into the gates to the operator. If another input from the receiver is desired to be viewed, switch the SIGNAL control to select the signal input.

a. RF. - In this position, the output from the r-f amplifier is applied to the indicator. The indicator bandpass filter is bypassed; however, the indicator notch filters are left in the circuit. If desired, one or both of the indicator notch filters may be used without affecting the operation of the receiver.

b. RF FIL. - In this position, the same input as for the RF input is selected. Within the indicator circuit, the two notch filters are left in the input circuit and a bandpass filter is added. This position may be used to view extremely noisy r-f conditions, with an improved signal-to-noise ratio, without affecting receiver operation. Again, the indicator notch filters may be inserted if desired.

c. DER ENV. - This position chooses the detected derived envelope waveform from the receiver. The shape of the derived pulse may be readily seen if a single pulse is selected to be observed on the scope.

d. AGC. - The AGC position presents trigger signals with variable amplitude on the scope face. The relative height of the trigger signals shows the relative strength of the signals as used by the detector portion of the receiver. The leading edge of the pulse is used to trigger the guard strobe blocking oscillator and the trailing edge is used to trigger the main strobe blocking oscillator. Therefore, it may be determined which portion of the received signal is being strobed.

e. PROBE. - The PROBE position selects the input to the scope which is inserted at the PROBE jack on the front of the indicator.

(4) LOCKING IN ON THE SLAVE SIGNALS VISUALLY.

(a) LOCK-ON PROCEDURE. - The slave signals may be locked on visually in much the same manner as the master signal.

Step 1. Place the SEARCH SELECTOR CONTROL on the bottom drawer of the receiver to the X(Y) position.

Step 2. Ensure that the REPETITION RATE controls, GAIN CONTROL, ATTEN control, BAND WIDTH control, and NOTCH FILTERS controls on the receiver are in the same positions that they were when the receiver was locking in on the master station.

Step 3. On the indicator, place the SWEEP control to SLOW, the VERT SENS (V/CM) control to a convenient position for viewing the trace, and the SIGNAL control to ENV DET.

Step 4. Depress and release the slew RIGHT or LEFT button on the receiver until the first slave signal approaches lock-on. As for the master signal, slave lock-on will be shown by the pulses all appearing in the same direction.

Step 5. Place the SIGNAL control to the DER ENV position.

Step 6. Place the SWEEP control to the M + X(Y) MED or M + X(Y) FAST position.

Step 7. Turn the STROBE control to a convenient position so that the strobe point will be displayed on the scope.

Step 8. Depress the appropriate slew button to move the slew point to the crossover point of the scope display.

Step 9. Switch the SEARCH SELECTOR CONTROL on the receiver to the Y(Z) position.

Step 10. Place the SIGNAL control on the indicator to ENV DET.

Step 11. Place the SWEEP control on the indicator to SLOW.

Step 12. Depress and release the slew RIGHT or the slew LEFT button on the receiver until the second slave signal approaches lock-on.

Step 13. Place the SIGNAL control to the DER ENV position.

Step 14. Place the SWEEP control to the M + Y(Z) MED or M + Y(Z) FAST position.

Step 15. Turn the STROBE control to a convenient position so that the strobe point will be displayed on the scope.

Step 16. Depress the appropriate slew button to move the slew point to the crossover point of the scope display.

(b) IRREGULARITIES. - The following irregularity conditions could occur during the lock-on of the slaves:

SIGNAL OVERLOAD
NOISE AND INTERFERENCE
SKYWAVE
INTERFERENCE AND SKYWAVE
EXCESS DELAY
BLINK
AMBIGUITY

1. SIGNAL OVERLOAD. - The r-f amplifier may be saturated if the receiver is located too near a slave transmitting station (or any station which is broadcasting on 100 kc). This will cause the SIGNAL OVERLOAD light on the receiver to light. When this happens, place the ATTEN switch to the 20 DB or 40 DB position. This attenuates all signals on the antenna of the receiver, not just the offensive station.

The VERT SENS (V/CM) control may be used to adjust the signal to the desired amplitude if the particular signal does not flood the receiver, but is too strong for the indicator. If the exact scale division is not important, the CAL switch is a fine control to regulate the pulse height between detents of the VERT SENS (V/CM) control.

2. NOISE AND INTERFERENCE. - There are receiver switches which may be used to alleviate the problem when the Loran-C signals are being bothered by noisy conditions. Switch the BAND WIDTH control on the receiver to the NAR position for generally noisy conditions. This improves the signal-to-noise ratio during tracking, but also distorts the signal somewhat. Therefore, switch the BAND WIDTH control back to the NORM position before a reading is taken. The NARROW BAND indicator light will be on while the BAND WIDTH control is in the NAR position.

There will be a small time delay added to the internal signals in the form of switching transients when the BAND WIDTH control is switched from NAR to NORM. When this happens, the receiver must settle again to lock on the received signal. Switching transients will again be introduced when the BAND WIDTH control is switched from NORM to NAR. This time there will be a delay subtracted from the internal signals.

If there is a specific interfering signal close to the 100-kc Loran-C frequency, it may be attenuated by the NOTCH FILTERS controls. Turn the NOTCH FILTERS ON-OFF switch on the receiver to the ON position. Tune one or both NOTCH FILTERS controls until the undesired signal is attenuated. The two notch filters may be used independently for two signals or may be stacked for one large one.

Turn the SEARCH SPEED CONTROL to the 1 or 2 position for searching when conditions are noisy.

3. SKYWAVE. - The SKYWAVE light will light if the receiver locks onto a slave station skywave. To lock onto the ground-wave signal, set the SEARCH SPEED CONTROL to position 1 and hold the LEFT slew button until the CYCLE ERROR and/or ENVL ERROR lights go out. The SKYWAVE light will go out when the ground wave is locked on. If the slewing has not automatically stopped after 45 microseconds, operate the STOP button and observe the lights and meter for indication of a ground wave.

4. INTERFERENCE AND SKYWAVE. - The SKYWAVE indicator alarm is not a reliable indication of skywave in the presence of noise. Therefore, to insure lock-on of the ground wave under noisy conditions, the operator must take special precautions as outlined in paragraph 3-3*b*(1)*(c)*5.

5. EXCESS DELAY. - When the slew action has taken a slave signal of the receiver to either extremity of its gate so that it interferes with the gate next to it, one of the gates will disappear and the slew action reverses. When this happens, the EXCESS DELAY light will remain lighted until slew has uncovered the gate overlap and the opposite slew indicator light becomes lighted. Ordinarily, this happens very rapidly so that the gate which disappears, quickly reappears.

6. BLINK. - A slave transmitting station will shift its transmit signal every 1.5 seconds when it has an indication that its timing relationship with respect to the master is no longer correct. This will blink the BLINK indicator light or cause it to remain steadily on. This is only a warning to the operator that his time delay reading is not reliable. Switch the SEARCH SELECTOR CONTROL to the X(Y) position and then to the Y(Z) position to identify the blinking slave station. The BLINK light only monitors the slave signal selected by the switch.

7. AMBIGUITY. - The AMBIGUITY lights are only meaningful after they have been originally set up on good, clear information. The AMBIGUITY lights, if lighted, should be turned off by switching the associated AMBIGUITY switch to its alternate position when lock-on has been accomplished and the envelope dials (vernier scale) and the cycle dials (arabic numbers) of the SLAVE DELAY readout are very close (within 1 microsecond). Thereafter, if an indicator light comes on, it should be interpreted as explained in paragraph 3-3*a*(1)*(i)*8.

(c) ALTERNATE INDICATOR VIEWS. - The same alternate indicator views as explained for the master station may be viewed for the slave stations. The SWEEP control may be used to select the master and either slave group of pulses or a master and the corresponding slave signal pulse.

(5) MASTER MULTIPLE. - This position may be used under extremely noisy conditions when no signals can be observed on the indicator. If signals can be observed on the indicator, lock-on can be accomplished faster by using this switch position and the procedures in paragraphs 3-3*b*(3) and (4).

(a) LOCK-ON PROCEDURES. - Ordinarily, there are four different codes generated in the receiver in this sequence: M1, S1, S1, M2, S2, S2. The M MULT position of the SEARCH SELECTOR CONTROL should be selected to lock on to the master signal quickly. This makes the receiver generate all M1 codes. Use the following procedures to lock onto the master.

Step 1. Place the METER FUNCTION switch to the M CYCLE position.

Step 2. Place the ATTEN control to 0 DB.

Step 3. Place the BAND WIDTH control to NORM.

Step 4. Place the NOTCH FILTERS ON-OFF control to OFF.

Step 5. Place the REPETITION RATE controls to the desired repetition rate.

Step 6. Place the SEARCH SELECTOR CONTROL to the M MULT position.

Step 7. Place the SEARCH SPEED CONTROL to the 2 position (or faster if the signal-to-noise conditions are favorable).

Step 8. Place the three GAIN CONTROL switches to their manual positions and adjust until the error lights just flicker.

Step 9. Place all of the ENVL SERVOS to their OFF positions.

Step 10. Slew for lock-on with the receiver slew controls by depressing and releasing the LEFT slew button and observing the CYCLE ERROR indicator.

Step 11. Each time slew action stops and the CYCLE ERROR indicator flashes, push the LEFT slew button. Automatic search is sometimes halted by large noise bursts.

Step 12. If noise continually flashes the CYCLE ERROR indicator and stops slew action, place the three GAIN CONTROL switches at a level where noise will not stop slew action too frequently.

Step 13. When the CYCLE ERROR light stays on, the master signal is in one of the gates.

Step 14. Turn on the M ENVL SERVOS switch.

Step 15. Place the SEARCH SELECTOR CONTROL to the M position (to erase all memory that may have been set up by noise bursts) and then back to the M MULT position.

Step 16. If the CYCLE ERROR light remains on, push the STOP button.

Step 17. Place the SEARCH SELECTOR CONTROL to the M position. If the CYCLE ERROR light stays on and, after a period of time, goes out, the receiver is locked on. If the light goes out as soon as the SEARCH SELECTOR CONTROL is switched to M, depress the GROUP ALTERNATE button.

Step 18. If the light does not come back on, the master signal was probably in a slave gate. Continue slewing as before if this is the case.

Step 19. Turn the M GAIN CONTROL to AGC once the master signal has been locked on.

Step 20. Before starting to slew for X, turn on the X ENVL SERVOS switch and turn the SEARCH SELECTOR CONTROL to the X(Y) position. Slew in the direction of decreasing time delay (as observed by the X SLAVE DELAY readout).

Step 21. Repeat Step 20. for the Y slave.

(b) IRREGULARITIES. - The same irregularity conditions may exist as when searching in the M position, described in paragraph 3-3*b*(1).

(6) TRACKING.

(a) NORMAL SWITCH POSITIONS. - The receiver may be unattended when it is tracking. It will track all signals as long as the r-f signal remains within the receiver capabilities. The receiver knobs should be placed in the following positions for normal tracking.

1. The METER FUNCTION switch to M CYCLE.
2. The ATTEN switch to the 0 DB position, if possible (if the SIGNAL OVERLOAD light does not light).
3. The BAND WIDTH control to NORM.
4. The NOTCH FILTERS controls to ON or OFF, as desired.

5. The GAIN CONTROL switches to AGC.
6. The SEARCH SELECTOR CONTROL to OPR.
7. The SEARCH SPEED CONTROL to 3.
8. The REPETITION RATE CONTROL to the desired rate.
9. The ENVL SERVOS switches to on (or OFF if desired).

NOTE

The operating tracking range of the receiver may be extended when there is noisy or interference conditions. The receiver must be capable of lock-on as previously described in these procedures. This means that the units delay as read on the vernier scale on the last envelope dial is the same number as read on the first, or units, cycle dial. If the ENVL SERVOS switches are then turned to their OFF positions, the cycle servoloops will then drive the entire readout and there will be no apparent envelope-cycle discrepancy. Hence, the problem of noise, which normally affects the envelope dials to a greater extent than the cycle dials, has been reduced.

(b) INDICATORS. - The indicator lights are monitoring all three stations while the receiver is tracking in the OPR position of the SEARCH SELECTOR CONTROL. Should a light come on, switch the SEARCH SELECTOR CONTROL to the M, X(Y), and Y(Z) positions to see which station is encountering the difficulty. Some of the lights work on a time-shared basis. In these cases, the light will blink when trouble occurs. Turn the SEARCH SELECTOR CONTROL away from the OPR position to each of the single-station positions to see which signal keeps the light on.

The lights that are not time-shared will remain on continuously (not blinking) when just one of the stations is blinking. When this occurs, switch the SEARCH SELECTOR CONTROL to the M, X(Y), and Y(Z) positions. The light will go out for the stations not blinking. The light will remain on for the station or stations blinking.

The indicator setup in no way affects the operation of the receiver. Therefore, any desired indicator presentation may be selected for viewing as desired by the operator.

3-4. SUMMARY OF OPERATING PROCEDURES.

The following tables outline a step-by-step procedure for operating the AN/SPN-30 equipment to perform its various functions. For a more detailed explanation of what happens when the procedures are performed, refer to paragraph 3-3.

TABLE 3-1. NORMAL SEARCHING OF MASTER WITHOUT USING THE INDICATOR

INITIAL SETTINGS		
CONTROL	POSITION	INDICATION, IF ANY
1. HEATER ON-OFF	ON	HEATER light comes on
2. RCVR ON-OFF	ON	RCVR light comes on
3. METER FUNCTION	M CYCLE	
4. ATTEN	0 DB	
5. BAND WIDTH	NORM	
6. NOTCH FILTERS ON-OFF	OFF	
7. LIGHTS	As desired	
8. ENVL SERVOS	ON	
9. GAIN CONTROL switches	Manual	
10. BASIC and SPECIFIC REPETITION RATE	Proper repetition rate	
11. SEARCH SELECTOR CONTROL	M	
12. SEARCH SPEED CONTROL	3	
13. LEFT slew button	depress and release	LEFT light comes on

TABLE 3-1. NORMAL SEARCHING OF MASTER WITHOUT USING THE INDICATOR (Cont)

INDICATION OF LOCK-ON ACTION		
INDICATOR	**INDICATION**	
1. LOST SIG light	Light comes on	
2. CYCLE ERROR and ENVL ERROR lights	Lights come on	
3. Meter	Swings to right of center	
4. LOST SIG light	Light goes out	
5. LEFT slew light	Light goes out	
6. CYCLE ERROR light	Light goes out	
7. Meter	Swings back to center position	
8. ENVL ERROR light	Light goes out	
IRREGULARITIES		
CONDITION	**INDICATION**	**REMEDY**
1. Too strong signal	SIGNAL OVERLOAD light comes on	Place ATTEN switch to 20 DB or 40 DB
2. Noisy operating conditions	Slew action does not lock on receiver	(a) Place BAND WIDTH control to NAR (b) Place SEARCH SPEED CONTROL to 1 of 2
3. Frequency drift of 100-kc oscillator	Meter drifts off the center position	Adjust meter back to center position with the FREQ ADJUST control
4. Lock-on of skywave	SKYWAVE light comes on	Depress and release the RIGHT slew button
5. Presence of skywave under noisy conditions	SKYWAVE light blinking indiscriminately during lock-on	(a) Place METER FUNCTION switch in M AGC position and M GAIN CONTROL to manual (b) Slew ahead of received r-f wave until meter swings negative and then positive. (c) Slew back onto leading edge until meter again swings negatively

TABLE 3-2. NORMAL SEARCHING OF SLAVES WITHOUT USING THE INDICATOR

INITIAL SETTINGS		
CONTROL	**POSITION**	**INDICATION, IF ANY**
1. ATTEN	0 DB	
2. BAND WIDTH	NORM	
3. NOTCH FILTERS ON-OFF	OFF	
4. GAIN CONTROL switches	Manual	
5. SEARCH SELECTOR	X(Y) or Y(Z)	
6. LEFT slew button	Depress and release	LEFT light comes on

TABLE 3-2. NORMAL SEARCHING OF SLAVES WITHOUT USING THE INDICATOR (Cont)

INDICATION OF LOCK-ON ACTION		
INDICATOR	**INDICATION**	
1. LOST SIG light	Light turns on	
2. CYCLE ERROR and ENVL ERROR lights	Light turns on	
3. LOST SIG light	Light goes out	
4. LEFT slew light	Light goes out	
5. CYCLE ERROR light	Light goes out	
6. ENVL ERROR light	Light goes out	
IRREGULARITIES		
CONDITION	**INDICATION**	**REMEDY**
1. Too strong signal	SIGNAL OVERLOAD light comes on	Place ATTEN switch to 20 DB or 40 DB
2. Noisy operating conditions	Slew action does not lock on receiver	(a) Place BAND WIDTH control to NAR (b) Place SEARCH SPEED CONTROL to 1 or 2
3. Lock-on skywave	SKYWAVE light comes on	Depress and release the RIGHT slew button
4. Presence of skywave under noisy conditions	SKYWAVE light blinking indiscriminately during lock-on	(a) Place METER FUNCTION switch in X(Y) AGC or Y(Z) AGC position and X(Y) or Y(Z) GAIN CONTROL to manual (b) Slew ahead of received r-f wave until meter swings negative and then positive (c) Slew back onto leading edge until meter again swings negatively
5. Excess delay	EXCESS DELAY light comes on, LEFT slew light goes out, and RIGHT slew light comes on	Slew action reverses automatically and EXCESS DELAY light goes out
6. Blink	BLINK light begins to flash	Transmitter trouble. Must wait for light to stop before a reading can be taken
7. Ambiguity (a) immediately following initial lock-on of good data	If any AMBIGUITY light comes on	Place associated switch to alternate position
(b) after the transmit signal has become somewhat weak	(1) + AMBIGUITY light comes on (2) - AMBIGUITY light comes on	(1) Interpret readout of envelope portion of scale to the next higher digit (2) Interpret readout of envelope portion of scale to the next lower digit as explained in paragraph 3-3*a*(1)*(i)*8

TABLE 3-3. SEARCHING OF MASTER VISUALLY

RECEIVER INITIAL SETTINGS		
CONTROL	POSITION	INDICATION, IF ANY
1. HEATER ON-OFF	ON	HEATER light comes on
2. RCVR ON-OFF	ON	RCVR light comes on
3. METER FUNCTION	M CYCLE	
4. ATTEN	0 DB	
5. BAND WIDTH	NORM	
6. NOTCH FILTERS ON-OFF	OFF	
7. ENVL SERVOS	ON	
8. GAIN CONTROL switches	Manual	
9. BASIC and SPECIFIC REPETITION RATE	Proper repetition rate	
10. SEARCH SELECTOR CONTROL	M	
11. SEARCH SPEED CONTROL	5	
INDICATOR INITIAL SETTINGS		
CONTROL	POSITION	INDICATION, IF ANY
1. POWER ON	ON	POWER light comes on
2. NOTCH FILTERS	Fully clockwise	
3. SIGNAL	ENV DET	
4. BASIC PRR	Proper basic repetition rate	
5. SWEEP	SLOW	
6. VERT SENS (V/CM)	0.5	
7. CAL	Fully clockwise	
8. FOCUS	As desired	
9. INTENSITY	As desired	
10. SCALE ILLUM	As desired	
11. SPEC PRR	Unit the full face of the scope is utilized	
LOCK-ON PROCEDURE		
ACTION	RESULT	INDICATION, IF ANY
1. LEFT or RIGHT slew button	(a) Slave station comes into master gate (b) M2 comes into M1 gate or M1 comes into M2 gate (c) M1 comes into M1 gate and M2 comes into M2 gate	(a) Alternate groups of two pulses up and down (b) Every other pulse up and down (c) All pulses in the same direction
2. If condition (b) above occurs, depress and release GROUP ALTERNATE switch	M1 will be in the M1 gate and M2 will be in the M2 gate	All pulses in the same direction
3. SWEEP control to a MED or FAST position, SIGNAL control to DER ENV, STROBE control clockwise	Slew for exact lock-on	Coincidence of slew point and cross-over point on top trace

TABLE 3-3. SEARCHING OF MASTER VISUALLY (Cont)

IRREGULARITIES		
CONDITION	INDICATION	REMEDY
1. Frequency drift of 100-kc oscillator	Meter drifts off the center position	Adjust meter back to center position with the FREQ ADJUST control
2. Too much gain within indicator	Pulses on scope face overlap when they come into gate	Turn to next scale with VERT SENS (V/CM) control and CAL control
3. Noisy operating conditions	Slew action does not lock on receiver; large noise comes into gate on scope	(a) Place BAND WIDTH control to NAR (b) Place NOTCH FILTERS ON-OFF switch on receiver to ON and tune out noise with the NOTCH FILTERS controls
4. Too strong signal	SIGNAL OVERLOAD light comes on	Place ATTEN switch to 20 DB or 40 DB
5. Lock-on of skywave	SKYWAVE light comes on	Depress and release the RIGHT slew button
6. Presence of skywave under noisy conditions	SKYWAVE light blinking indiscriminately during lock-on	(a) Place METER FUNCTION switch in M AGC position and M AGC position and M GAIN CONTROL to manual (b) Slew ahead of received r-f wave until meter swings negative and then positive (c) Slew back onto leading edge until meter again swings negatively

TABLE 3-4. SEARCHING OF SLAVES VISUALLY

LOCK-ON PROCEDURE		
CONTROL	POSITION	INDICATION, IF ANY
1. SEARCH SELECTOR CONTROL	X(Y)	
2. BASIC and SPECIFIC REPETITION RATE	Proper repetition rate	
3. GAIN CONTROL switches	Manual	
4. ATTEN	0 DB	
5. NOTCH FILTERS ON-OFF	OFF	
6. SWEEP (indicator)	SLOW	
7. VERT SENS (V/CM)	Convenient position	
8. SIGNAL control	ENV DET	
9. LEFT or RIGHT slew button	depress and release	When all pulses are in the same direction, slave is in its gate

TABLE 3-4. SEARCHING OF SLAVES VISUALLY (Cont)

LOCK-ON PROCEDURE		
CONTROL	**POSITION**	**INDICATION, IF ANY**
10. SWEEP (indicator)	M + X(Y) MED or M + X(Y) FAST	
11. SIGNAL	DER ENV	
12. STROBE	Clockwise to convenient position	Coincidence of slew point and crossover point on bottom trace
13. SEARCH SELECTOR CONTROL	Y(Z)	
14. SWEEP (indicator)	SLOW	
15. LEFT or RIGHT slew button	Depress and release	When all pulses are in the same direction, slave is in its gate
16. SWEEP (indicator)	M + Y(Z) MED or M + Y(Z) FAST	
17. SIGNAL	DER ENV	
18. STROBE	Clockwise to convenient position	Coincidence of slew point and crossover point on bottom trace

IRREGULARITIES		
CONDITION	**INDICATION**	**REMEDY**
1. Too strong signal	SIGNAL OVERLOAD light comes on	Place ATTEN switch to 20 DB or 40 DB
2. Noisy operating conditions	Slew action does not lock on receiver	(a) Place BAND WIDTH control to NAR (b) Place SEARCH SPEED CONTROL to 1 or 2
3. Lock-on skywave	SKYWAVE light comes on	Depress and release the RIGHT slew button
4. Presence of skywave under noisy conditions	SKYWAVE light blinking indiscriminately during lock-on	(a) Place METER FUNCTION switch in X(Y) AGC or Y(Z) AGC position and X(Y) or Y(Z) GAIN CONTROL to manual (b) Slew ahead of received r-f wave until meter swings negative and then positive (c) Slew back onto leading edge until meter again swings negatively
5. Excess delay	EXCESS DELAY light comes on, LEFT slew light goes out, and RIGHT slew light comes on	Slew action reverses automatically and EXCESS DELAY light goes out
6. Blink	BLINK light begins to flash	Transmitter trouble. Must wait for light to stop before a reading can be taken
7. Ambiguity (a) immediately following initial lock-on of good data (b) after the transmit signal has become somewhat weak	If any AMBIGUITY light comes on (1) + AMBIGUITY light comes on (2) - AMBIGUITY light comes on	Place associated switch to alternate position (1) Interpret readout of envelope portion of scale to the next higher digit (2) Interpret readout of envelope portion of scale to the next lower digit as explained in paragraph 3-3*a*(1)*(i)*8

TABLE 3-5. SEARCHING OF MASTER IN THE MASTER MULTIPLE POSITION OF THE SEARCH SELECTOR CONTROL

CONTROL	POSITION	INDICATION, IF ANY
1. METER FUNCTION	M CYCLE	
2. ATTEN	0 DB	
3. BAND WIDTH	NORM	
4. NOTCH FILTERS ON-OFF	OFF	
5. GAIN CONTROL switches	manual	
6. ENVL SERVOS	OFF	
7. BASIC and SPECIFIC REPETITION RATE	proper repetition rate	
8. SEARCH SELECTOR CONTROL	M MULT	
9. SEARCH SPEED CONTROL	2 (or faster)	CYCLE ERROR indicator
10. STOP button	Depress	
11. If there is failure to lock on, GROUP ALTERNATE switch	Depress and release	

TABLE 3-6. TRACKING OF STATIONS

CONTROL	POSITION	INDICATION, IF ANY
1. METER FUNCTION	M CYCLE	
2. ATTEN	0 DB (if SIGNAL OVERLOAD does not light)	
3. BAND WIDTH	NORM	
4. NOTCH FILTERS ON-OFF	OFF or ON, as desired	
5. GAIN CONTROL switches	Manual	
6. SEARCH SELECTOR CONTROL	OPR	
7. SEARCH SPEED CONTROL	3	
8. BASIC and SPECIFIC REPETITION RATE	Proper repetition rate	
9. ENVL SERVOS	On or OFF, as desired	

TABLE 3-7. ALTERNATE USE OF INDICATOR

DESIRED USE	HOW ACCOMPLISHED	INDICATION, IF ANY
1. Manual gain; viewing of agc action on scope face	Place M GAIN CONTROL X(Y) GAIN CONTROL, or Y(Z) GAIN CONTROL away from AGC position	(a) With METER FUNCTION switch in the M AGC, X(Y) AGC, or Y(Z) AGC position, proper agc is indicated by centering meter

TABLE 3-7. ALTERNATE USE OF INDICATOR (Cont)

DESIRED USE	HOW ACCOMPLISHED	INDICATION, IF ANY
		(b) With SIGNAL control on scope to AGC, relative trace height reflects relative signal strength
2. Medium pulse sweep	Place SWEEP control to M + X(Y) MED or M + Y(Z) MED position	Top trace is master chain (ninth pulse may be seen by use of FINE control); bottom trace is the selected slave chain
3. Fast pulse sweep	Place SWEEP control to M + X(Y) FAST or M + Y(Z) FAST position	Top trace is a composite master pulse; bottom is a composite slave pulse
4. R-F input; capabilities of using indicator notch filters	Place SIGNAL control to RF position	
5. R-f input, capabilities of using indicator notch filters and the narrow-bandpass filter	Place SIGNAL control to RF FIL position	
6. Derived envelope input	Place SIGNAL control to DER ENV	
7. External input	Place SIGNAL control to PROBE; insert input at PROBE jack	
8. Internal trigger by the vertical circuit	Place BASIC PRR control to INT TRIG	
9. External trigger	Place BASIC PRR control to EXT TRIG; insert external trigger at EXT TRIGGER jack	

3-5. EMERGENCY OPERATION.

There are no operating procedures other than those listed in paragraphs 3-3 and 3-4. If there is any indication of a malfunction, the RCVR ON-OFF switch should be immediately placed in the OFF position. Jamming will have no effect on the receiver and will appear to be only normal interference.

3-6. OPERATOR'S MAINTENANCE.

Because of the possibility of disturbing critical adjustments, as a rule the operator should avoid opening both the receiver and the indicator cabinets. Therefore, for the most part, the operator's maintenance should be confined to checks of the fuses, the indicator lamps, and the air filters. If, however, it becomes necessary for the operator to perform more detailed maintenance on the equipment, the location of modules and internal fuses may be determined by reference to figure 3-8 for the indicator, and to figures 3-9 through 3-14 for the receiver. Lubrication of the unit is not required.

a. FUSES. - The receiver has four 115-volt fuses on the front panel. Two are rated at 3/4 ampere and two are rated at 4 amperes. There is one spare of each type on the front panel. Should a fuse blow, the spare should be replaced as soon as possible. There are additional fuses at the rear of the cabinet. These fuses should not blow unless there is a major circuit malfunction. The operator should not attempt to replace these fuses.

There are two 1/2-ampere, 115-volt fuses on the indicator front panel. A spare fuse is also provided. Should a fuse blow, this spare should be replaced as soon as possible.

b. INDICATOR LAMPS. - The indicator lamps on the receiver may be tested after the RCVR ON-OFF switch has been turned to ON. Depress the lamps one at a time to determine if every lamp will light. If any lamp does not light, it should be immediately replaced. A daily check of these lamps is recommended.

c. AIR FILTERS. - There are three air filters on the receiver, one on each side and one in the back of the cabinet. Once a week these should be inspected for accumulation of dust. If any appears, the filters should be snapped off and cleaned with soap and water.

CAUTION

Do not use cleaning solvent. The filters are plastic and may be damaged by solvents. After the filters are clean, they should be thoroughly dried before they are replaced.

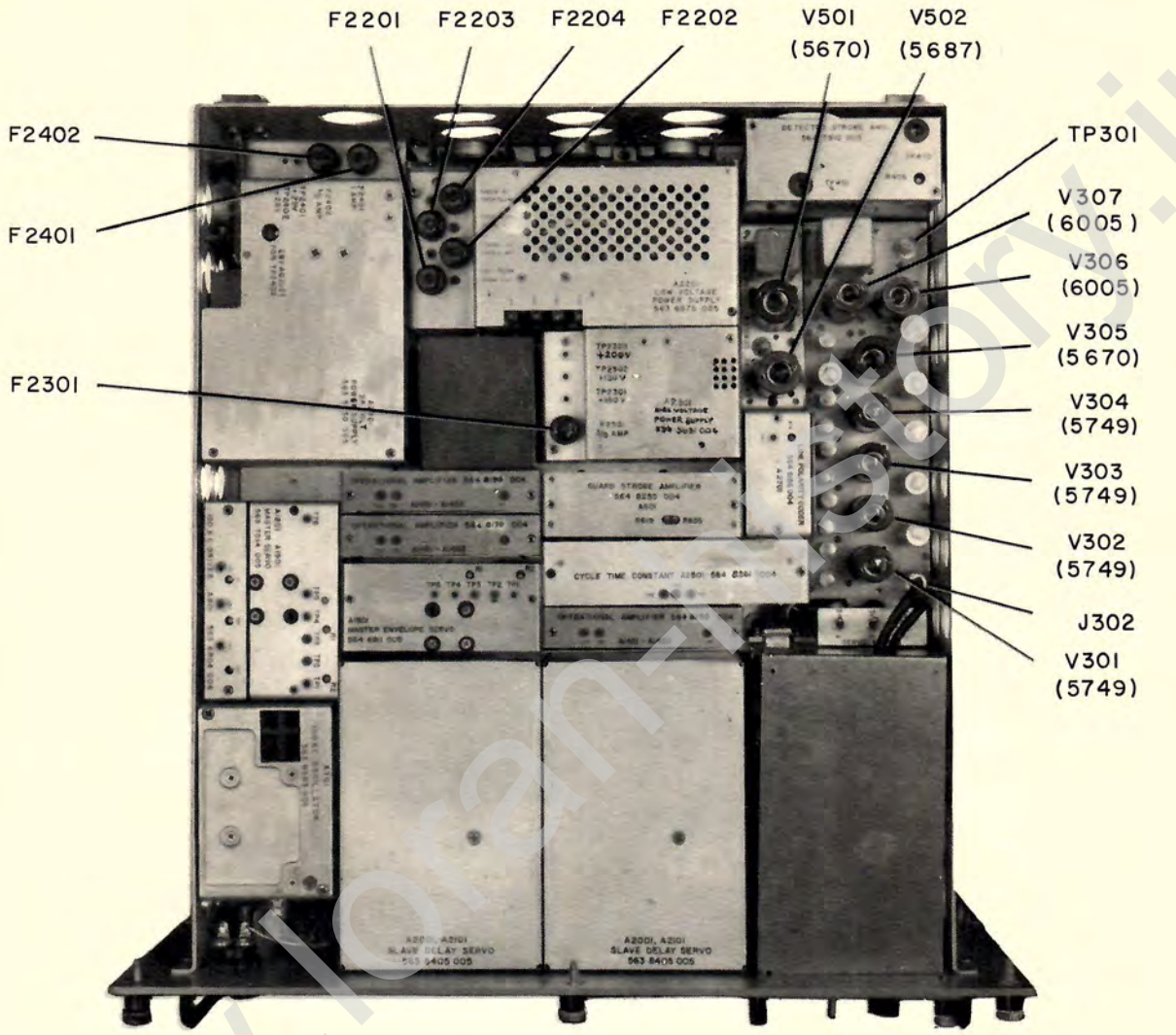


Figure 3-9. Loran Receiver R-963/SPN-30, Top Drawer, Tube and Fuse Location

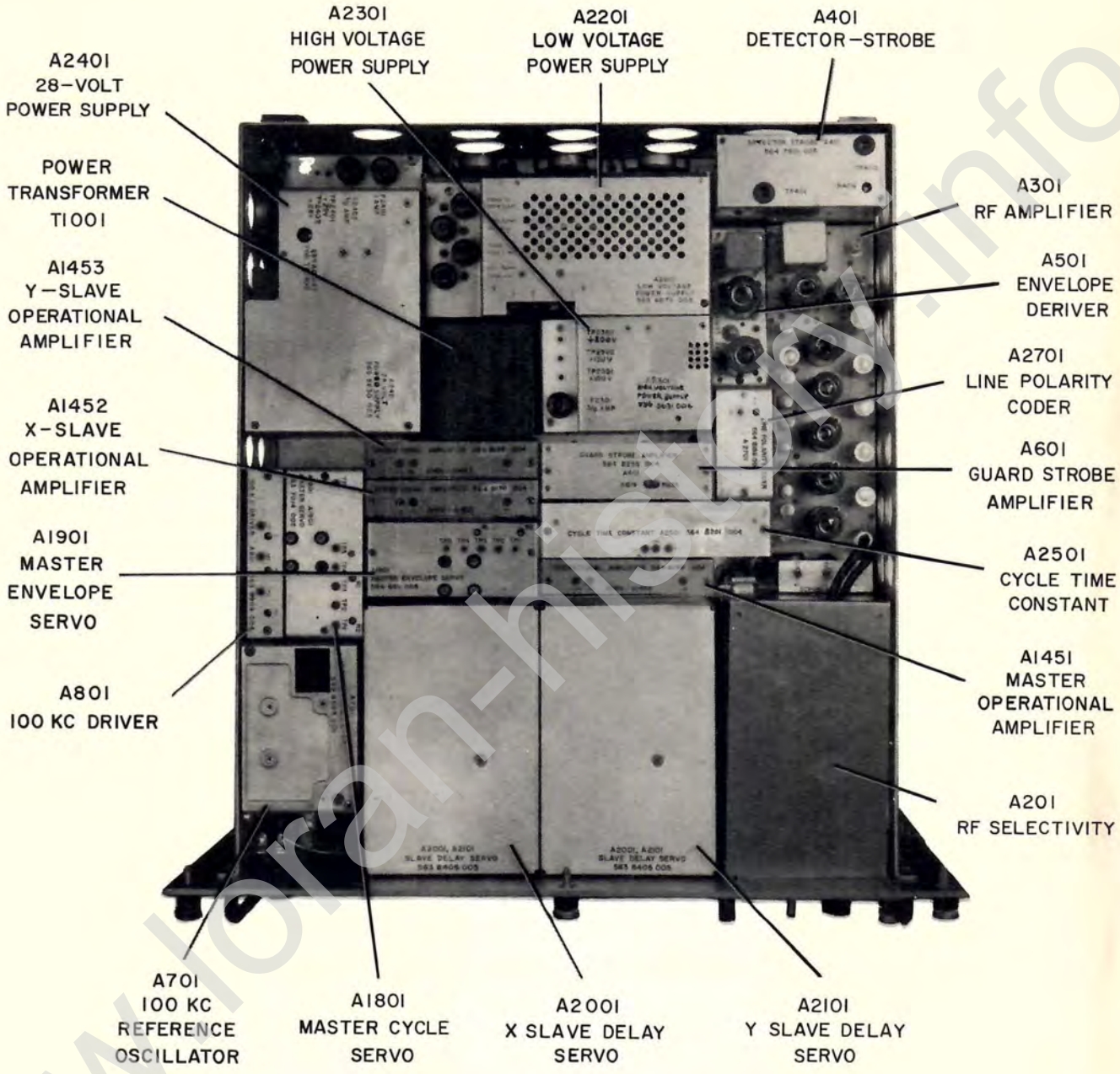


Figure 3-10. Loran Receiver R-963/SPN-30, Top Drawer, Module Location

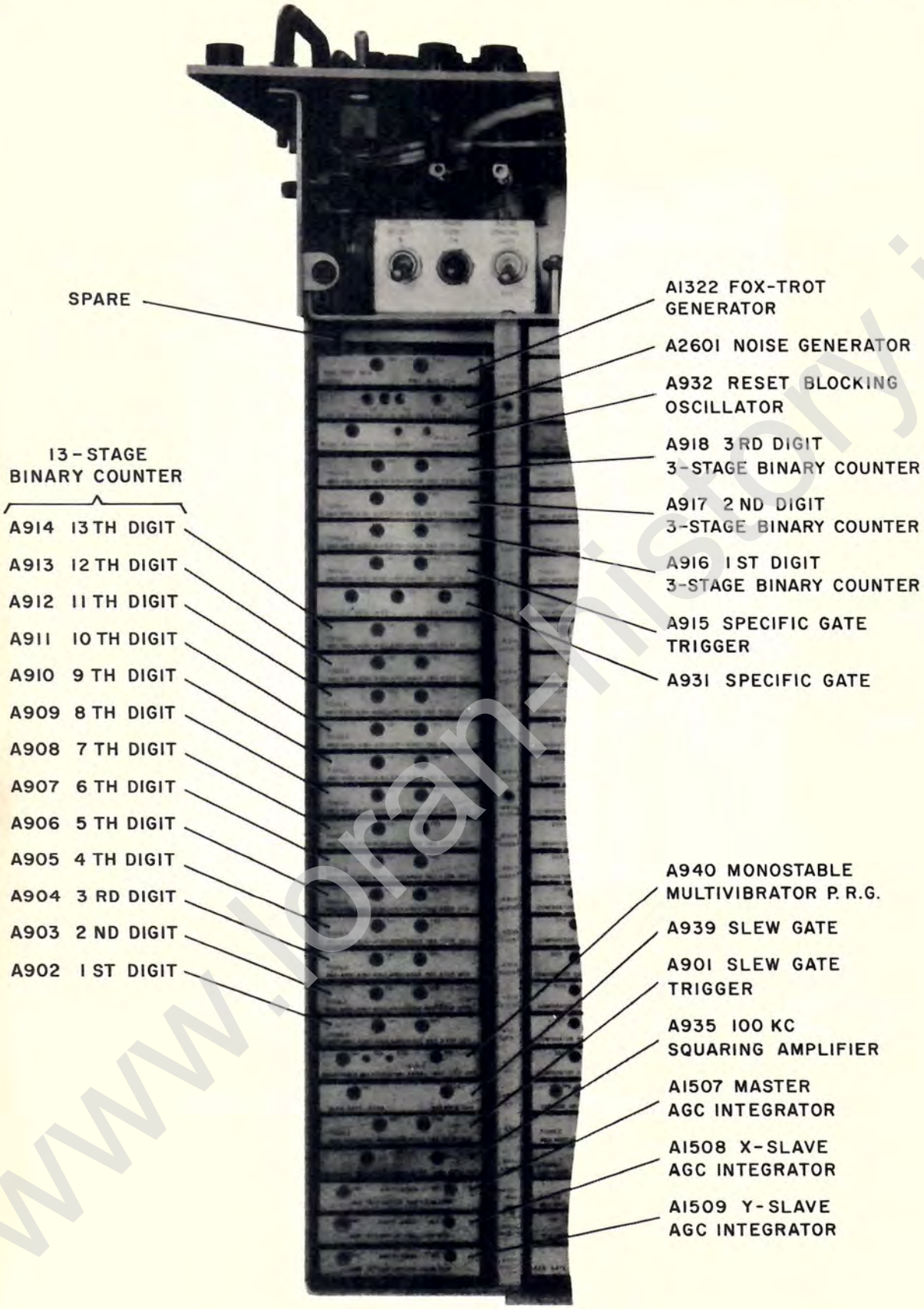


Figure 3-11. Loran Receiver R-963/SPN-30, Bottom Drawer, First Channel, Module Location

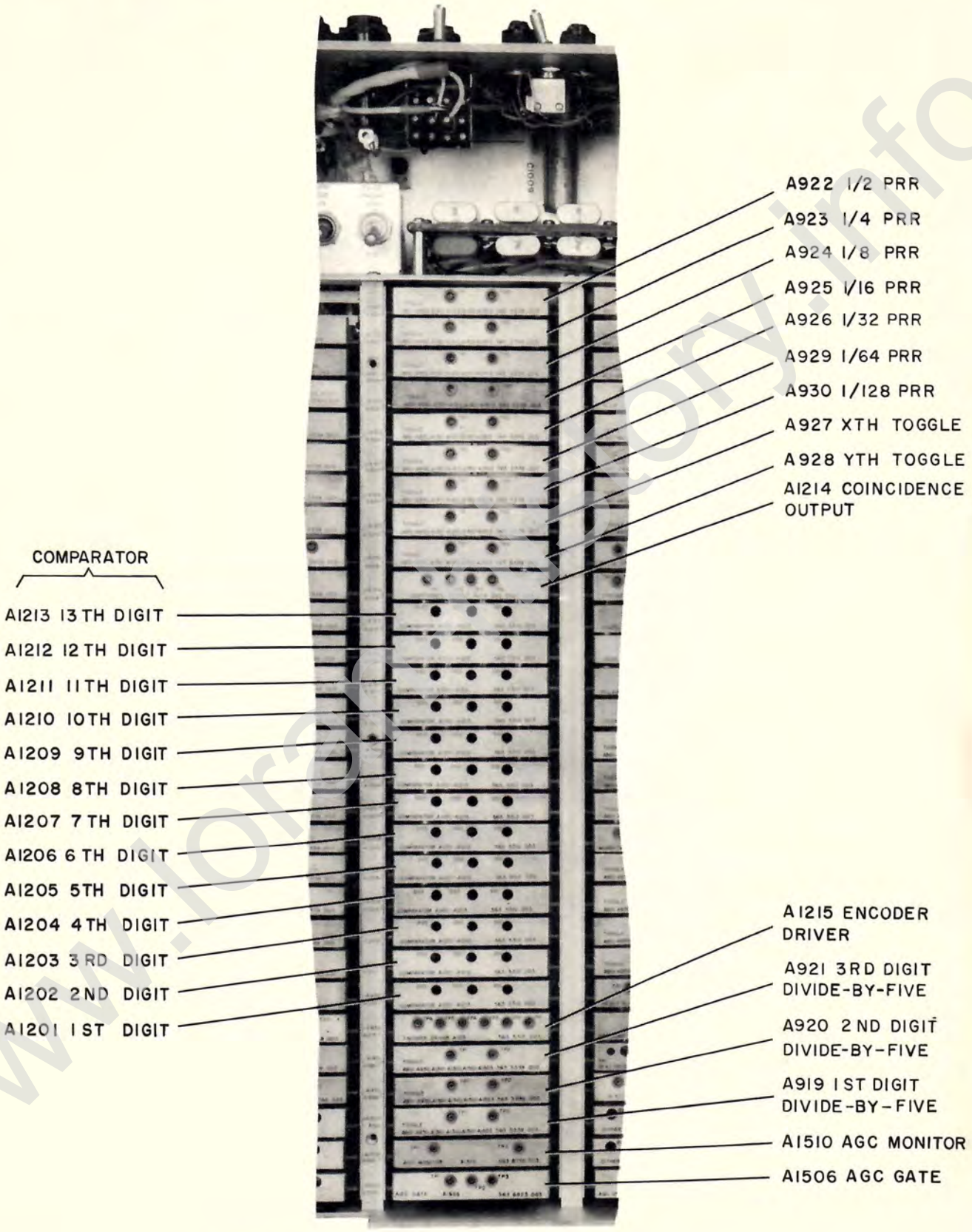


Figure 3-12. Loran Receiver R-963/SPN-30, Bottom Drawer, Second Channel, Module Location

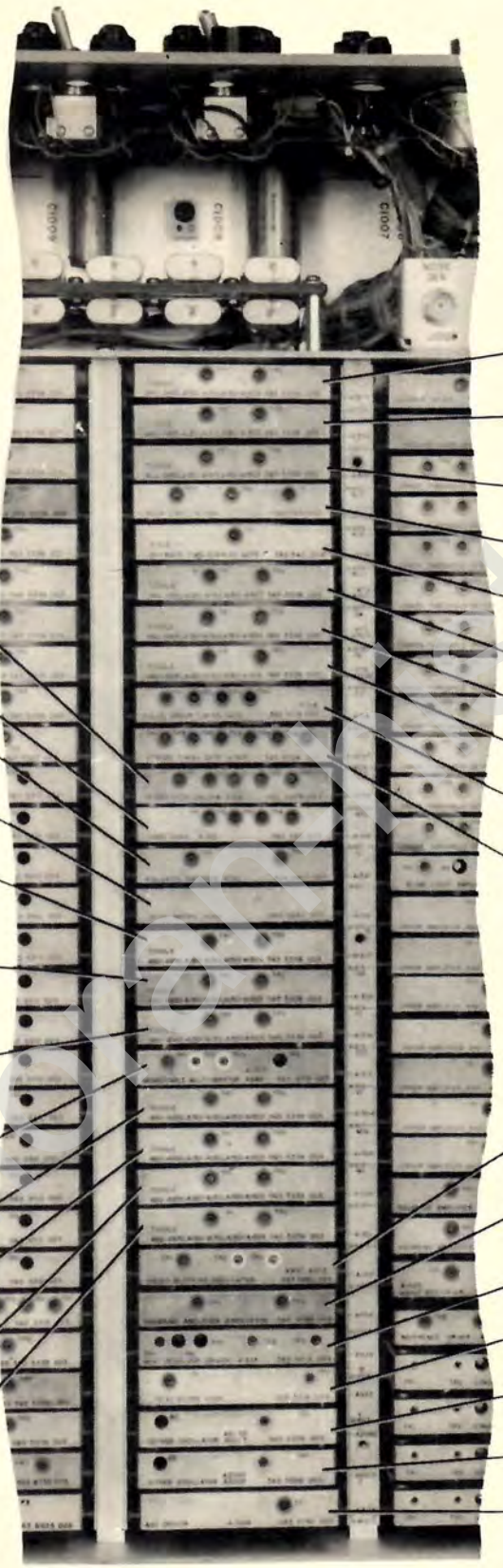


Figure 3-13. Loran Receiver R-963/SPN-30, Bottom Drawer, Third Channel, Module Location

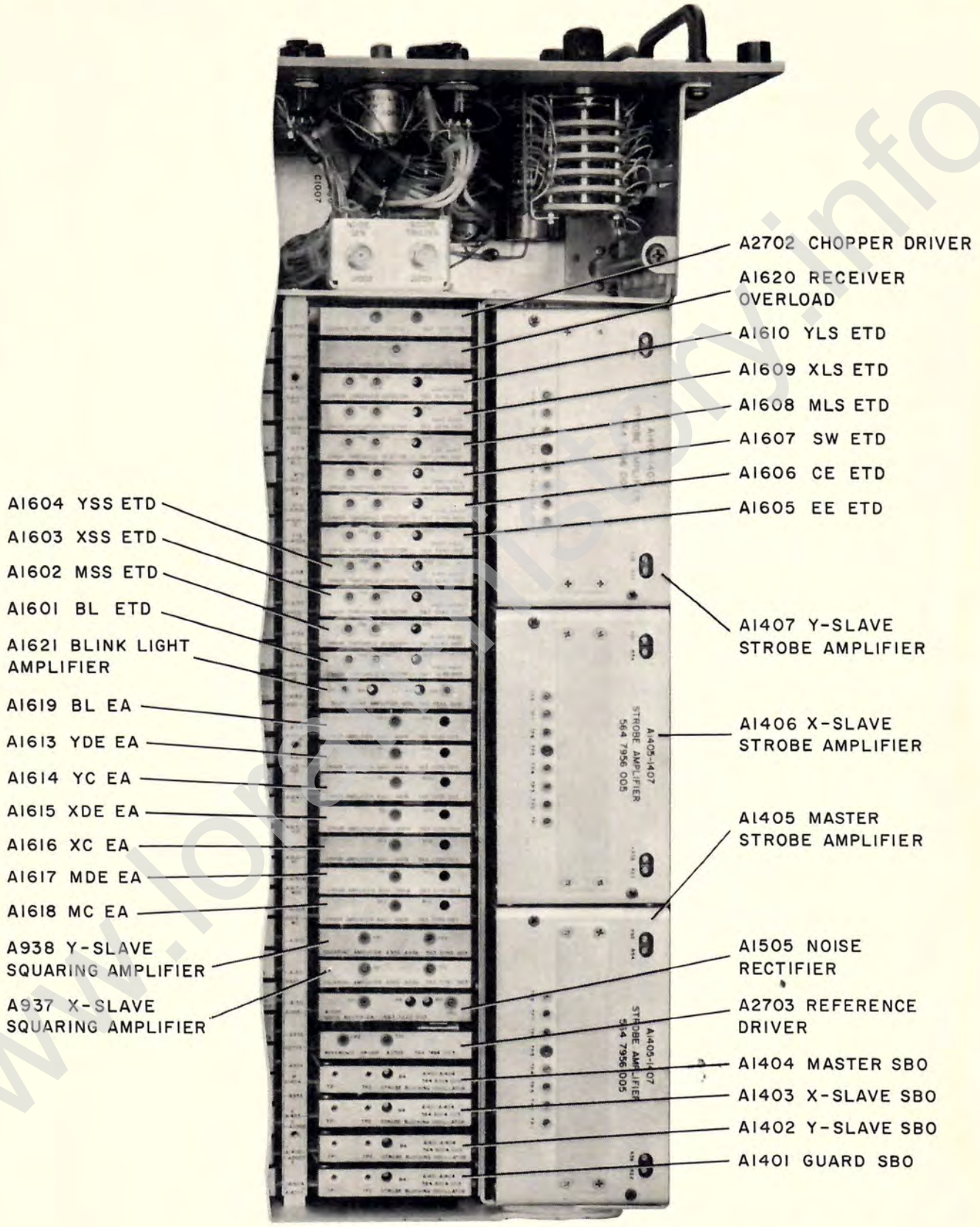


Figure 3-14. Loran Receiver R-963/SPN-30, Bottom Drawer, Fourth and Fifth Channels, Module Location

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont)

TABLE OF CONTENTS (Cont)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont)

LIST OF ILLUSTRATIONS (Cont)

LIST OF TABLES

SECTION 4
PRINCIPLES OF OPERATION

4-1. GENERAL DESCRIPTION OF LORAN-C SYSTEM OF OPERATION.

Loran-C is a precision, long-range, hyperbolic navigational system employing automatic envelope and r-f cycle comparison techniques. It operates in the frequency band of 90 to 110 kc with a carrier frequency of 100 kc. Loran-C utilizes group pulsing; eight pulses per group at each slave station and nine pulses per group at the master station. The multi-pulse-transmission method increases the average power for the same amount of peak power if only a single pulse were transmitted. The pulses of the group are phase coded. That is, the carrier frequency-cycle phase relationship with respect to the envelope is changed from pulse to pulse in a group as prescribed by stipulated code. The use of synchronous detection and post-detector narrow banding reduces the effect of noise and interference and, in conjunction with phase coding, virtually eliminates the effect of skywave contamination. In addition, phase coding provides signal identification required for automatic search operation.

The Loran-C navigational system is dependent upon three or four transmitting stations which comprise a Loran-C station group. Each station group consists of a master station and either two or three slave stations. The master station is designated M and the slave stations are designated X, Y, and Z. Each transmitting station transmits bursts of r-f energy from omnidirectional antennas on a carrier frequency of 100 kc. The output waveform from the master station consists of eight equally spaced bursts and a ninth pulse at a slightly wider space. The first eight pulses of the master station are phase-code modulated in accordance with table 4-1.

Phase coding of the pulses in table 4-1 refers to the time reference at which the modulated cycle coding is initiated with respect to the envelope bursts. For instance, 0 indication has been arbitrarily selected to indicate that the modulating signal is increasing at the start of the burst. A 180 indication means that the modulation is 180° out-of-phase with a 0-modulation signal, or that it is decreasing at the start of the burst. All slave stations transmit the same signal code; only the delay from the master varies.

The primary purpose of phase coding is to provide a means of signal identification. Phase coding is also helpful in reducing the effects of skywave contamination and makes lock-on and tracking possible even under extremely poor signal-to-noise conditions. The ninth pulse of the master group is not used by the receiver, but is used by the transmitting stations in maintaining their proper time relationships. It is, however, an easy means of visually identifying a master group on an oscilloscope.

The sequence of operation from the transmitting stations is as follows. The burst of pulses from the master station is received by the slave stations. The first slave station, slave X, delays its transmission from the master transmission by a predetermined amount. This amount is referred to as coding delay. The second slave, slave Y, delays its transmission by a slightly longer amount. The same is true for slave Z, if there is a slave Z operating in the station group. A receiver, located at an unknown position in the geographical area of operation, receives signals from all three (or four) stations on the 100-kc frequency. The coding delays are adjusted so that there will be no interference or overlap of bursts from the three (or four) transmitting stations in the service area.

TABLE 4-1. PULSE PHASE CODE OF LORAN-C STATIONS

GROUP	1	2	3	4	5	6	7	8
Master-1	0	0	180	180	0	180	0	180
Master-2	0	180	180	0	0	0	0	0
Slave-1	0	0	0	0	0	180	180	0
Slave-2	0	180	0	180	0	0	180	180

Each station has two patterns of coded bursts that it sends alternately. For instance, the master station will first transmit a master 1 code group and then a master 2 code group. The same is true for all slave stations; a slave 1 code group followed by a slave 2 code group is sent. At a receiver that is receiving signals from a master station and three slaves, the code groups will be received in the following order: M-1, XS-1, YS-1, ZS-1, M-2, XS-2, YS-2, ZS-2.

The time difference between the pulse groups is measured by the receiver and presented as dial readings in microseconds. The dial readings, together with charts supplied with the receiver, provide a means for locating the position of the receiver. Because the receiver is measuring time differences, the grid lines on the chart are hyperbolic in nature. When measuring the time differences of the master and slave X, the receiver dial reading will locate the receiver on one set of hyperbolic lines. When operating with the master and slave Y, the receiver dial reading will locate the receiver on another set of hyperbolic lines. The intersection of these two lines marks the position of the receiver. If the Loran-C station group includes a slave Z station, an additional line can be plotted which intersects the two previously plotted lines. A small triangle will normally result. Because the plot of one line is no more accurate than the others, an average reading within the triangle is the most probable location of the receiver.

Although extreme accuracy is present in every area of normal operation for a transmitting station group, the greatest accuracy of the system is realized in an

area where the intersection of the grid lines approach a right angle. In areas where the lines approach parallelism, the accuracy of the precise intersection is decreased. The third slave station in the system, slave Z, minimizes the loss of accuracy resulting from this phenomenon.

The phase-coded multipulse system used in Loran-C operation provides a means for minimizing skywave contamination. Signals from a transmitting station may be received by detecting the ground wave or a skywave. The ground wave is the shortest path distance for the transmission but is not always the strongest. Skywave hops from the first and second ionospheric layers may be stronger than the ground-wave signal, but the skywave distance travelled is completely unpredictable. Therefore, time-delay measurement based on skywave reception is completely unreliable. The undistorted ground-wave signal, even though often smaller in magnitude, is predictable and must be used as the most accurate signal for navigation. By strobing ahead of the locked-on signal, it is possible to ascertain whether this signal is a skywave.

The various pulse repetition rates listed in table 4-2 provide a means for ascertaining the identity of the Loran-C station group with which operation is desired. Because all Loran-C stations in all station groups are operating on 100 kc, there must be some way to identify the desired station group. Each station group is assigned a pulse-repetition rate. There are 48 possible allocations of pulse-repetition rates. Each station is assigned a basic and a specific rate. The two identify the exact operating pulse-repetition rate of the station group. The basic rates differ from each other successively by either 10,000 or 20,000 microseconds. Within a basic group, the specific rates vary successively by 100 microseconds. This separation is sufficient so that the receiver will not mistake one station group for another. Pulse rates in the system vary from the slowest rate of 10 pulses per second (on SS-0) to 34.13 pulses per second for the fastest rate (on H-7).

The spacing between the bursts is ordinarily 1000 microseconds. This spacing is sufficient to allow skywave contamination to fade out between pulses. Possible interference is thereby avoided. The entire sequence of transmission for a Loran-C station (ignoring the ninth slew pulse of the master group) is shown in the diagram of figure 4-1.

The slave station pulses are interspersed so that there is no overlap of signals of slave on the master or on one another. It is the time-delay relationship of the master and slave transmission that provides the means for plotting the receiver's location.

The system has the alternate capability of operating with only 500 microseconds between pulses instead of the standard 1000 microseconds. There is a possibility that this operation may not be satisfactory because the skywave contamination will not have sufficient time to fade between pulses. If this operation is selected by the transmitter station group, the receiver operation may also be changed simply by flipping a switch on the receiver.

If the transmission stations are on single-pulse operation, the receiver will receive the first two pulses from the master station and a single pulse from each of the slave stations. The coding of the master M1 and M2 signals is the same as the first two pulses for 8-pulse operation. Under single-pulse operation, the full capabilities of Loran-C navigation are not utilized and interference will become more of a factor.

See the overall block diagram of the receiver, figure 4-2. The operation of the receiver (R-963/SPN-30) may be summarized as follows. The synthesized signal created inside the receiver is compared to the incoming composite signal from the antenna. The difference is used to activate six servo motors. These motors eliminate the error between the two signals so that eventually both signals are identical in timing. When this happens, the receiver is considered to be locked on the received signal and provides a continuous dial indication of the time difference between the master and the two slaves.

The indicator (IP-532/SPN-30) is used to monitor the lock-on procedure and troubleshoot the receiver.

4-2. RECEIVER.

a. GENERAL INFORMATION.

(1) DEFINITIONS.

(a) COUNTING TOGGLE. - The toggle is a bistable multivibrator. The counting toggle is a basic memory device building block that can, upon receipt of a triggering pulse, assume either of two stable states and remain in that state until triggered to the opposite state. In application, the counting toggle is triggered by the positive-going edge of a square wave. This means that a counting toggle is effectively a divide-by-2 device of the frequency of any square wave applied.

(b) GATE TOGGLE. - The same basic bistable multivibrator is used for a gate toggle that is used for a counting toggle. Only the external connections are different. A gate toggle receives inputs which keep it in a desired state until the occurrence of a desired event, at which time a square wave or sharply spiked pulse changes the state of the circuit.

(c) FLIP-FLOP. - The flip-flop circuits are the bistable multivibrators in the indicator that initiate the starting circuit for the sweep trace (main flip-flop) and establish two traces on the face of the oscilloscope (trace-shift flip-flop). The circuits are essentially identical in operation to the toggle circuits in the receiver.

(d) GATE CIRCUIT. - The gate circuit is a multiple-input circuit that produces a specified output only when a particular relationship exists between input signals. The two most common types of gates are the AND gates and the OR gates. The AND gate produces the desired output when all of the inputs applied are of the same desired value. The OR gate produces the desired output when any of the inputs are of the desired value.

(e) GATED WAVEFORM. - The output waveform from a gate circuit is referred to as a gated waveform. In most applications, the output from the gate is a specific voltage level; for example, -6 volts. When the desired input conditions are met, the output will change levels; for example, to 0 volt. When the inputs are no longer the desired ones, the output will again return to the original level, -6 volts.

(f) CLOCK PULSE. - The clock pulse, often abbreviated CP, is an input signal to the flip-flop or

TABLE 4-2. BINARY CODES FOR LORAN-C PULSE RATES

SPECIFIC		BASIC					
		SS	SL	SH	S	L	H
0	Microseconds Decimal Number Binary Number	100,000 5,000 1001110001000	80,000 4,000 0111110100000	60,000 3,000 0101110111000	50,000 2,500 0100111000100	40,000 2,000 0011111010000	30,000 1,500 0010111011100
1	Microseconds Decimal Number Binary Number	99,900 4,995 1001110000011	79,900 3,995 0111110011011	59,900 2,995 0101110110011	49,900 2,495 0100110111111	39,900 1,995 0011111001011	29,900 1,495 0010111010111
2	Microseconds Decimal Number Binary Number	99,800 4,990 1001101111110	79,800 3,990 0111110010110	59,800 2,990 0101110101110	49,800 2,490 0100110111010	39,800 1,990 0011111000110	29,800 1,490 0010111010010
3	Microseconds Decimal Number Binary Number	99,700 4,985 1001101111001	79,700 3,985 0111110010001	59,700 2,985 0101110101001	49,700 2,485 0100110110101	39,700 1,985 0011111000001	29,700 1,485 0010111001101
4	Microseconds Decimal Number Binary Number	99,600 4,980 1001101110100	79,600 3,980 0111110001100	59,600 2,980 0101110100100	49,600 2,480 0100110110000	39,600 1,980 0011110111100	29,600 1,480 0010111001000
5	Microseconds Decimal Number Binary Number	99,500 4,975 1001101101111	79,500 3,975 0111110000111	59,500 2,975 0101110011111	49,500 2,475 0100110101011	39,500 1,975 0011110110111	29,500 1,475 0010111000011
6	Microseconds Decimal Number Binary Number	99,400 4,970 1001101101010	79,400 3,970 0111110000010	59,400 2,970 0101110011010	49,400 2,470 0100110100110	39,400 1,970 0011110110010	29,400 1,470 0010110111110
7	Microseconds Decimal Number Binary Number	99,300 4,965 1001101100101	79,300 3,965 0111101111101	59,300 2,965 0101110010101	49,300 2,465 0100110100001	39,300 1,965 0011110101101	29,300 1,465 0010110111001

Note: One pulse period equals 20 microseconds

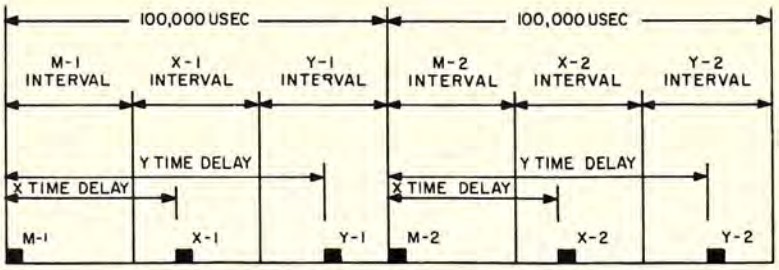


Figure 4-1. Time Sequence Diagram of Pulses from Loran-C Stations

toggle circuit that causes the circuit to change state, regardless of its previous condition. In other words, it is a pulse, which when applied to both sides of the circuit, causes the conducting transistor to cutoff and the nonconducting transistor to conduct. In a few instances, the clock pulse is connected to only one side of the circuit, rather than both. It is then only a regular reset pulse. The inverted clock pulse ($\overline{CP}$) is the complementary signal that is applied to the opposite side of the circuit from the CP signal.

(g) Q AND $\overline{Q}$. - The bistable multivibrator has two outputs, one from the collector of each transistor. The Q output is taken from the collector of Q2 and the $\overline{Q}$ output is taken from the collector of Q1. Therefore, the two outputs are complementary, or one is the inverted output of the other. The bar symbol throughout this instruction book indicates that the signal so represented is the complement, or the inverse, of the signal without the bar.

(h) MT, XT, YT. - These symbols represent the master trigger, X-slave trigger, and Y-slave trigger. The triggers are sharply spiked, positive-going pulses from a normal -6-volt level. They occur at the start of the respective group of pulses for the master signal, the X-slave signal, and the Y-slave signal, respectively.

(i) MTS, XTS, YTS. - These symbols represent the time-shared, gated waveforms for the respective intervals, master, X-slave, and Y-slave. For instance, during the duration of the master signal, the MTS waveform is at a -6-volt level. At any other time, it is at a 0-volt level.

(j) M1, M2, S1, S2. - These symbols represent the logic timing-gate waveforms from which the phase coding information is produced. During the interval of the first group of master pulses, the M1 waveform is -6 volts. At all other times, the M1 level is 0 volt. During the interval of both the X-slave and Y-slave first group of pulses, the S1 level is -6 volts. At other times the level is 0 volt. Similarly, the M2 waveform occurs during the second group of master pulses and the S2 waveform occurs during the second group of X-slave pulses and the Y-slave pulses.

(k) MXY TS, $\overline{MXY}$ TS. - These symbols represent the complementary outputs from the phase code driver (A1316) that reduce the MTS, XTS, and YTS signals to a common time base. The inverted, or $\overline{MXY}$ TS, signal is the one used in the receiver operation.

(l) PHASE CODE, $\overline{PHASE\ CODE}$. - These outputs from the phase code driver (A1316) are the phase-coded signals from the diode matrix (A1314) reduced to a common time base.

(m) MC, XC, YC. - These signals are the error voltages that drive the servo motors in the master, X-slave, and Y-slave cycle loops. When phase lock has been achieved, these voltages are reduced to 0 volt.

(n) ME, XE, YE. - These signals are the error voltages that drive the servo motors in the master, X-slave, and Y-slave envelope loops. When envelope lock has been achieved, the envelope error will be reduced to 0 volt.

(o) MST, XST, YST. - These signals are the master, X-slave, and Y-slave strobe trigger outputs from the strobe timing gate (A1317) to the strobe blocking oscillators (A1402 through A1404).

(p) MGST, XGST, YGST. - These signals are the master, X-slave, and Y-slave guard strobe trigger outputs from the strobe timing gate to the guard strobe blocking oscillator (A1401).

(q) MSBO, XSBO, YSBO, GSBO. - These are the master, X-slave, Y-slave, and guard strobe blocking oscillator output signals applied to the strobe circuits in the detector-strobe module (A401).

(r) MSS, XSS, YSS. - These are the names for the slew stop error threshold detectors that receive both the outputs from the cycle and derived envelope error amplifiers. When lock-on has been achieved, the error threshold detector will sense this and slew will stop.

(s) IMT, IXT, IYT. - These are the triggers for the indicator circuits. The triggers occur in time coincidence with the guard strobe triggers, or slightly ahead of the occurrence of their respective pulses. This allows viewing of the entire pulse shape on the face of the oscilloscope.

(t) XTH, YTH TOGGLES. - These toggles are only used when the SEARCH SELECTOR CONTROL is placed in the M MULT position. In this case, when the received r-f master signal comes into the X-slave or Y-slave interval, the XTH, or YTH, toggle causes a trigger hop so that the master r-f signal and internally generated signal will be in the same interval and lock-on can be rapidly accomplished.

(u) M AGC D. - This signal is the master automatic gain-control delay signal that prevents the agc level for the master signal from changing levels until the ninth pulse has been received.

(v) YMG, MXG, XYG. - These signals and their inverted complements are applied to the agc gate (A1506) to permit the agc level for each group of pulses to be established in accordance with the strength of the pulses being received.

(2) BINARY NUMBER SYSTEM. - The use of binary numbers in electronic equipment greatly simplifies its design since simple on-off devices such as switches or flip-flop multivibrators can be used. Since the decimal system is based upon powers of 10, the decimal number 5000 might be expressed as follows:

$5 \times 10^3 = 5000$ (thousands)
$0 \times 10^2 = 000$ (hundreds)
$0 \times 10^1 = 00$ (tens)
$0 \times 10^0 = 0$ (units)
5000

Decimal numbers used in electronic circuits are cumbersome, since 10 discrete circuits are required for each decimal place. Consequently, the electronic computer capable of handling decimal numbers up to 5000 would require a total of 35 discrete circuits (5 thousands, 10 hundreds, 10 tens, and 10 units).

The binary system is a simpler system to use in electronic computers since all binary numbers are based on powers of 2. By using powers of 2, the circuits involved are either ON or OFF to produce information. When writing numbers in binary form, it is a common practice to indicate ON functions with the figure 1 and OFF functions with the figure 0. When expressed in written form, the binary number 13 would be 1101. For example, the binary number can be expressed, in powers of 2, as the following:

$1 \times 2^3 = 8$ (eights digit) - on
$1 \times 2^2 = 4$ (fours digit) - on
$0 \times 2^1 = 0$ (twos digit) - off
$1 \times 2^0 = 1$ (ones digit) - on
13

In order to construct an electronic computer circuit capable of handling binary numbers up to 5000, only 13 discrete circuits are required. However, a 13-stage binary counter is actually capable of counting, in binary sequence, up to 8192.

Table 4-3 lists binary equivalents of decimal numbers up to 15. A binary counter which will handle numbers of this magnitude is made up of 4 circuits (flip-flop multivibrators).

A decimal number may be converted to its binary equivalent by successive divisions of 2. For example, the decimal number 13 is converted to its binary equivalent as follows:

	0		
2)	1	1	2 into 1 - 0 times - 1 left over
2)	3	1	2 into 3 - 1 time - 1 left over
2)	6	0	2 into 6 - 3 times - 0 left over
start - 2)	13	1	2 into 13 - 6 times - 1 left over

Initially the decimal number is divided by 2, and the remainder noted for each step. The remainders will be the binary equivalent starting with the last division. Therefore, the binary equivalent starting at 13 is 1101 as shown in the paragraph above. The conversion of the decimal number 5000 to its binary equivalent is as follows:

TABLE 4-3. BINARY EQUIVALENTS OF DECIMAL NUMBERS

DECIMAL	BINARY EQUIVALENT			
	$(8)=2^3$	$(4)=2^2$	$(2)=2^1$	$(1)=2^0$
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

	0	
2)	1	1
2)	2	0
2)	4	0
2)	9	1
2)	19	1
2)	39	1
2)	78	0
2)	156	0
2)	312	0
2)	625	1
2)	1250	0
2)	2500	0
2)	5000	0

Answer: 1001110001000

From the discussion above it is shown that the binary system represents the various powers of 2 in this sequence, from left to right:

$4096 = 2^{12}$, $2048 = 2^{11}$, $1024 = 2^{10}$, $512 = 2^9$, $256 = 2^8$, $128 = 2^7$, $64 = 2^6$, $32 = 2^5$, $16 = 2^4$, $8 = 2^3$, $4 = 2^2$, $2 = 2^1$, $1 = 2^0$

Therefore, a binary number may be converted to its decimal equivalent by counting powers of 2 from right to left starting with 2^0, the least significant digit. Wherever a 1 occurs in the binary number the power of two at this point is added to the total which will be the decimal number. For example, the binary number 1101 has three powers of 2, namely 2^0, 2^2, and 2^3. Consequently, the binary number 1101 may be expressed as:

1101 (binary) = 1 + 4 + 8 = 13 (decimal)

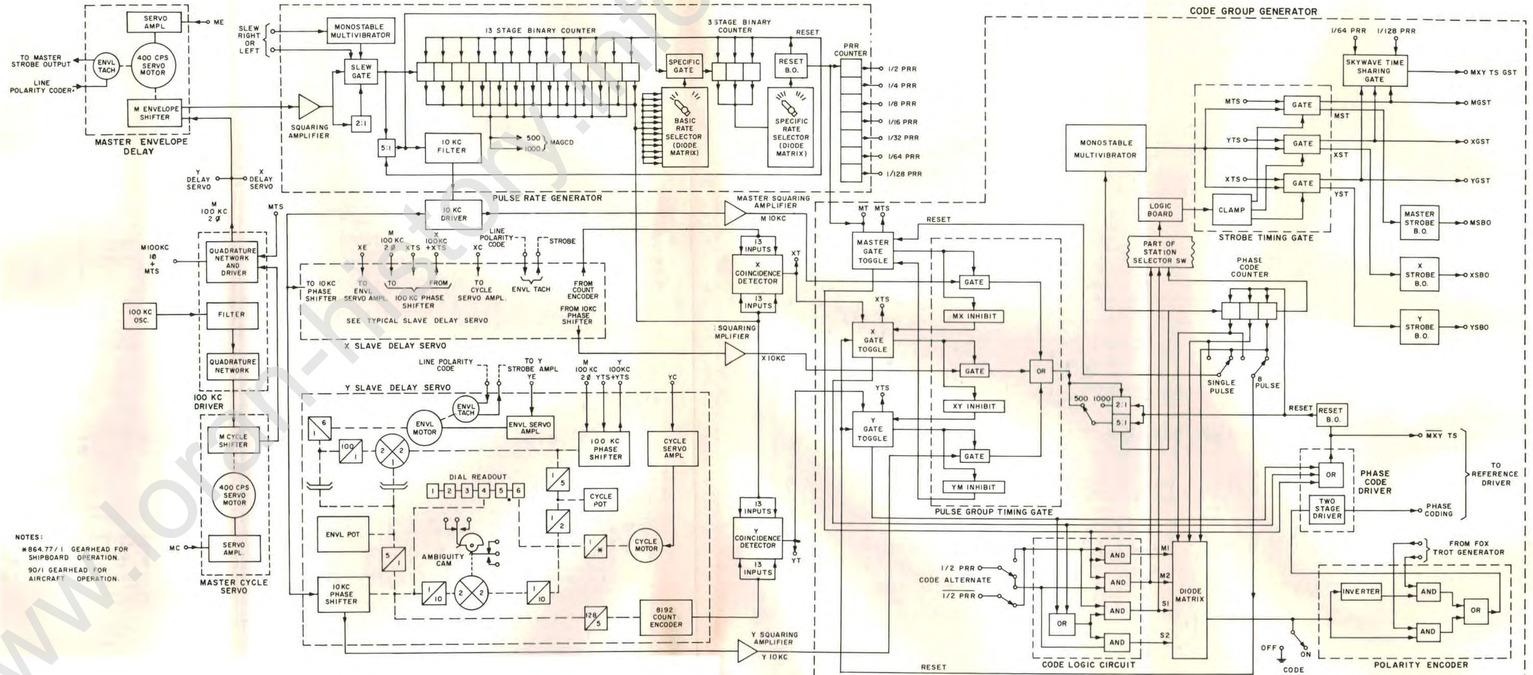


Figure 4-2. Loran Receiver R-963/SPN-30, Overall Block Diagram (Sheet 1)

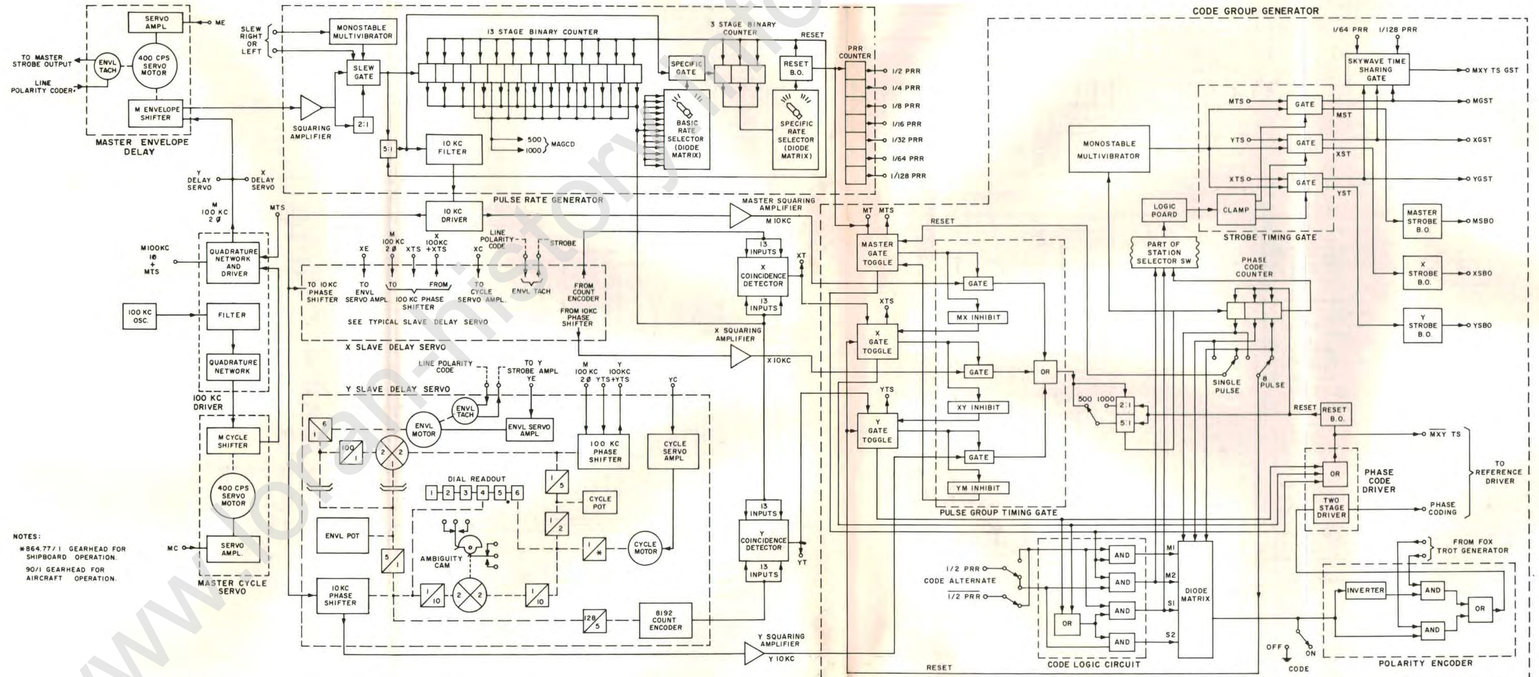


Figure 4-2. Loran Receiver R-963/SPN-30, Overall Block Diagram (Sheet 1)

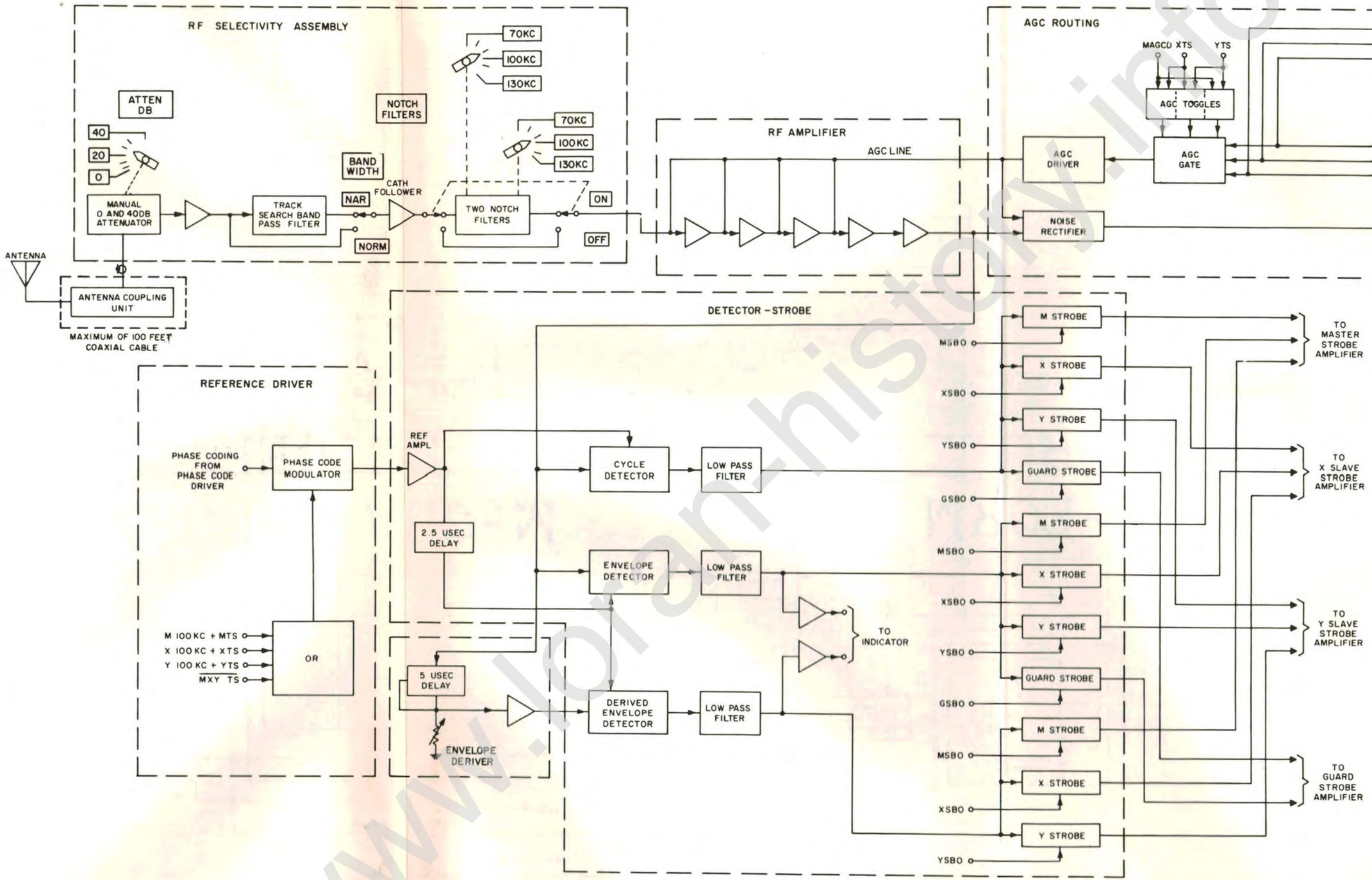


Figure 4-2. Loran Receiver R-963/SPN-30, Overall Block Diagram (Sheet 2)

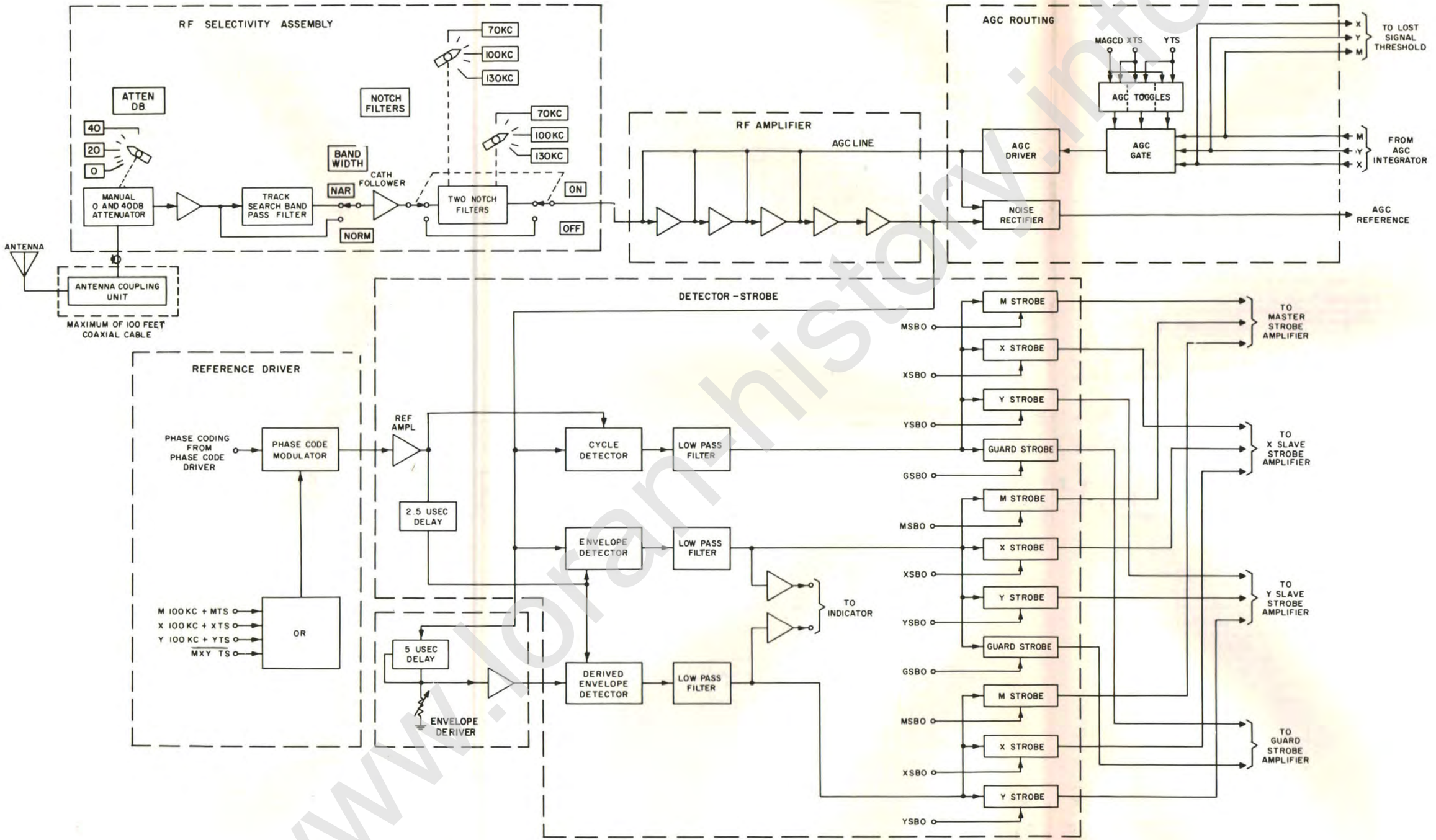


Figure 4-2. Loran Receiver R-963/SPN-30, Overall Block Diagram (Sheet 2)

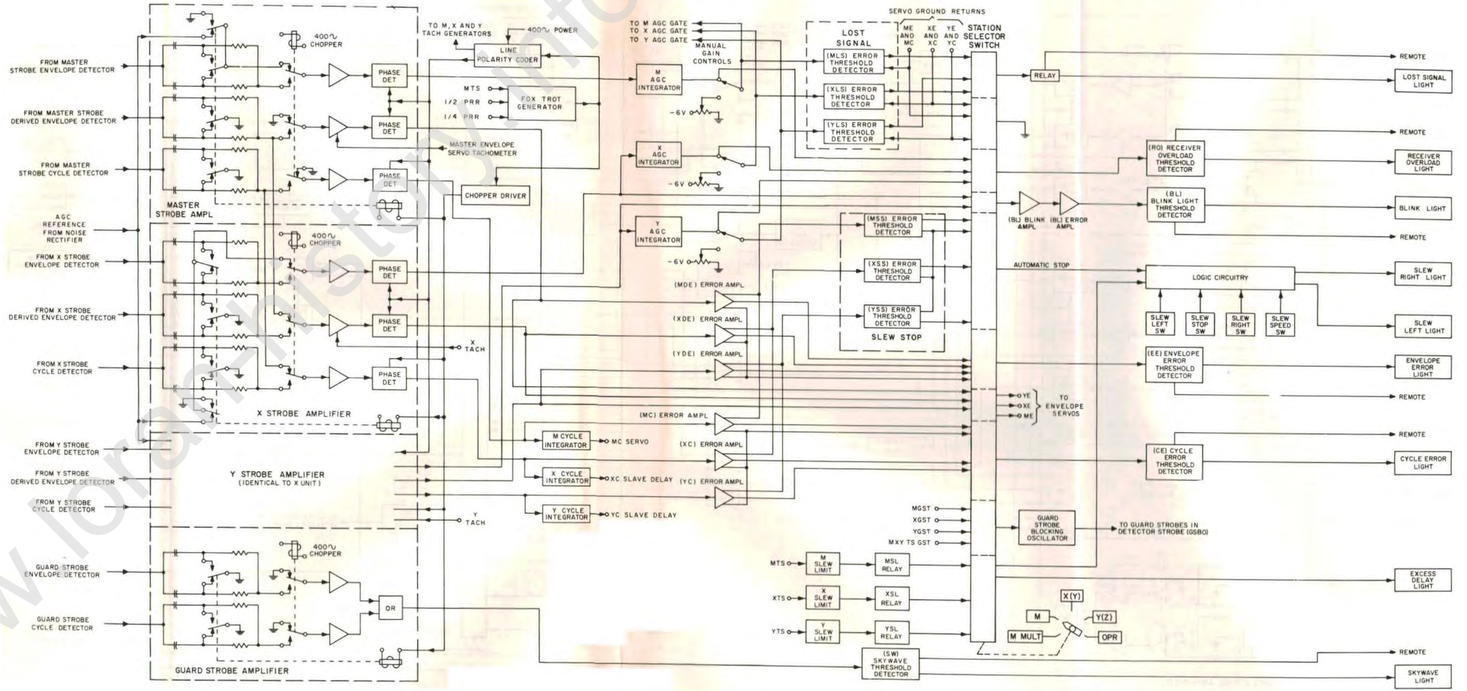


Figure 4-2. Loran Receiver R-963/SPN-30, Overall Block Diagram (Sheet 3)

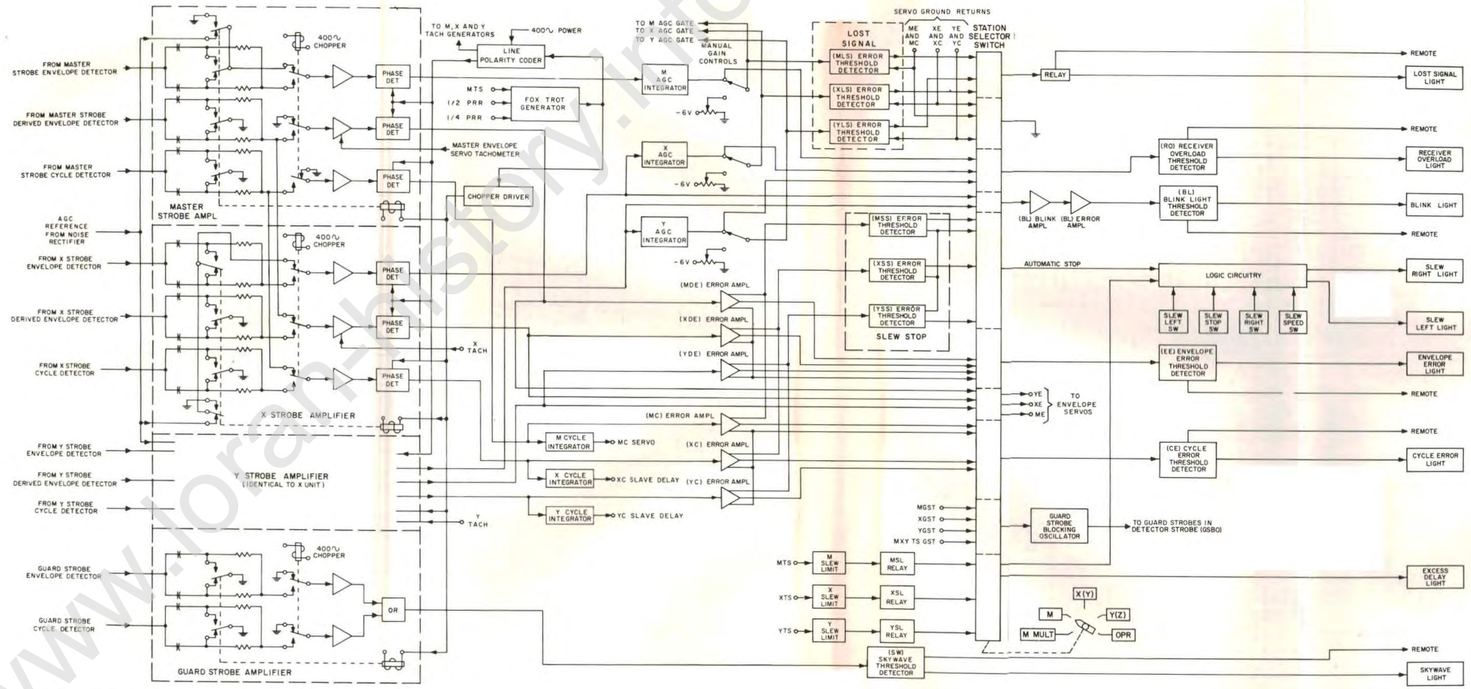


Figure 4-2. Loran Receiver R-963/SPN-30, Overall Block Diagram (Sheet 3)

(3) BINARY COUNTERS. - In this receiver, a binary counter is considered as a decimal-to-binary converter. An input of a fixed frequency or pulse duration is applied to the counter, which converts the input pulses, one by one, into binary information.

The binary counters in the Loran-C receiver are made up of standard toggle (flip-flop) circuit boards as described in paragraph 4-2*d*(1). With the three toggle boards connected as shown in figure 4-3, only a positive-going input to a toggle circuit will cause it to change state. The triggering pulse for a toggle circuit is applied to the base of the nonconducting transistor. This transistor is commonly referred to as being OFF and the conducting transistor is referred to as being ON. When the OFF transistor is turned ON, the circuit will change state and cause the previously ON transistor to turn OFF. There are several possible input triggers to a toggle circuit that are connected through an OR gate. One input to each transistor is labelled the clock pulse input (abbreviated CP). In almost every application in the receiver, the two CP inputs are externally connected. This ensures that whenever a positive pulse occurs, it will be applied to the OFF transistor regardless of which one this may be and the circuit will change state. In some applications, the clock pulses are not tied together. A positive pulse applied to an ON transistor will not change the state of the toggle.

The reset blocking oscillator shown in figure 4-3 causes all three of the toggle boards to return to the state in which the Q1, Q2, and Q3 outputs are all at a 0-volt level and the $\bar{Q}1$, $\bar{Q}2$, and $\bar{Q}3$ outputs are all at a -6-volt level. The reset blocking oscillator is actuated when the $\bar{Q}3$ output goes in a positive direction. The first positive-going input pulse will cause the counter to begin its counting sequence from the zero condition and will continue through seven counts before it resets again. The relative time sequence of input-to-output waveforms is shown in figure 4-4.

An examination of the table of decimal-to-binary equivalents (table 4-3) will disclose that the binary equivalents of numbers are represented by 0 and 1 in a specific sequence for each number. The binary equivalent of the decimal number 0 for a 3-stage counter is expressed as 000. The binary equivalent of the decimal number 3 is expressed as 011, and so on. It should also be noted that the outputs of the 3-stage binary counter (Q3, Q2, and Q1) are either 0 volt or -6 volts as shown in figure 4-4. Now, the binary equivalents in the table should be compared with the outputs of the binary counter for the decimal number 0. The table indicates the number 0 to be 000, and the outputs of the binary counter at 0 are shown to be 000 (Q3=0, Q2=0, Q1=0). The table indicates the binary equivalent of the number 3 to be 011, and the outputs of the counter during pulse 3 are 011 (Q3=0, Q2= -6, Q1= -6). It may be seen from this illustration that the 3-stage counter produces decimal-to-binary conversion.

The highest number that a binary counter will produce depends on the number of toggle boards used. The Loran-C receiver includes two 3-stage counters, one 5-stage counter, and one 13-stage counter.

(4) AND GATES. - The basic AND circuit may be considered as a type of gating device which receives

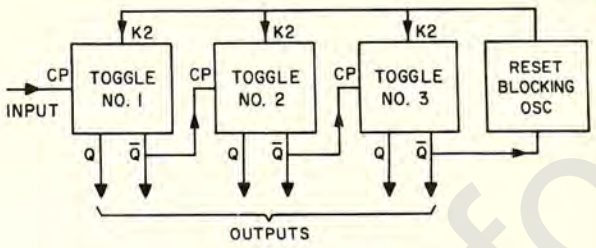


Figure 4-3. Three-Stage Binary Counter, Block Diagram

information from two or more sources and supplies an output when all of the specified input requirements are met. The output from an AND circuit contains components of the input signals applied. The AND circuits most commonly used in the Loran-C receiver combine two or more waveforms varying between levels of 0 volt, -6 volts, or +6 volts and produce an output when all of the voltages are at the same desired level.

A typical AND circuit might be used to sense the overlap of two gate signals. The input and output relationships of an AND circuit of this nature are shown in figure 4-5. The AND circuit which will produce this result might be constructed in the manner shown in figure 4-6.

When input 1 is at 0 volt, CR1 will conduct and clamp the output line to a level of 0 volt. When input 2 is at 0 volt, CR2 will conduct and clamp the output line to a level of 0 volt. However, when both input 1 and input 2 are at -6 volts, the diodes are cut off, there is no voltage drop across R1, and the output line is released to a level of -6 volts. It can be seen that -6 volts must be present at inputs 1 and 2 at the same time in order for the circuit to produce an output signal of -6 volts.

(5) DIODE MATRIX. - A diode matrix is an application of the basic AND circuit. The diode matrix in the Loran-C receiver is used to produce an output when a specified binary number is applied to its input. The diode matrix shown in figure 4-7 senses the binary outputs of the counter during time 0 and time 3, with respect to the input pulses at the counter. The output signal during these times will be a square pulse of -6 volts.

In the discussion of the AND circuit, it was shown that all inputs to the AND diodes must be at -6 volts in order to release the output line to -6 volts. The binary number for 0 is 000. Selecting -6 volts for logic 0 and 0 volt for logic 1, it is apparent from the waveforms that the Q outputs represent logic 1 and the $\bar{Q}$ outputs represent logic 0. Counter outputs Q3, $\bar{Q}2$, and $\bar{Q}1$ must be applied through diodes CR1, CR2, and CR3 (the AND circuit) to the matrix line in order to release it to the desired output of -6 volts at time 0. Therefore an output on the matrix line is produced for time 0 when the switch in figure 4-7 is in the left-hand position.

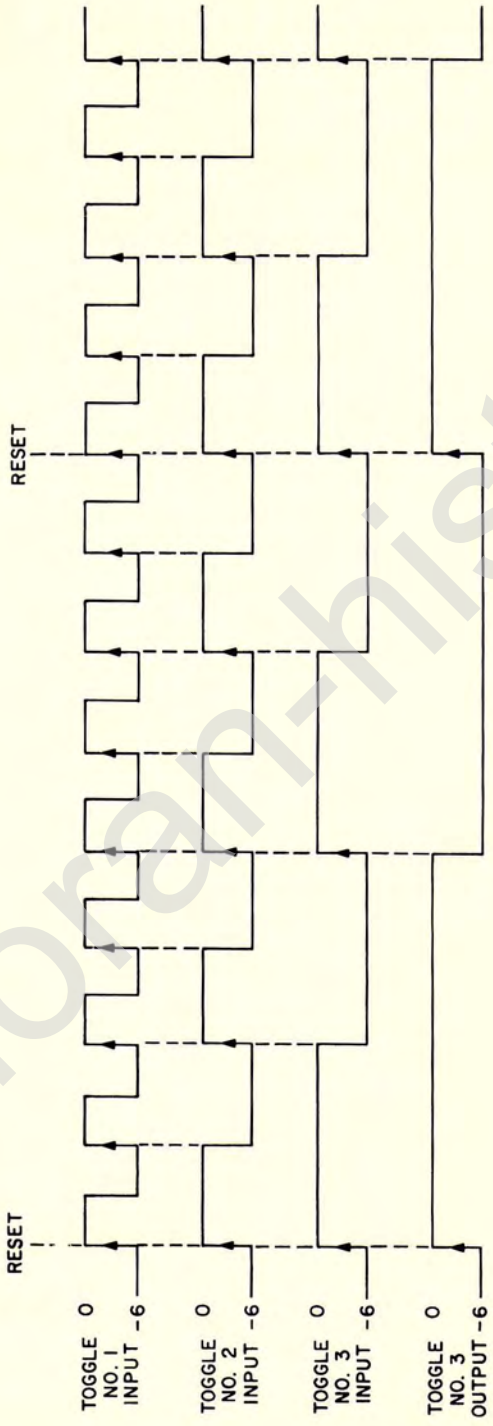


Figure 4-4. Three-Stage Binary Counter, Waveshapes

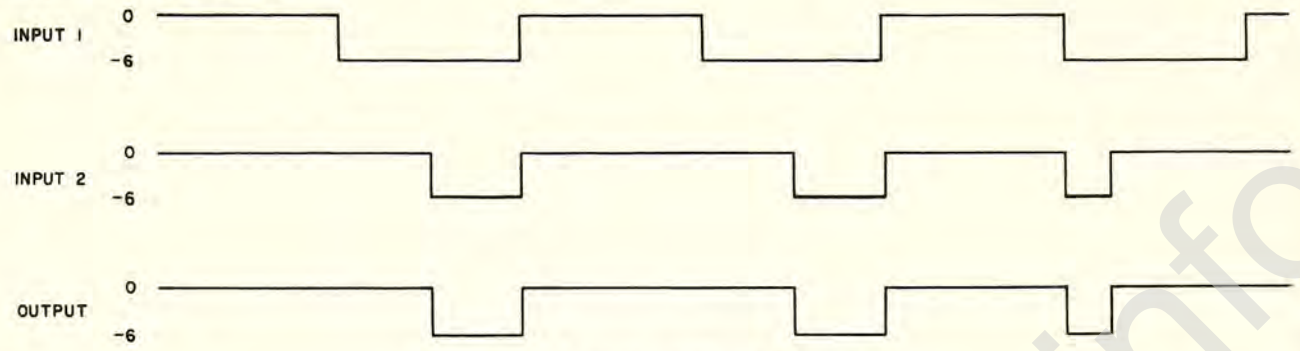


Figure 4-5. Typical and Circuit Waveshapes

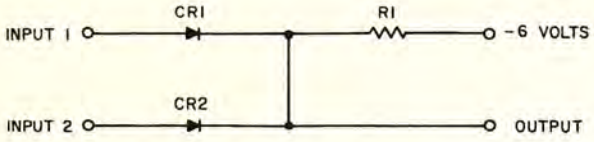


Figure 4-6. Typical AND Circuit, Simplified Schematic Diagram

The diode matrix will produce an output of -6 volts for time 3 when the switch is placed in the right-hand position. The binary equivalent for 3 is 011. During the third count, Q3=0, Q2= -6, and Q1 = -6. By selecting the complementary output of Q3, which is $\overline{Q3}$, all of the voltages from the matrix will be -6 volts and a -6-volt output will be produced. At all other times prior to reset at least one of the applied voltages will be 0 volt. If any one of the applied inputs to the matrix line is 0 volt, then the output will be clamped at 0 volt. All of the voltages must be -6 volts before an output of -6 volts can be produced.

The type of diode matrix shown in figure 4-8 is called a trunked matrix. A single output line is used and the diodes are switched between the outputs of the counter stages as needed to sense the counter output at the desired binary time. The trunked matrix is used to sense the outputs of the 13-stage basic pulse-repetition rate counter and the 3-stage specific pulse-repetition rate counter to be discussed later.

The other type of diode matrix used in the Loran-C receiver has a separate output line for each binary combination to be gated. Figure 4-8 shows a diode matrix of this design which will gate all odd-numbered combinations (1, 3, 5, 7) from the 3-stage counter.

b. R-F SECTION. - The major units of the r-f section of the Loran-C navigational receiver are the 30-foot whip antenna, the antenna coupler, the r-f selectivity unit, and the r-f amplifier. The r-f selectivity unit is further divided into a 20- or 40-db attenuator pad, a variable bandpass circuit, and two independent, tunable notch filters. The r-f amplifier is capable of 120-db amplification. Front panel controls associated wih the r-f section include ATTEN 0-20-40 DB switch, BAND WIDTH NORM-NAR switch, NOTCH FILTERS OFF-ON switch, and notch filter tuning. Sensitivity range of the system is from 5 microvolts to 5 volts, including the use of the 40-db pad. The amplifier portion delivers up to 20 volts rms into a 600-ohm load. Outputs from the r-f section are used in the detector, the envelope deriver, and the indicator circuits.

(1) ANTENNA COUPLER CU-793/SPN-30 (A4001). - Antenna Coupler CU-793/SPN-30 is an impedance-matching device from the 30-foot antenna to the receiver to allow a 30-db stepup from the antenna to the output of the r-f selectivity unit for a 100-kc signal. (See the schematic diagram shown in figure 6-182.) The typical antenna characteristics for a 30-foot whip antenna are 0.01-ohm resistance and 120-micromicrofarad capacitance. The tuning capacitor (C4001) in the primary of transformer T4001 parallel-resonates the antenna. Since the antenna itself closely simulates a capacitor, together with C4001 and the primary coil of T4001, there is a slight stepup applied to T4001. The secondary impedance of T4001 is 325 ohms. The first section of the filter in the secondary (L4001 and C4002) approximately matches the secondary impedance and provides a bandwidth of about 20 kc. Resistor R4001 lowers the impedance of the matched section.

The remainder of the circuit is an M-derived, low-pass filter that provides the circuit with an output impedance of 50 ohms. This matches the input to the r-f selectivity unit. The total gain for the entire section from the antenna, through the filter, and through the selectivity unit is about 30 db.

For protection from the elements, the antenna coupler is sealed in a weather-proof container. There is a horn-gap protector in the input to protect the unit from lightning bursts.

(2) R-F SELECTIVITY MODULE (A201).

(a) GENERAL. - The r-f selectivity module contains circuitry which includes an attenuator which provides either 20 db or 40 db of attenuation, bandpass switching, and two tunable notch filters. This unit functions as a fixed-frequency preselector between the antenna coupler and the r-f amplifier module. Front panel operator controls on this module

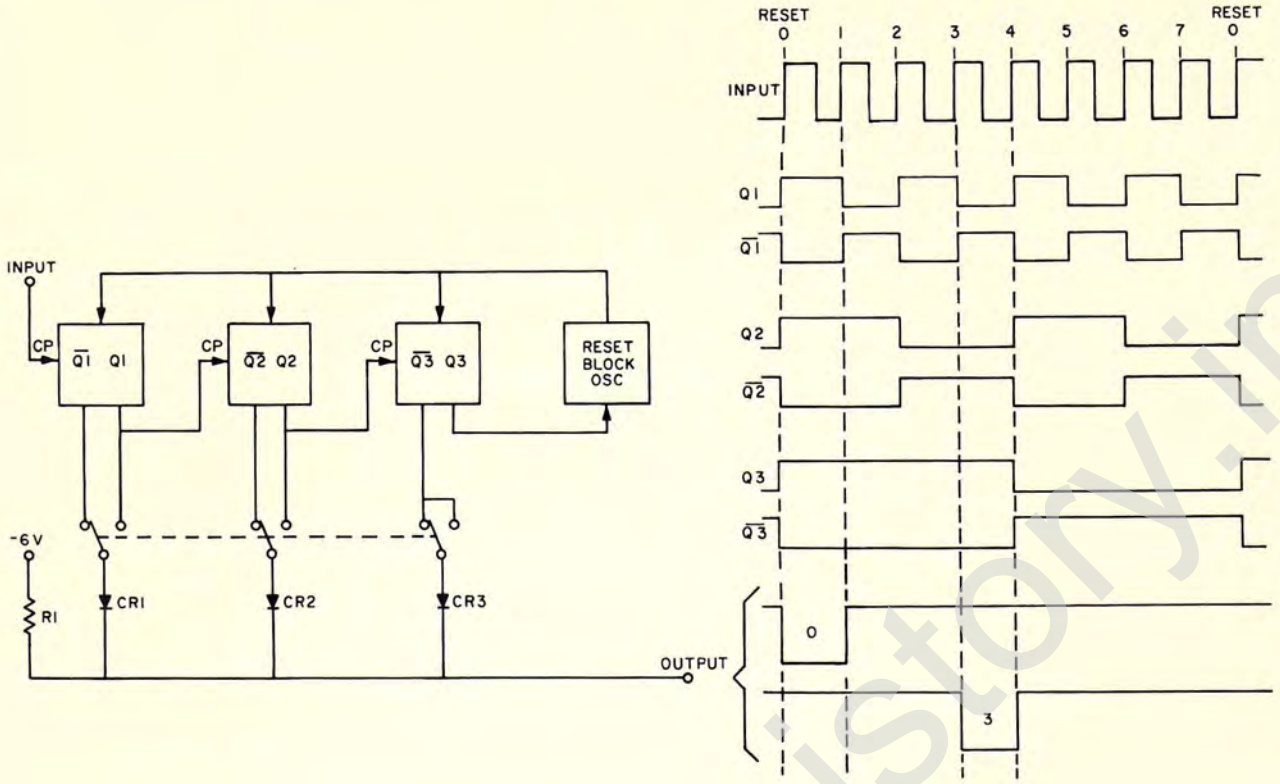


Figure 4-7. Counter Detecting Zero and Three

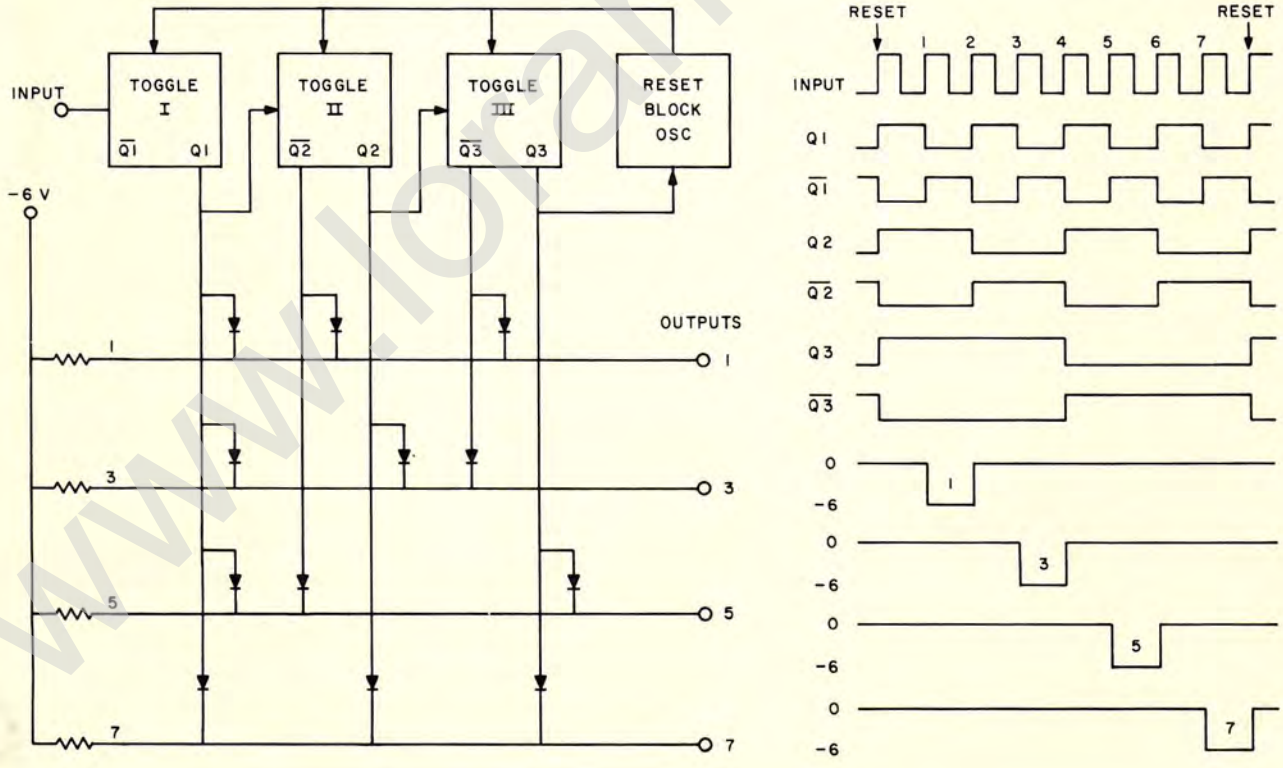


Figure 4-8. Four-Line Diode Matrix, Block Diagram

include an ATTEN 0-20-40-db switch, a BAND WIDTH NORM-NAR switch, a NOTCH FILTERS OFF-ON switch, and tuning controls for the two notch filters. The bandpass under normal conditions is 20 kc at the 6-db points on the selectivity curve. See figure 4-9. In the narrow position, the bandpass is approximately 6 kc at the 6-db points. Each of the notch filters is independently tunable from 70 to 130 kilocycles.

(b) ATTEN. - The ATTEN (attenuator) pad may be switched into the circuit to prevent receiver overloading when the Loran-C system is used in proximity to a transmitting station. The pad is basically two 20-db T-pads in series and has input and output impedances of approximately 50 ohms. Switch S201 allows selection of 0 db, 20 db, or 40 db of attenuation.

(c) BANDPASS SWITCHING. - The tuned circuits that accomplish the bandpass switching are associated with the plate circuit of vacuum tube V201A. (See figure 6-122). Assuming the 40-db pad is switched out, the input signal couples directly from input jack J201 to the primary of transformer T201. This transformer provides both impedance matching and voltage gain, resulting in optimum transfer of the desired 100-kc signal to the grid of V201B. The resistance of R206 establishes a 50-ohm input impedance at transformer T201 to match the 50-ohm characteristic impedance of the signal input coaxial cable. The secondary of T201 is tuned to 100 ±5 kc, by capacitor C201.

(d) BROADBAND OPERATION. - The output of transformer T201 drives the input of the cascode amplifier formed by V201B and V201A. This amplifier has a gain of 18 db with less than a 2° phase shift, and a dynamic range of approximately 0.5 volt with 10 mv applied. The V201B stage is a conventional amplifier except for the use of the cathode-to-plate impedance of V201A as part of the plate-load impedance. Bias for the V201B stage is obtained from cathode resistor R207.

Tube half V201A is the second stage of a cascode amplifier. The input signal at the cathode is obtained from the plate of V201B. Grid bias is obtained from the voltage divider formed by resistors R228 and R229. The V201A plate circuit, which consists of R210, L208, and C219, is tuned to the desired frequency, 100 kc. When relay K201 is deenergized (broadband operation), the plate output of V201A is coupled through capacitors C204 and C218 to the input of cathode follower V202A. The bandpass, in broadband operation, is approximately 20 kc between the 6-db points on the selectivity curve.

(e) NARROW BAND OPERATION. - Relay K201 is energized when narrow-band operation is desired. This connects the high-Q, parallel-resonant circuit consisting of L202, L203, C205, and C207 between the plate of V201A and the grid of V202A. The addition of the high-Q tank circuit narrows the bandpass

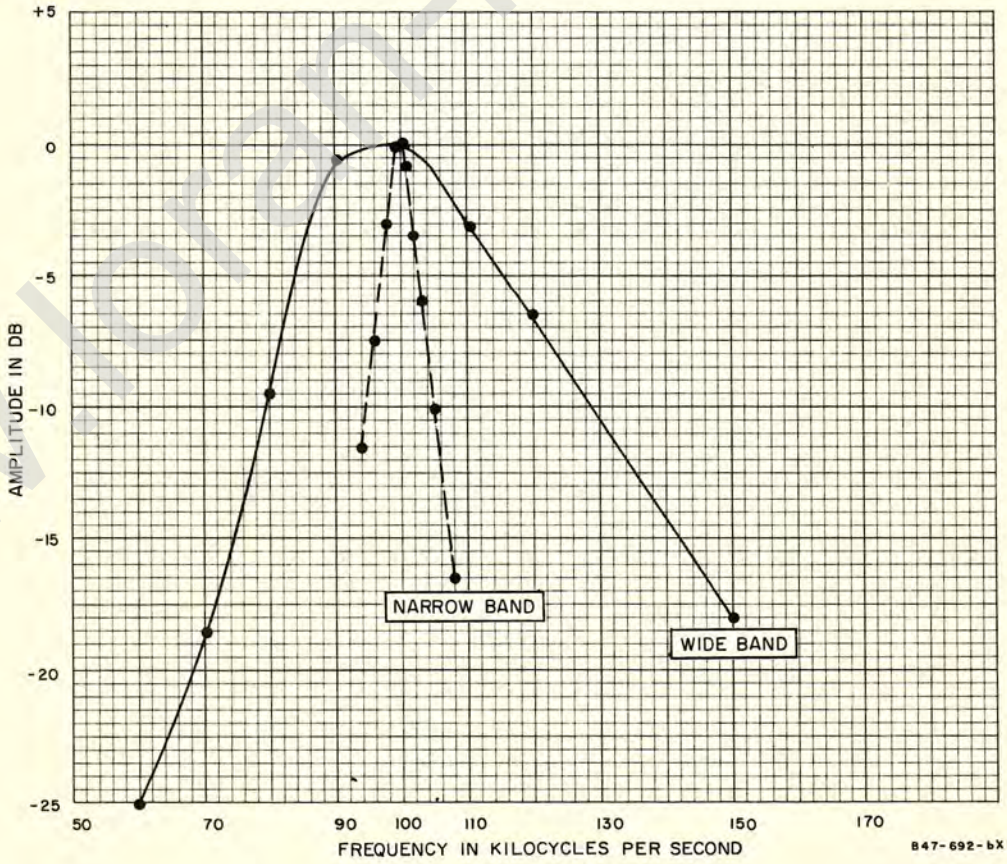


Figure 4-9. R-F Selectivity Curve

between the 6-db points to 6 kc. Inductors L202 and L203 are variable so that they can be tuned to an exact center frequency of 100 kc.

(3) NOTCH FILTERS.

(a) GENERAL. - The Loran-C receiver uses a pair of series-resonant Q-multipliers as notch filters. The basic idea of a Q-multiplier is to effectively increase the Q of a tuned circuit by applying regenerative feedback to the tuned circuit. This regenerative feedback, below the level of oscillation, can produce values of Q in the order of 2000 or more. It is possible to obtain sharp selectivity in a Q-multiplier since the selectivity of a tuned circuit is directly related to the Q. A desired frequency is peaked when parallel-tuned circuits are used. However, the result achieved with a series-tuned Q-multiplier is rejection of the desired frequency.

(b) DETAIL. - See the r-f selectivity module schematic diagram, figure 6-122, for the notch-filter circuitry. Both notch filters in the r-f selectivity module are identical. They are driven by low-impedance cathode followers V202A and V203A. Tubes V202B and V203B perform the actual filtering action. It is assumed that S203 is ON and the notch filters are active. The signal from V202A is coupled through C208 to isolation network R213-R225. The signal is applied across tuned circuit L204-L205-C212. Part of the signal is tapped off between L205 and C212 and applied to the grid of V202B. The signal at the cathode of V202B is applied in-phase to the tuned circuit of the grid of V202B through feedback loop R215-R214-C211. This constitutes positive feedback and results in Q-multiplication in the tuned circuit.

Potentiometer R225, in the isolation network, can be adjusted to control the amount of rejection, or notch depth. Potentiometer R215, in the feedback loop, can be adjusted to control the amount of Q-multiplication, or notch width. These controls are normally set to produce notch rejection characteristics as shown in figure 4-10. Capacitor C212 can be adjusted to tune the filter between 70 kc and 130 kc.

Notch filter V203A-V203B is identical in operation to the filter just discussed. Cathode follower V203A is an isolation device and driver for Q-multiplier V203B. Resistor R221 adjusts the notch depth and R223 adjusts the notch width for this filter. Capacitor C216 is the tuning control. When S203 is OFF, signals bypass the notch filters and are coupled directly through output transformer T202 to output jack J203. Regardless of the position of S203, the output is always approximately 0.5 volt rms.

(4) R-F AMPLIFIER MODULE (A301).

(a) GENERAL. - The r-f amplifier module receives the r-f output from the selectivity module, amplifies the signals as adjusted by an agc feedback loop, and applies the adjusted rf to the remainder of the receiver circuit. The r-f amplifier consists of seven stages. The first four are variable-gain stages. The other three stages form a feedback amplifier consisting of an RC-coupled amplifier, a phase splitter, and a push-pull output amplifier.

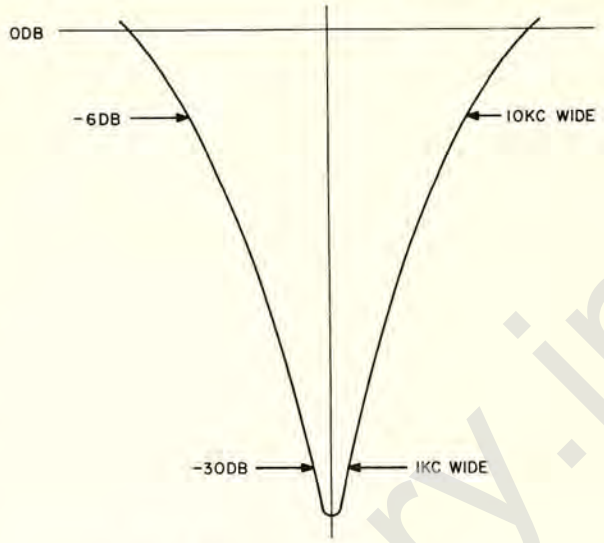


Figure 4-10. Notch Rejection Diagram

(b) DETAIL. - See the schematic diagram of the r-f amplifier, figure 6-123. The signal entering the amplifier at J302 varies in accordance with the strength of the three transmitting stations being received. That is, the master signal, the X-slave signal, and the Y-slave signal will all be different levels depending on the relative distance from the transmitting stations and upon the atmospheric conditions. The level at the input may be as small as 35 microvolts or as large as 0.35 volt rms. In order that the output of the amplifier be at a constant level for all signals, agc voltage applied to the grids is used to change the amount of amplification in the first four stages. These first four stages of the r-f amplifier module are wideband, variable-gain, remote-cutoff pentodes. The mu of this type of tube is a function of bias. Therefore, a large negative bias will reduce the gain of the tube. This means that when a weak signal is received, a small amount of agc will be fed back, permitting the amplifier gain to be near a maximum. Conversely, a large signal will cause a large amount of agc signal to be fed back, reducing the gain of the amplifiers. The normal agc range is from -1.5 to -10.5 volts over the 90-db dynamic range. The gain-controlled stages can actually handle an additional 15 db of large signal, but at reduced accuracy. The gain capability of each of the first two stages is typically from -12 to +17 db. The gain range is from -2 to +18 db for each of the other two stages.

The feedback amplifier consists of stages V305A, V305B, V306, and V307. The approximate overall gain of the feedback section is 20 db. Combined with the first four amplifiers, the maximum gain possible through the r-f amplifier module is 90 db. The output from V305A is applied to V305B, which acts as a phase splitter. The plate output from V305B is applied to the control grid (pins 1 and 7) of V307. The cathode output is supplied to the control grid of V306. These two pentodes are connected in push-pull. The output from the push-pull amplifier is then

applied to output transformer T301. Negative feedback is derived from the secondary of T301 to the cathode of V305A by way of R337 and capacitor C322. The output impedance is lowered to about 100 ohms and some linearity is obtained by the use of this feedback.

Maximum linear output is about 40 volts rms and the saturation level is about 50 volts rms. The output operating level is 0.25 volt rms at the 30-microsecond sample point when the receiver is locked on to a signal and the agc loop is active.

There are four outputs from the r-f amplifier module. One is supplied from the T301 secondary through terminal 15 of TB301 to the detector-strobe portion of the receiver. The second output is supplied from a tap on the T301 secondary through terminal 13 of TB301 to the indicator for monitoring purposes. The third output is filtered and supplied to the envelope deriver through terminal 12 of TB301. The filter is tuned to 200 kc to remove frequencies that would otherwise impair the operation of the envelope deriver. The fourth output is supplied to the noise rectifier through a network consisting of a secondary on transformer T301, capacitors C331 and C332, resistor R349, and diode CR301. This circuitry, together with the noise rectifier, reduces the r-f amplifier gain when it is in danger of saturation. The discussion of the noise rectifier is found in paragraph 4-2*i*(6).

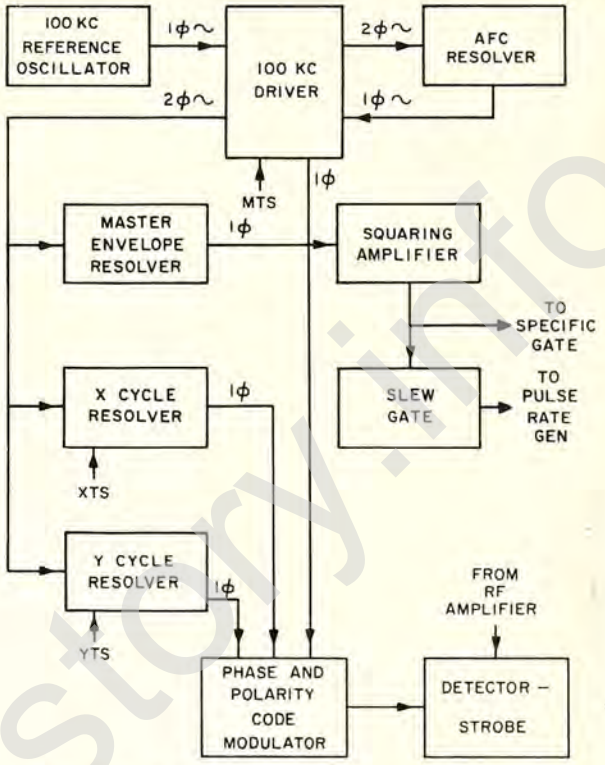


Figure 4-11. 100-Kc Signal Path, Block Diagram

c. 100-KC SIGNAL PATH. - Figure 4-11 shows the 100-kc signal path in block diagram form. A highly stable 100-kc reference oscillator is incorporated in the Loran-C receiver so that the accuracy of the system will be maintained. This oscillator is a transistorized plug-in module which is considered to be as stable and as accurate as a secondary frequency standard. Its output is filtered in the 100-kc driver module to insure minimum harmonic distortion. The output of the filter is applied to the first circuit of the 100-kc resolver driver where the signal is phase split (in quadrature) and is applied as excitation to the master cycle, or afc, resolver. The afc resolver output (single phase) is then applied to the second half of the 100-kc resolver driver where two outputs are produced. One output is the master 100-kc single-phase signal (M 100kc 1Ø); and the other output, 2-phase, is used to excite the X and Y cycle resolvers and the master envelope resolver. Before being applied to the detector-strobe section, the outputs of the afc, X, and Y cycle resolvers are phase and polarity coded in the reference driver.

The master afc signal is then applied to the detector-strobe section and used for synchronous detection of the incoming master signal. The resulting output is used to establish phase-lock between the locally generated master 100-kc signal and the received master signal from the master transmitter. The X and Y cycle resolver outputs are then applied to the detector-strobe for phase detection of the X and Y slave signals. The X and Y cycle servo loops establish and maintain phase-lock between the X and Y 100-kc and the received X and Y slave signals.

The master 100-kc 2-phase signal is also applied to the master envelope resolver. The resolver output is used in the pulse rate generator section of the receiver. The master envelope signal (ME 100kc 1Ø) is locked in with the envelope pattern of the received master signal. The master envelope signal is used to derive the timing sequences in the receiver.

(1) 100–KC REFERENCE OSCILLATOR (A701).

(a) GENERAL. - The 100-kc reference oscillator provides a stable reference frequency for the Loran-C receiver. The 100-kc transistor oscillator has the following characteristics:

Output frequencies	- 100 kc and 2.4 mc
Frequency stability	- One part per million under all ambient conditions for at least one month
Temperature control	- +80.0°C (+176.0°F) within less than 0.1°C from -55.0° to +71.0°C (-67.0°to+159.8°F)
Warmup time	- 30 minutes at -55.0°C (-67.0°F) and 5 minutes at +71.0°C (+159.8°F)
Power to oven	- Approximately 12.0 watts for warmup and approximately 1.5 watts after warmup.

The operation of the reference oscillator can be most readily understood by referring to the block diagram, figure 4-12. The reference oscillator consists of a 3.0-mc, crystal-controlled oscillator; two regenerative divider circuits; a bridge-type circuit, which includes the oven heater; and an audio amplifier circuit tuned to approximately 5.0 kc. The 3.0-mc

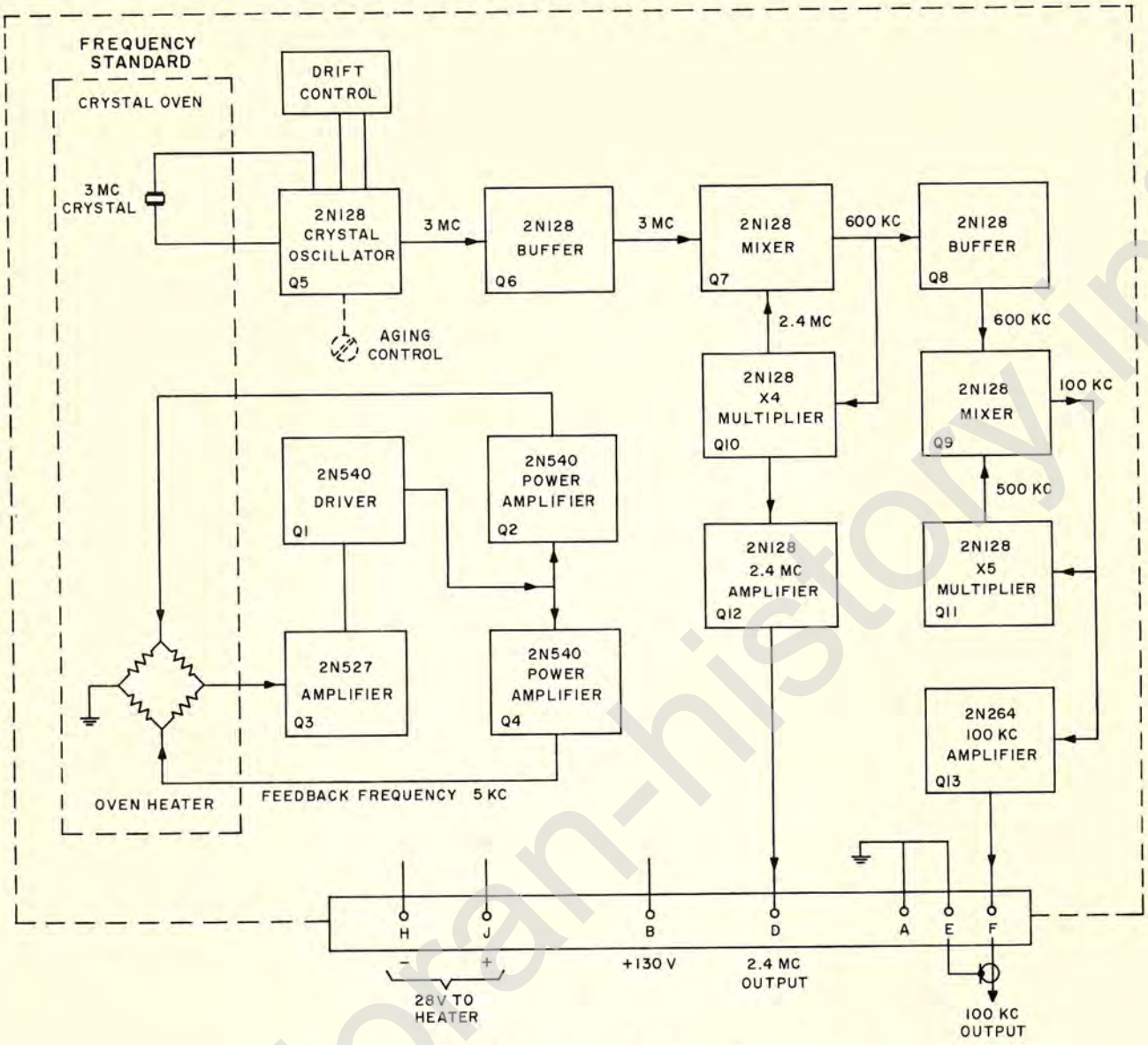


Figure 4-12. 100-Kc Reference Oscillator, Block Diagram

output of the oscillator is coupled to a mixer where it is mixed with a 2.4-mc signal. The difference output of the mixer stage is a 600-kc signal, which is multiplied by 4 in a multiplier to produce the 2.4-mc signal mentioned above. This divider is followed by another divider of the same type in which the 600-kc mixer output is mixed with a 500-kc signal to produce a 100-kc difference frequency. The 100-kc signal is multiplied by 5 to produce the 500-kc injection frequency. The 100-kc and 2.4-mc frequencies are applied as the outputs of the reference generator.

(b) DETAIL. - See the schematic diagram shown in figure 6-127. The crystal-controlled oscillator uses a 3.0-mc quartz crystal, Y701. Oscillator feedback for Q705 is through a variable capacitor that is located on the front panel external to the 100-kc reference oscillator circuit, an internal variable inductor (L701), and crystal Y701. The variable capacitor can be adjusted to compensate for doppler shift. Inductor L701 is a precise variable-frequency control to permit the capacitor to be adjusted in the middle of its range. The oscillator output is taken from the collector of Q705 and coupled through a 3.0-mc buffer amplifier stage Q706 that provides isolation for the oscillator circuit. The collector output of Q706 is applied to the emitter of a 600-kc mixer, Q707. Mixer Q707 and multiplier Q710 form a regenerative divider circuit that is used to divide the oscillator frequency by 5. Mixer Q709 and multiplier Q711 function similarly to divide the first mixer output by 5 for a total division of oscillator frequency by 25. These divisions produce outputs of 2.4 mc and 100 kc from the reference oscillator.

To assist understanding, the following discussion of the regenerative divider theory is provided. The

3.0-mc signal on the emitter of Q707 is not coupled to the collector circuit, since the collector tank circuit is tuned to 600 kc. Regenerative divider operation is initiated when the 3.0-mc emitter signal drives Q707 into conduction and produces transients or noise voltages in the mixer circuit. A 600-kc component of the noise voltage causes low-level oscillations in the collector-tuned circuit that is tuned to 600 kc. A sample of the oscillations is taken from a capacitive voltage divider consisting of C709, C710, and C711, and coupled to the base of multiplier Q710. Application of signal to the base drives Q710 into conduction and results in production of a 2.4-mc component in the collector tank circuit. The 2.4-mc output of Q710 is taken from a capacitive voltage divider consisting of C724, C725, and C726 and applied to the base of mixer Q707 where it beats with the 3.0-mc signal present on the emitter. The difference frequency of 600 kc reinforces the low-level oscillations in the tank circuit of Q707. The collector output of Q707 is coupled to the base of Q708, a buffer amplifier. From the collector of Q707 the signal is applied to the emitter of mixer Q709.

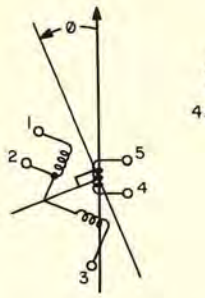
Regenerative divider operation of mixer Q709 and multiplier Q711 is identical to the operation of mixer Q707 and multiplier Q710 except for the frequencies involved. The 600-kc output of Q708 is applied to the emitter of Q709 and initiates low-level oscillations in the collector tank circuit at 100 kc. A sample of the 100-kc signal is taken from capacitive voltage divider C715, C716, C717 and applied to the base of multiplier Q711, driving it into conduction and resulting in production of 500-kc oscillations in the collector tank circuit. A sample of the 500-kc signal is taken from capacitive voltage divider C728, C729, C730 and applied to the base of multiplier Q709 where it is mixed with the 600-kc signal on the emitter. The difference frequency of 100 kc reinforces the low-level oscillations in the Q709 collector circuit. The advantage of these regenerative divider circuits lies in the fact that failure of a preceding stage prevents spurious signal production that could be caused if the circuits were free-running. Another important advantage of these circuits is that a change in the 3-mc oscillator frequency results in a change in the frequency of the 100-kc output which is only 1/30th as great. The 100-kc and 2.4-mc signals are coupled to the output of the reference oscillator through output amplifiers Q713 and Q712 respectively.

Since the frequency accuracy of the Loran-C receiver depends on the stability of the reference oscillator, an oven circuit is employed to stabilize the crystal of the oscillator against ambient temperatures. The crystal, Y701, and a heater, HR701, are enclosed in an insulated envelope for ambient thermal isolation. This unit is temperature controlled at +80.0°C (+176.0°F) by a proportional feedback circuit consisting of the heater and a transistorized audio amplifier tuned to approximately 5.0 kc. The oven heater is in the form of a Wheatstone bridge. Two of the bridge legs, R710 and R711, are composed of high-temperature coefficient nickel wire; while the other two bridge legs, R709 and R712, are made of a low-temperature coefficient copper alloy. The oven heater acts as both heater and temperature-sensing element. At balance temperature, the resistance of the individual resistance arms is 47 ohms with balance predetermined to occur at +80.0°C. When the bridge is below balance temperature, there is a positive feedback around the audio amplifier loop, and power is applied to the heater arms of the bridge. As the bridge heats, it becomes closer to balance until the attenuation of the bridge is nearly equal to the gain of the amplifier. Thus, unity loop gain is nearly achieved and the temperature is only 0.01° below bridge balance temperature.

The transistorized oven-controlled amplifier consists of input amplifier Q703 feeding driver amplifier Q701. Transistor Q701 drives a push-pull, class-B power amplifier consisting of transistors Q702 and Q704. This combination delivers about 12.0 watts to the heater during warmup. When the bridge circuit is subjected to temperature change, the resistance of sensing-element bridge arms changes, causing bridge unbalance. Under this condition, an error signal is derived from the voltage divider action of the bridge and applied to the base of voltage amplifier Q703. The output of Q703 is taken from the collector, coupled through transformer T702, which is tuned to approximately 5.0 kc by C702, and applied to the base of driver amplifier Q701. The collector output of Q701 is applied to transformer T701, which drives the push-pull amplifier stage, Q702 and Q704. The output power of the power amplifier stage at transformer T703 is applied across the heater bridge circuit. This causes element heating that raises the oven temperature until the bridge is restored to balance condition. A temperature-controlled avc bias is supplied to Q703 through R720-C718 so that amplifier saturation is reached with relatively small power outputs at high ambient temperatures. Protective device CB701 removes the short across R706 to provide additional bias when the heater circuit rises above +65.0°C (+149.0°F). This provision prevents transistors Q702 and Q704 from exceeding their maximum leakage current that would cause them to operate nonlinearly and make them susceptible to damage. The 28-volt d-c transistor supply return is isolated from ground to prevent the 5.0-kc frequency of the heater loop from coupling into either of the reference oscillator outputs.

(2) RESOLVERS. - The resolvers used in the Loran-C receiver are electromechanical devices that require two input signals having a phase displacement of 90°. This 2-phase signal is applied to two rotor windings which are physically displaced by 90°. The output signal is induced in the single winding of the stator and is the resultant of the two input signals. Figure 4-13 is a schematic representation of a typical resolver.

With the required 2-phase signal applied to the rotor inputs, the output amplitude will remain constant as the rotor is turned. However, the output phase will shift 360° for each complete turn of the rotor. Ideal signal conditions for a resolver require that the 2-phase signals are exactly 90° out-of-phase and of equal amplitude. Amplitude error, phase error, or harmonic distortion at the input will introduce error in the output signals of the resolver.



1. ROTOR +45 DEGREES
2. ROTOR COMMON
3. ROTOR −45 DEGREES
4,5. STATOR PHASE SHIFTED OUTPUT AT Ø DEGREES

Figure 4-13. Schematic Representation of a Typical Resolver

See figure 4-14 for a pictorial representation of the resolver phase-shift characteristics. Consider sine waves E1 and E2 as applied to the rotor windings E1 and E2. The signals are electrically displaced by 90° and the windings are physically displaced by 90°. Next, consider the voltage induced into the stator winding, shown as output A, by rotor winding E1. Since they are parallel, there will be maximum signal transfer between them. However, no voltage will be induced in the stator by rotor winding E2, when they are at right angles. When the physical relationship of the stator to the rotor changes to 45°, shown as example B, the output signal is a function of both E1 and E2 rotor inputs. Equal energy transfer occurs and the electrical sum, at any one instant, of E1 and E2 will appear as the output. Notice how the phase of the output has changed by 45° when the physical position was changed by 45°. As shown in example C, the rotor moves to a position 90° displaced from the starting point. The stator winding is parallel with the E2 winding and there is maximum signal transfer between them. There is no signal transfer from E1 to the stator when they are at right angles.

The resolvers used in the Loran-C receiver are usually connected so that the rotor common has 15 volts dc applied. This is a supply voltage for the two transistor amplifiers in a resolver driver. The two rotor windings serve as the load elements for these amplifiers which are driven in quadrature (90° phase difference). A typical simplified connection is shown in figure 4-15.

(3) 100-KC DRIVER (A801). - Single-phase inputs to the 100-kc driver produce split-phase outputs which are 90° apart electrically. The circuitry within this unit is used to excite mechanical resolvers which require 2-phase rotor inputs and produce single-phase outputs from the stators. The output phase varies with rotation of the resolver rotor.

The schematic diagram of the 100-kc driver module appears in figure 6-128. A 100-kc sine wave input is coupled from the reference oscillator into INPUT LEVEL control potentiometer R801. This control is set to produce outputs of 4 volts peak-to-peak from the ME, XC, and YC resolvers as observed at TP1 of the master envelope servo module, A1901. A portion of the input signal is coupled through stepup transformer T801 into filter networks L801 and C801 and L802 and C802. The L801 and C801 combination is tuned to reject fourth harmonics (400 kc), and L802 and C802 is tuned to reject second harmonics (200 kc) which might be present in the input signal. The filtered input is impressed across two phase-shift networks. The total combination of the two filters and the phase-shift networks form a series resonant circuit tuned to the fundamental of 100 kc.

Phase-shift network C803-R802-R803 produces a leading phase shift (+45°) that is applied to the base of Q801. Phase-shift network R804, R805, and C804 causes a lagging phase shift (-45°), which is applied to the base of Q802. The signals applied to emitter followers Q801 and Q802 now have a total phase difference of 90°. The emitter circuit of Q801 consists of R806 and C805 and one rotor winding of the afc resolver. Combination R806 and C805 establishes the proper bias for Q801. Combination R807 and C806 and the second rotor winding form the emitter circuit for Q802 with R807 and C806 performing the biasing function. In order to complete the circuits for Q801 and Q802, + 15 volts dc is applied through decoupling network R822-C815 to the afc resolver rotor, which is external to the driver module.

The variable-phase 100-kc output of the afc resolver is applied to the base of Q803. Base bias voltage is applied through the resolver stator and decoupled by R819 and C810. Emitter resistor R808 sets the operating point of Q803 and the signal is amplified and developed across the tuned collector circuit L803, C807, C808, and C809. Collector supply voltage for Q803 is decoupled through network R821 and C816. The output from Q803 is tapped off between C807 and C809 of the tuned circuit. A split-capacity output is employed to match the impedance presented by the following phase-shift networks and to establish a 0-volt d-c level.

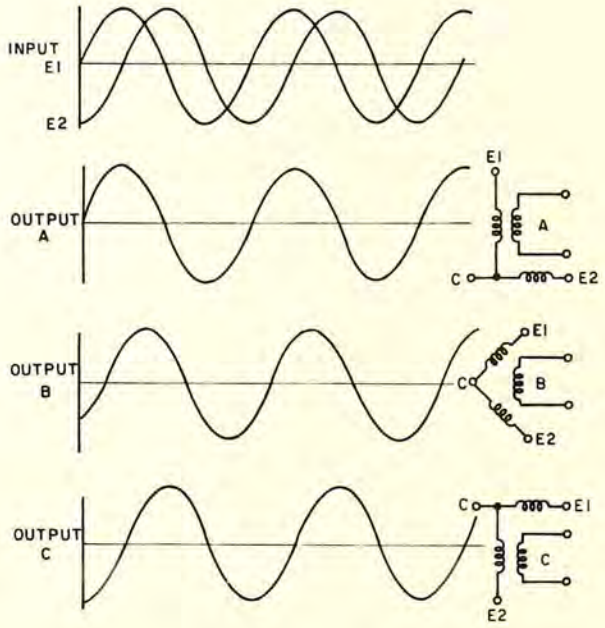


Figure 4-14. Resolver Phase-Shift Characteristics

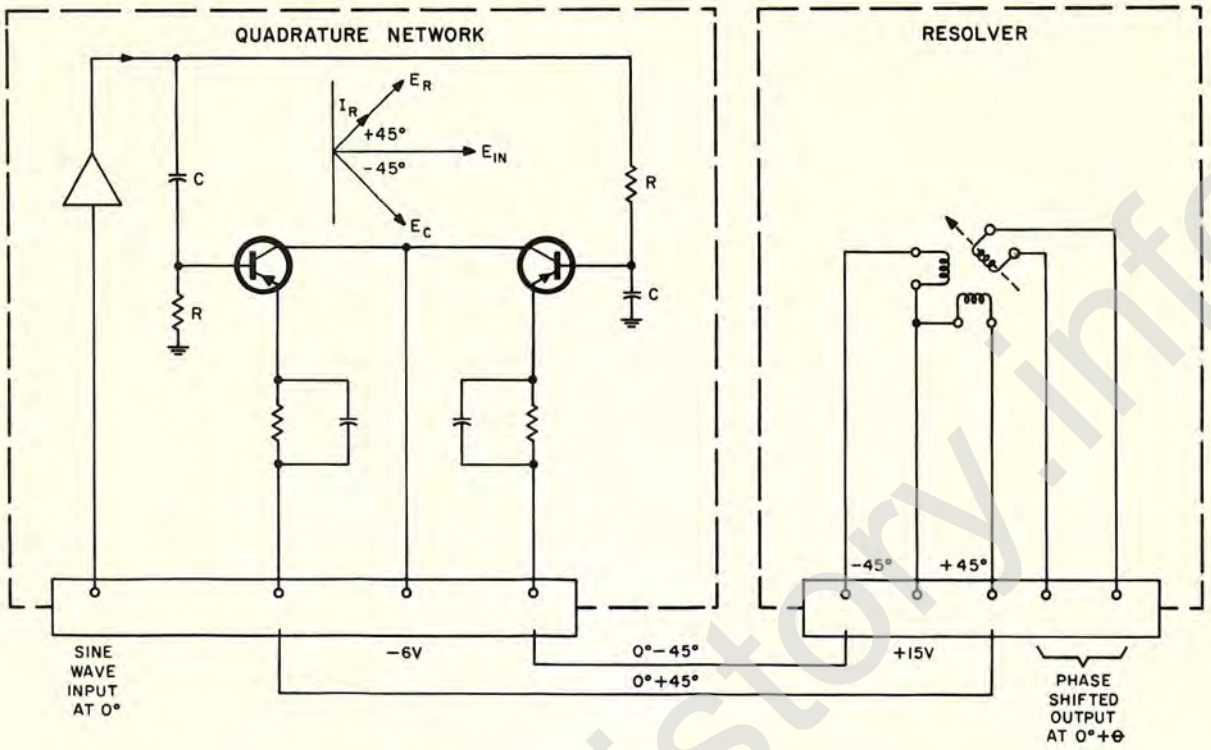


Figure 4-15. Resolver, Typical Connection

Phase-shift network R809, R810, and C811 causes a -45° phase shift on the base of Q804 whereas network C812, R811, and R812 causes a +45° phase shift on the base of Q806. To insure maximum power transfer with minimum distortion, Q804 and Q805 and Q806 and Q807 are compound-connected as emitter followers. The collector supply voltage for Q804, Q805, Q806, and Q807 is decoupled through network R820 and C818. The output signals of Q805 and Q807 are developed across the external rotor windings. The component combinations of R814, R815, C813 and R817, R818, and C814 determine bias. The primary of T802 is connected between Q805 and Q807 in order to cancel out the master 100-kc signal. The emitter circuits of Q805 and Q807 are completed by supplying + 15 volts dc to the common points of the external resolvers through decoupling network R822 and C815.

Provisions for fine adjustment have been incorporated in this driver circuit since exact 90° phase-shift relationship is requird for the master envelope resolver, the X-slave cycle resolver, and the Y-slave cycle resolver. PHASE ADJ potentiometer R809 controls exact phase relationship, and BALANCE ADJ potentiometer R817 controls level balance between Q805 and Q807. In addition to these refinements, zero temperature coefficient components are used in the phase-shift networks for Q804 and Q806.

(4) MASTER CYCLE, X-SLAVE CYCLE, Y-SLAVE CYCLE, AND MASTER ENVELOPE RESOLVERS. - The resolvers used in the Loran-C receiver shift the phase of their outputs to provide the necessary phase matching of locally generated signals with the received transmitted signals. See figure 4-16 for a block diagram arrangement of the resolvers. The master cycle resolver in the master cycle servo is driven by the 100-kc reference signal which has been phase-split in a quadrature network. The output signal from this resolver is a single-phase signal. The signal phase is dependent on the position of the resolver shaft as driven by the servomotor in the master cycle servo module. The signal from the master cycle resolver is amplified and applied to the quadrature and driver network in the 100-kc driver. From this network, two outputs are produced. One is single-phase and the other one is split-phase (two signals separated by 90°). The single-phase, 100-kc signal is essentially the same as the single-phase output from the master cycle resolver unit. This signal is gated by MTS and is applied to the detector-strobe. The MTS, XTS, YTS gating signals are applied from the code group generator.

The 2-phase, 100-kc signals from the 100-kc driver are applied to the X-slave cycle, the Y-slave cycle, and the master envelope resolvers. The X-slave cycle and the Y-slave cycle resolvers are identical in operation. Each is located in its respective delay servo unit. The 2-phase input to a slave resolver determines the frequency and amplitude of the output. The position of the resolver shaft position, as determined by the envelope and cycle motors acting through various gear ratios, establishes the phase position of the resolver output. The two phase-shifted,

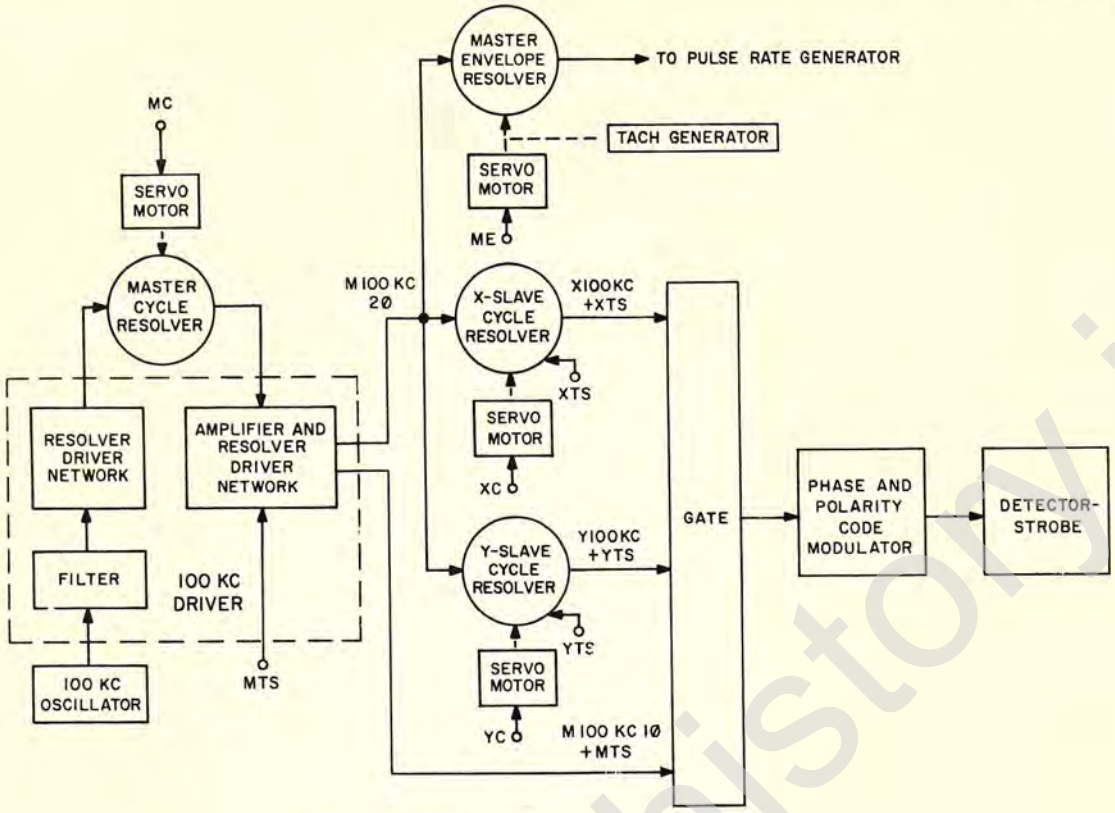


Figure 4-16. 100-Kc Resolvers, Block Diagram

single-phase, 100-kc signals from the slave delay servo units are gated with the XTS (or YTS) signal before being applied to the gate input of the reference driver. The reference driver combines the M100KC, X100KC, and Y100KC signals in time-sharing sequence. The reference driver also filters the signals, modulates them with phase and polarity coding, and applies the resulting signal to the reference input of the detector-strobe. Should any of the reference signals be at an improper phase, the error will be detected and the servomotor involved will drive to correct the phase of the resolver output.

The master envelope resolver also is driven by the 2-phase, 100-kc output from the 100-kc driver. The output from this unit is applied to the pulse rate generator. If there is any error in the master envelope, the derived envelope error output (refer to section 4-2*h*) will cause the master envelope servomotor to reduce the error by moving the repetition interval in time.

The servomotor in the master cycle servo will receive a cycle error input if there is any small frequency difference between the locally generated master signal and the received master signal. This causes the servomotor to drive the master cycle resolver so that the frequency difference cycle error is eliminated. When the master cycle resolver position is changed, the inputs and, hence, the outputs of the X-slave, the Y-slave, and the master envelope resolvers are all phase-shifted a corresponding amount.

(5) SQUARING AMPLIFIER (A935-A938).

(a) GENERAL. - The squaring amplifier plug-in printed board produces a symmetrical square-wave output from a sine wave input. The printed circuit board contains three transistors, associated resistors and capacitors, and one diode. The squaring amplifier is basically a high gain amplifier that is overdriven to clip the applied sine-wave input and produce the square-wave output.

(b) DETAIL. - See the schematic diagram of the squaring amplifier, which appears in figure 6-134. Assume that the sine wave input is swinging in a negative direction. The input signal is applied to the junction of R1-R2-Q1 (base). Network R1 and R2 establishes the bias level for the emitter follower Q1. As the signal at the base of Q1 goes more negative, Q1 conducts more heavily and a negative-going signal is produced at the emitter of Q1 due to the increased current flow through R3. Combination R3, R4, and R5 forms a bias and signal-dividing network. The negative-going signal is applied to the base of Q2, a high-gain common-emitter amplifier. A small change in the negative-going base signal will drive the transistor into saturation and cause clipping in the output of Q2. Combination R7, R8, and C2 forms the emitter circuit of Q2. Resistor R8 is heavily bypassed by C2 to reduce negative feedback and maintain the high-gain characteristics of the amplifier. The emitter of Q2 is returned to ground and is biased so that the transistor tends to saturate as the signal on its base goes negative (from zero). The signal

applied to Q2 is amplified, inverted, and developed across the collector load, R6. Combination R6, R9, R10, and C3 forms a bias and signal-divider network for Q3. Capacitor C3 is a compensating capacitor which steepens the wave shape applied to the base of Q3. The collector voltage of Q3 is clamped to -6 volts through R11 by CR1.

During the positive-half cycle of the input, Q1 passes the positive-going signal to the base of Q2. Transistor Q2 tends to cut off and produces a negative-going signal at its collector. The negative-going signal is coupled to the base of Q3 which goes into heavy conduction. During heavy conduction, the collector approaches the emitter level of 0 volt and the output of the module switches from -6 volts to 0 volt. As the sine wave input crosses the zero reference in a positive direction, the output will go to 0 volt. As the sine-wave input crosses the zero reference in a negative direction, the output will go to a level of -6 volts.

d. 50-KC AND 10-KC SIGNAL PATH AND SIGNAL GENERATING SCHEME. - See figure 4-17 for the 50-kc and 10-kc signal path block diagram. The 50-kc and 10-kc signals used in the Loran-C receiver are derived from the 100-kc source previously discussed. Since the phase relationship of both the 50-kc and 10-kc signals must be referenced to the master 100-kc (M 100-kc 1Ø), the output of the master envelope resolver is the source from which the 50-kc and 10-kc signals are derived. The output of the master envelope resolver is applied to a squaring amplifier and the resulting square wave is applied to a divide-by-2 toggle circuit to produce 50-kc square waves. The 50-kc signal is passed through the slew gate module and terminates at the inputs to the basic

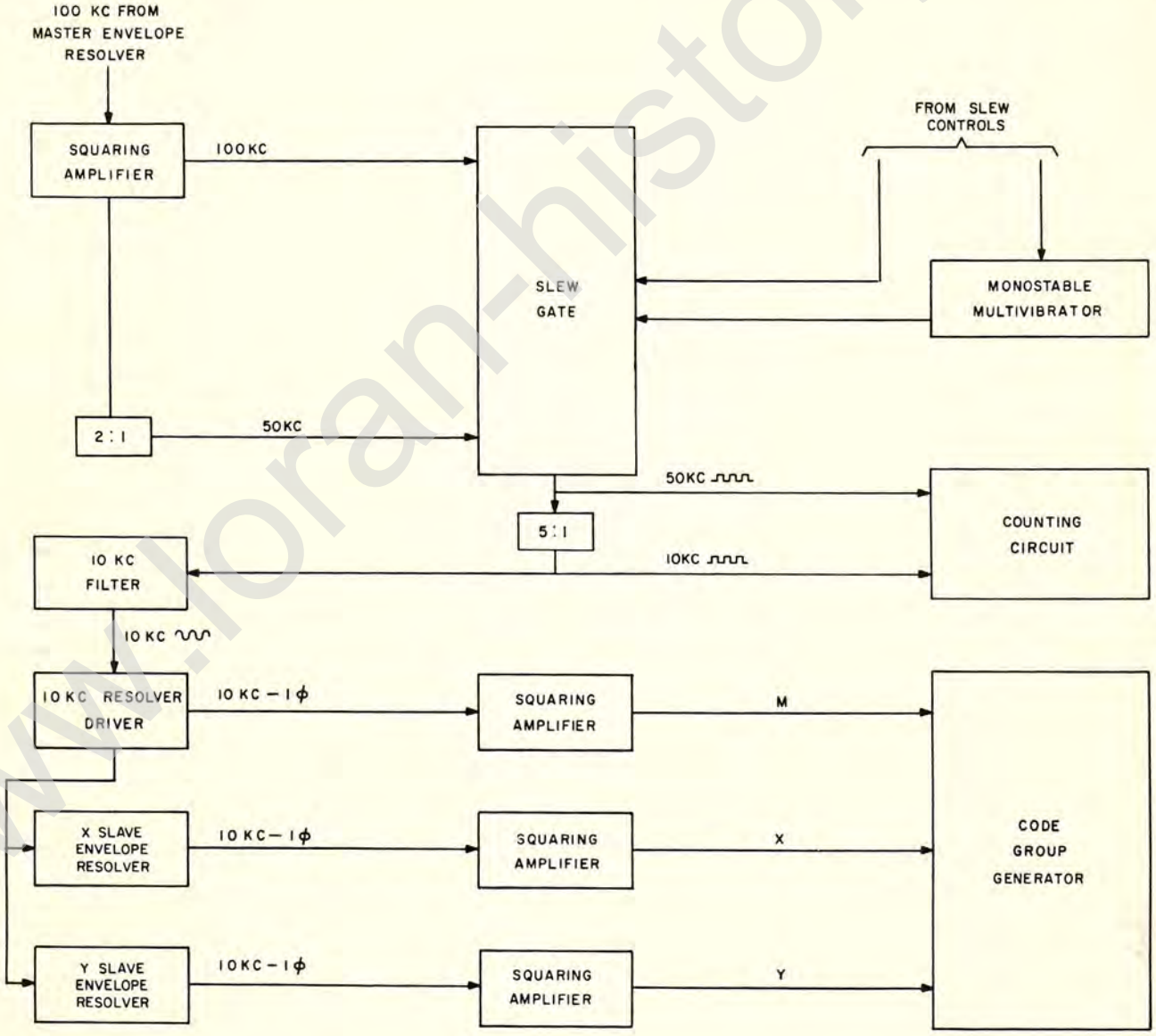


Figure 4-17. 50-Kc and 10-Kc Signal Paths, Block Diagram

counter (in the pulse rate generator), to the divide-by-5 counter circuit, and to the coincidence output circuit. See figure 4-2, the overall block diagram for the receiver. The 50-kc square wave, varying between 0 and -6 volts, is applied to the coincidence output circuit and prevents diode noise from affecting the gate signal to the code group generator from either coincidence detector.

With 50kc as an input, the divide-by-5 circuit produces a 10-kc square-wave output. The 10-kc square wave is passed through the specific gate (in the pulse rate generator) and terminates as the inputs to the specific counter circuit (also in the pulse rate generator). The 10-kc square wave also is applied to the 10-kc filter module. Since a 10-kc sine wave is required for resolver excitation, the 10-kc filter is employed to reshape the incoming square wave into a sine wave. This 10-kc sine wave is applied to the 10-kc resolver driver that produces two outputs: a single-phase output and a 2-phase quadrature output. The single-phase output is applied to the master squaring amplifier from which the M10KC input to the pulse group timing gate (in the code group generator) is produced. The 2-phase output is applied to the X and Y envelope resolvers in the slave delay servo modules. The X and Y 10-kc signals from these slave delay modules are each squared in individual squaring amplifiers. The resulting X10KC and Y10KC signals also are supplied as inputs to the pulse group timing gate.

(1) BASIC TOGGLE CIRCUIT (A901-A930, A1301-A1310, A1501-A1503).

(a) GENERAL. - The toggle circuit may be thought of as a 2-position switch which is stable in either position. The toggle circuit has several applications in the Loran-C receiver; however, it is primarily used as a divide-by-2 device. By applying a square-wave signal to the two CP inputs in parallel, the toggle circuit will produce a square-wave output that is at one-half of the frequency of the applied signal. See figure 6-129 for the schematic diagram of the toggle circuit. Connections are made so that only positive-going pulses will change the state of the circuit. In practice, the toggle is a bistable flip-flop multivibrator. Except during the transient time of changing circuit state, either one of the transistors may be conducting while the other is cut off. Transistors in the circuit are referred to as being ON (conducting) or OFF (nonconducting). In most applications of the toggle, a positive-going input pulse will turn the ON transistor OFF.

(b) DETAIL. - The basic toggle circuit is shown in figure 4-18. As shown, the circuit consists of collector-load resistors, feedback resistors, and base-biasing resistors. The toggle circuit is bistable: either one of the transistors may conduct while the other is cut off. There is also no tendency for the existing condition to change except by the application of an external pulse. First, the assumption has been made that Q1 is conducting and that Q2 is shut off. In this condition, the collector of Q1 is at zero potential and the base is biased somewhat negatively. The collector of Q2 is established at the negative supply voltage and the base is at some small positive voltage.

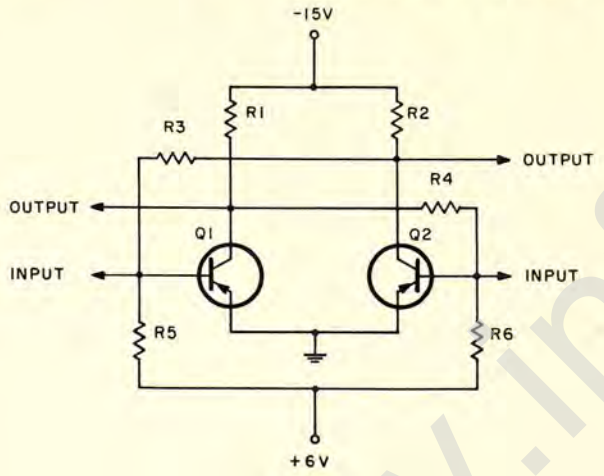


Figure 4-18. Basic Toggle Circuit, Simplified Schematic Diagram

The simplified circuit shown in the figure will change state with either the application of a positive voltage to the base of Q1 or with a negative voltage to the base of Q2. If a positive voltage is applied to Q1, the base becomes less negative than the grounded emitter and the transistor will cut off. The collector voltage will quickly drop to the value of the negative bias voltage applied to it. As the collector of Q1 becomes more negative, the base of Q2 will become more negative with the voltage across resistor R6. Transistor Q2 will begin to conduct when its base goes negative. Positive feedback is, therefore, effectively applied to Q2. As a result, the circuit has changed state. Notice that negative voltage applied to the base of Q2 would cause the same effect. Transistor Q2 will start to conduct with the applied voltage. As it conducts, the voltage on the collector will start becoming more positive from the low bias voltage at which it was maintained at cutoff. The rising voltage on the collector will be reflected on the base of Q1 through feedback resistor R3, driving it positive and cutting off Q1.

In the actual circuit, figure 6-129, several other refinements are made. First, diodes with their anodes biased at -6 volts are inserted in the output paths. These diodes will ensure that any voltage will not be more negative than -6 volts. Should a voltage more negative than -6 volts be applied to either diode, that diode will conduct and establish a level of -6 volts to the circuit. Hence, all output signals from the circuit vary only from 0 volt (the potential of the emitter when a transistor is conducting) to -6 volts.

Capacitors have been placed parallel to the feedback resistors. The voltage across one of these capacitors will change instantaneously with an applied voltage and, as a result, will instantaneously reflect any level change. Once a new steady level is reached, the voltage will still be maintained across the feedback resistors as shown in the simplified circuit.

The input capacitors placed in both input paths will reflect any new change in level without maintaining it. For example, should the input rise from a constant

level of -6 volts to a constant level of 0 volt, the voltage on the capacitor will reflect an instantaneous rise of 6 volts and then return to its previous value.

The diodes with their anodes in the collector circuit of the two transistors act as saturation-suppressors. Without a diode in the circuit, as the base of a transistor goes from its positive cutoff value to its negative bias, the emitter will go more positive, and at some point the transistor will reach saturation. A diode is placed in the collector circuit of the transistor to prevent this from happening. When the base and the collector approach a point where their potentials are very close to being the same value, near saturation, the 180-ohm resistor will cause the diode to conduct, drawing the high potential of the collector to the potential of the base. This establishes the extent to which the transistor will conduct.

The gating diodes inserted at each input eliminate the possibility of triggering the circuit with a negative pulse. In the simplified diagram of figure 4-19, a negative-going pulse is applied to the circuit at the CP points. This would ordinarily change the state of the circuit if the diodes were not present. If Q2 is assumed to be conducting prior to the pulses, the voltages will be as marked in the diagram if it is also assumed that the diodes were not perfect and that a nominal 0.2-volt drop existed across each one of them. Remember, that in the actual circuit, the cathodes of the diodes are always just slightly more negative than the anodes when the diodes are conducting. At the diodes working in connection with Q1 (on the left), the cathodes (which are joined together at point A) will be approximately zero. This is because the anodes of both diodes are at zero potential. The cathodes of the other pair of diodes, at point B, will also be at a potential of approximately zero since a level of 0 volt is applied at CP. When a negative voltage is applied to the circuit, there will still be a zero voltage applied on the left, at K1, which maintains the potential of the joined cathodes at 0 volt.

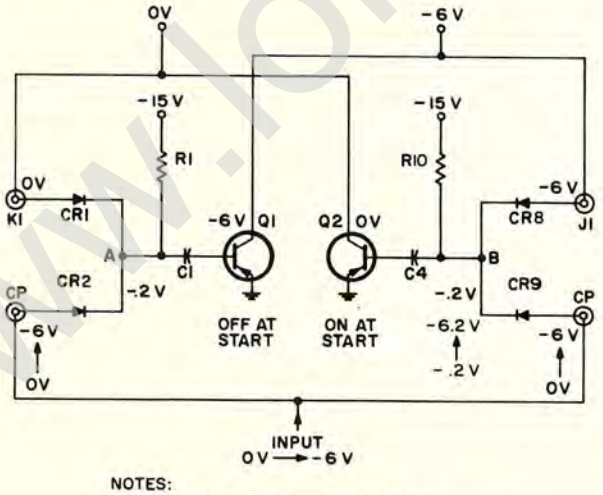


Figure 4-19. Toggle Diode Gating with a Decreasing Input

On the right, the anodes of the diodes will be -6 volts. This will cause the joined cathodes to become negative. Therefore, point B has gone from a value of approximately zero to a negative value, which has no effect on conducting transistor Q2. Hence, an incoming pulse that is negative-going will not change the state of the circuit.

The assumption is now made that Q1 is cut off and a level of -6 volts is being inserted at the CP points. Under these conditions, the voltages are as marked in figure 4-20. Notice that at point B, the voltage is approximately -6 volts since J1 and CP are both at -6 volts. A positive-going pulse at the CP points will now have a definite effect. On the left, since the anode of diode CR1 at K1 was zero before, there will be no change in the voltage at point A, the voltage remaining at 0 volt. But a change from -6 volts to 0 volt on the right will cause point A to become more positive. The positive-going signal will be reflected in the input capacitor and will drive the base of Q2 positive. This cuts off Q2 and changes the state of the circuit. These gating diodes, then, ensure that only a positive-going pulse will change the state of the circuit.

Points K2 and J2 provide a means of externally applying a signal that will ensure the conduction of a specific transistor. In figure 4-21, the assumption is

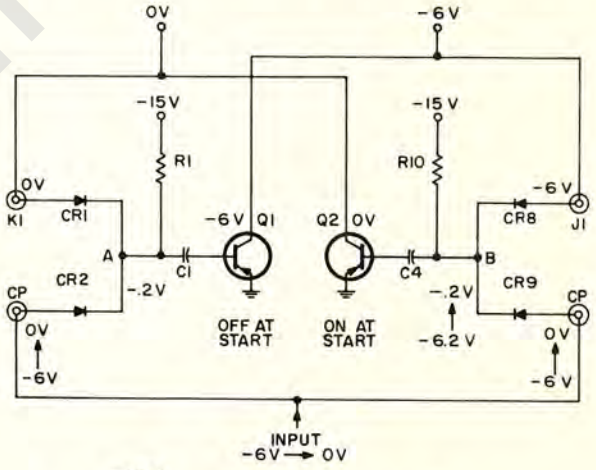


Figure 4-20. Toggle Diode Gating with an Increasing Input

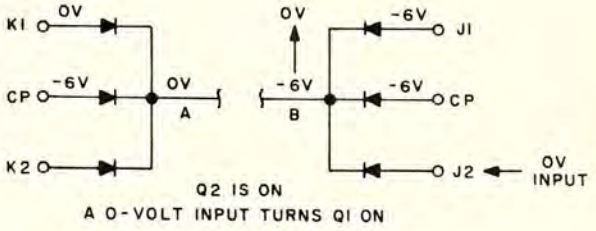


Figure 4-21. Toggle External Gate Switching Starting with Q1 Off

that the voltages are as marked and that Q2 is conducting. It is desired that Q1 be conducting. A positive-going signal applied at J2 will cause this effect, driving the base of Q2 positive. Had Q2 been cut off and Q1 been conducting, the initial voltages would be as in figure 4-22. The joined cathodes of the diodes would already be near zero potential. The -6-volt to 0-volt positive-going pulse applied to J2 would have no effect on the joined cathodes, and Q2 wold remain cut off.

It should be noted that the K2 input is applied directly to the base of Q1. This input is used for the reset pulse, which swings from -6 volts to +6 volts. The width of the reset pulse is sufficient to overcome any switching transients and assures that all toggles, when reset, will settle in a common reference state with the $\overline{Q}$ output at -6 volts and the Q output at 0 volt.

(2) SLEW GATE (A939).

(a) GENERAL. - The slew gate circuit is used in the 50-kc signal path to control the input to the basic counter of the pulse rate generator. The slew gate serves as an inverter for the 50-kc signal from the divide-by-2 toggle under normal tracking conditions. When the system is "searching", the function of the slew gate is to add to or subtract pulses applied to the input of the counter between each master trigger. The actual time between master triggers is extended by 20 microseconds by deleting a pulse to the counter. The actual time between master triggers is shortened by 20 microseconds by adding a pulse. In this manner, the generated trigger can be made to move, in time relationship, with respect to the received master signal. Slewing is used to expedite the search process and cause coincidence between the received trigger and the generated trigger faster than could be accomplished by automatic servo search of the receiver. See figure 6-135 for the schematic diagram of the slew gate circuit. The time relationships of the wave shapes encountered in the slew gate circuit are shown in figure 4-23. The slew gate is composed of two basic functions, a 50-kc gate (Q2-Q3), and a 100-kc gate (Q1).

(b) TRACK. - First consider the operation of the circuit in the normal track condition when only the 50-kc signal is passed. The following reference letters list the signal conditions and locations discussed. The signal wave shapes with time relationships are presented in figure 4-23 in the same reference letter order:

A - 100-kc input, terminal 3
B - 50-kc input, terminal 2

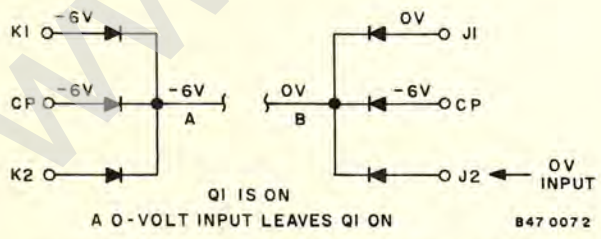


Figure 4-22. Toggle External Gate Switching Starting with Q1 On

C - Output to the counter during track conditions, terminal 7
D - Monostable multivibrator input, terminal 4
E - Complementary monostable multivibrator input, terminal 1
F - Slew left input on the base of Q2
G - Output to the counter during slew left conditions, terminal 7
H - Slew right 100-kc input on the emitter of Q1
I - Slew right composite input on the base of Q3
J - Output to the counter during slew right conditions, terminal 7

Inputs applied during the track condition are A, B, D (zero volts), and E (-6 volts). The 100-kc signal (A) is applied to the anode of CR3 and is blocked. The 50-kc signal (B) is applied to the anode of CR2 at the same time an input of -6 volts (E) is applied to the anode of CR1. Diodes CR1-CR2 form an AND circuit which requires that both signals be present. When both input B and input E are at a level of -6 volts, the base of Q2 is also at a level of -6 volts. Since Q2 is an emitter follower, the level applied at the base is also present at the emitter. When input B swings to a level of zero volts, this level is applied at the base of Q2, and in this manner the 50-kc signal is passed to the emitter of Q2. During track conditions, the 100-kc gate is effectively closed since the base of Q1 is held at ground potential by R1 and R2 and the 100-kc signal never causes CR3 to conduct. The level of 0 volt applied to the base of Q1 is also present at the emitter of Q1.

An OR circuit composed of CR5 and CR4 precedes the output transistor Q3. The OR circuit is constructed so that either Q1 or Q2 emitter signal will be applied to the base of Q3. Since the emitter of Q1 is held at a level of 0 volt, the signal from the emitter of Q2 is applied at the base of Q3, inverted, and coupled to the output from the collector of Q3. CR6 clamps the maximum negative level of the output to -6 volts. Consequently, only the 50-kc signal (C) is present at the output of the circuit during the track condition.

(c) SLEW LEFT. - Next, examine the input conditions during slew left condition. Assume that the slew speed control is set to maximum speed and the monostable multivibrator produces an input to the slew gate with each master trigger (MT). Refer to figure 4-23 for the relationships of the input signals. At the time of MT, the monostable multivibrator fires and input D goes to a level of -6 volts while input E goes to a level of 0 volt. Inputs A and B are applied as in the previous example. Since relay K1 remains open, the emitter of Q1 remains at a level of 0 volt as previously explained. When input E goes to a level of 0 volt, the base of Q2 is clamped to 0 volt by CR1 and the 50-kc signal is blocked at the base of Q2. The input signal applied at the base of Q2 is shown as signal F. This signal is applied to the base of Q3, inverted, and appears at the collector of Q3 as the output signal (G). Notice that one pulse of the 50-kc signal is blocked and does not appear at the output.

(d) SLEW RIGHT. - For the slew right process, the contact of K1 is closed, allowing input D to be applied to the junction of R1 and R2. The monostable

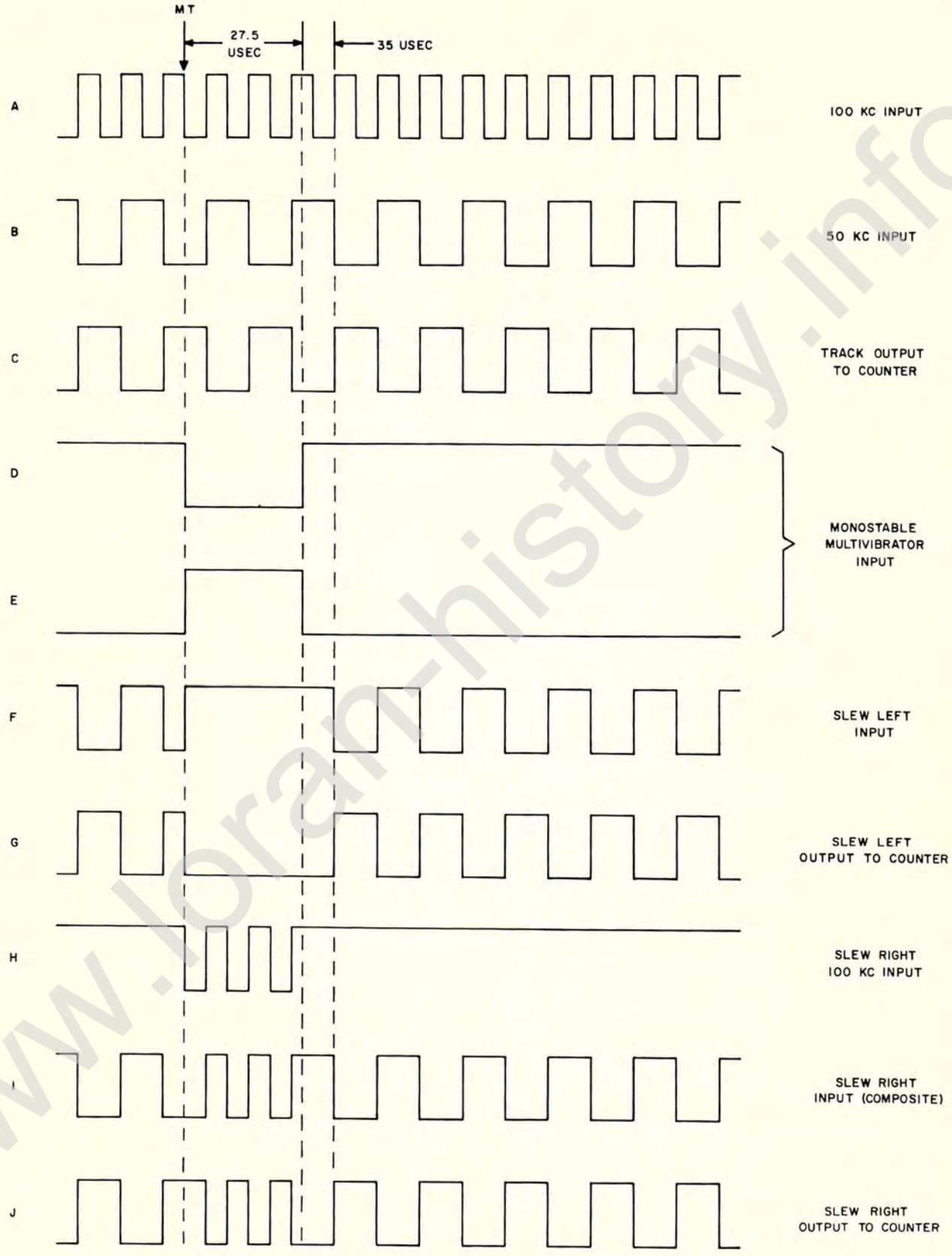


Figure 4-23. Slew Gate, Timing Waveshapes

multivibrator fires at MT time, which blocks the 50-kc signal to the base of Q2 and opens the 100-kc gate. Signal H appears at the emitter of Q1 for the duration of the monostable pulse (input D). Diode CR4 passes the two pulses of the 100-kc signal to the base of Q3, where they are added to signal F to produce the composite signal (I) at the base of Q3. This signal is inverted and appears at the collector of Q3 as the output signal (J). It can be seen that an extra pulse has been added at the output.

(3) MONOSTABLE MULTIVIBRATOR (A940).-The monostable multivibrator plug-in printed board is triggered by the negative-going trailing edge of a timing pulse. The monostable multivibrator produces two square-wave output pulses of equal duration and opposite polarity. The duration of the output pulse is adjustable between 20 and 50 microseconds. The circuit operates as a 2-stage collector-coupled multivibrator and produces one output cycle for each input trigger applied.

See the schematic diagram of figure 6-136. During the time between input triggers, an "at rest" condition is established. Divider R1-R2 supplies cut-off bias to Q1, and its collector is clamped at a level of -6 volts by CR1. Q2 is conducting, its collector is approximately 0 volt, and C2 is charged to approximately 6 volts. The output from the Q1 collector is -6 volts and the output from the Q2 collector is 0 volt.

The following chain of events takes place when a negative-going signal is applied to the input of the monostable multivibrator. Capacitor C1 differentiates the change in input voltage that causes the voltage at the base of Q1 to go to a negative value and Q1 to conduct. The collector of Q1 goes to 0 volt, the charge across C2 is impressed on the base of Q2 as a positive signal, Q2 cuts off, and the collector of Q2 goes to -6 volts. Diode CR2 clamps the collector of Q2 to a level of -6 volts and divider R1 and R2 holds Q1 in a conducting state. Capacitor C2 discharges through R5 and R4 to the negative 6-volt supply and the base voltage of Q2 moves toward 0 volt. When the base of Q2 reaches approximately 0 volt, Q2 conducts and returns the multivibrator to the "at rest" condition. The time required for one cycle depends on the setting of R5 in the C2 discharge path.

(4) DIVIDE-BY-5 CIRCUIT. - The divide-by-5 circuit is composed of three basic toggle plug-in boards. Special interconnections for this circuit are shown in figure 4-24. Since the basic toggle has an inherent divide-by-2 function, it is necessary to incorporate inhibit functions in the circuit to overcome the normal operation of the toggles and to produce the desired division of 5.

As previously explained in paragraph 4-2*d*(1), the basic toggle has three inputs for each transistor. An input is applied to change the state of the flip-flop and produce a change in output. Only positive-going pulses applied to inputs of conducting transistors will cause a change at the output of a toggle board. Positive-going pulses applied to a transistor that is cut off have no effect at the output. Negative-going pulses applied to either a conducting or cut off transistor have no effect at the output. However, a zero voltage applied to an input prevents a positive-going pulse on the same side (-6 to 0) from passing to the base and inhibits any change at the output of a toggle board.

The input to the divide-by-5 circuit is a square wave which swings between 0 volt and -6 volts. The output is a square wave with polarity and amplitude similar to the input, but its period is five times that of the input. There is also a special reset input which is applied to all three boards used in the divide-by-5 circuit of the code group generator. The reset input is used to establish a starting time reference for the divider.

In order to simplify the explanation for the divide-by-5 circuit, refer to figure 4-24 and table 4-4. Figure 4-24 also shows the time relationship of the important wave shapes encountered in the divider. The table shows the polarity of important signals applied to inputs of the divider toggles. By comparing the wave shapes in the figure and the simultaneous inputs in the table, the divide-by-5 circuit can easily be explained. A + indicates a positive-going pulse, a 0 indicates no change, and a - indicates a negative-going pulse.

First, assume that a reset pulse is applied to the divide-by-5 circuit. The reset pulse has sufficient amplitude (-6 to +6 volts) to overcome any inhibit action in the circuit and cut off all $\overline{Q}$ transistors. Thus, immediately after the reset pulse occurs, all $\overline{Q}$ outputs are at -6 volts. This condition is illustrated at the beginning of the time diagram of figure 4-24.

The first pulse of the input signal is applied to the divide-by-5 circuit. The positive-going pulse is applied to both the $\overline{CP}$ and CP inputs of toggle 1, and to the $\overline{CP}$ input of toggle 3. Toggle 1 is triggered by the positive-going pulse at the CP input, causing the $\overline{Q}$-1 output to switch from -6 volts to 0 volt. The $\overline{Q}$-1 output, which is connected to the $\overline{CP}$ and CP inputs of toggle 2, triggers this stage and causes the $\overline{Q}$-2 output to switch from -6 volts to 0 volt. The $\overline{Q}$-2 variation, in turn, is applied to the CP input of toggle 3 to trigger this stage, and switches the $\overline{Q}$-3 output from -6 volts to 0 volt. Thus, after the first signal pulse, all $\overline{Q}$ outputs are at 0 volt.

The second input pulse at $\overline{CP}$ of toggle 1 causes the $\overline{Q}$ transistor to cut off; and, consequently, the $\overline{Q}$-1 output switches from 0 volt to -6 volts. Since positive variations are required to trigger the toggle circuits, toggle 2 is not affected by the negative $\overline{Q}$-1 output variation. The $\overline{Q}$-2 output, therefore, remains at 0 volt. Toggle 3, which would normally be switched by the positive pulse at $\overline{CP}$, is inhibited from switching at this time because the $\overline{Q}$-1 output (0 volt before switching) is connected to the K1 input of toggle 3 as an inhibit voltage. Therefore, the $\overline{Q}$-3 output remains at 0 volt.

At the third pulse, toggle 1 is inhibited from triggering by a voltage obtained from the $\overline{Q}$-3 output of toggle 3 (0 volt before triggering) and applied to the J2 input of toggle 1. Therefore, the $\overline{Q}$-1 output remains at -6 volts. Since toggle 2 is triggered by a positive variation in the $\overline{Q}$-1 output, it is not affected by the third trigger pulse. Therefore, $\overline{Q}$-2 remains at 0 volt. However, toggle 3 is triggered by the third input pulse at the $\overline{CP}$ input, because the previously mentioned K1 inhibit voltage was removed when toggle 1 was triggered by the second pulse. The $\overline{Q}$-3 output switches from 0 volt to -6 volts.

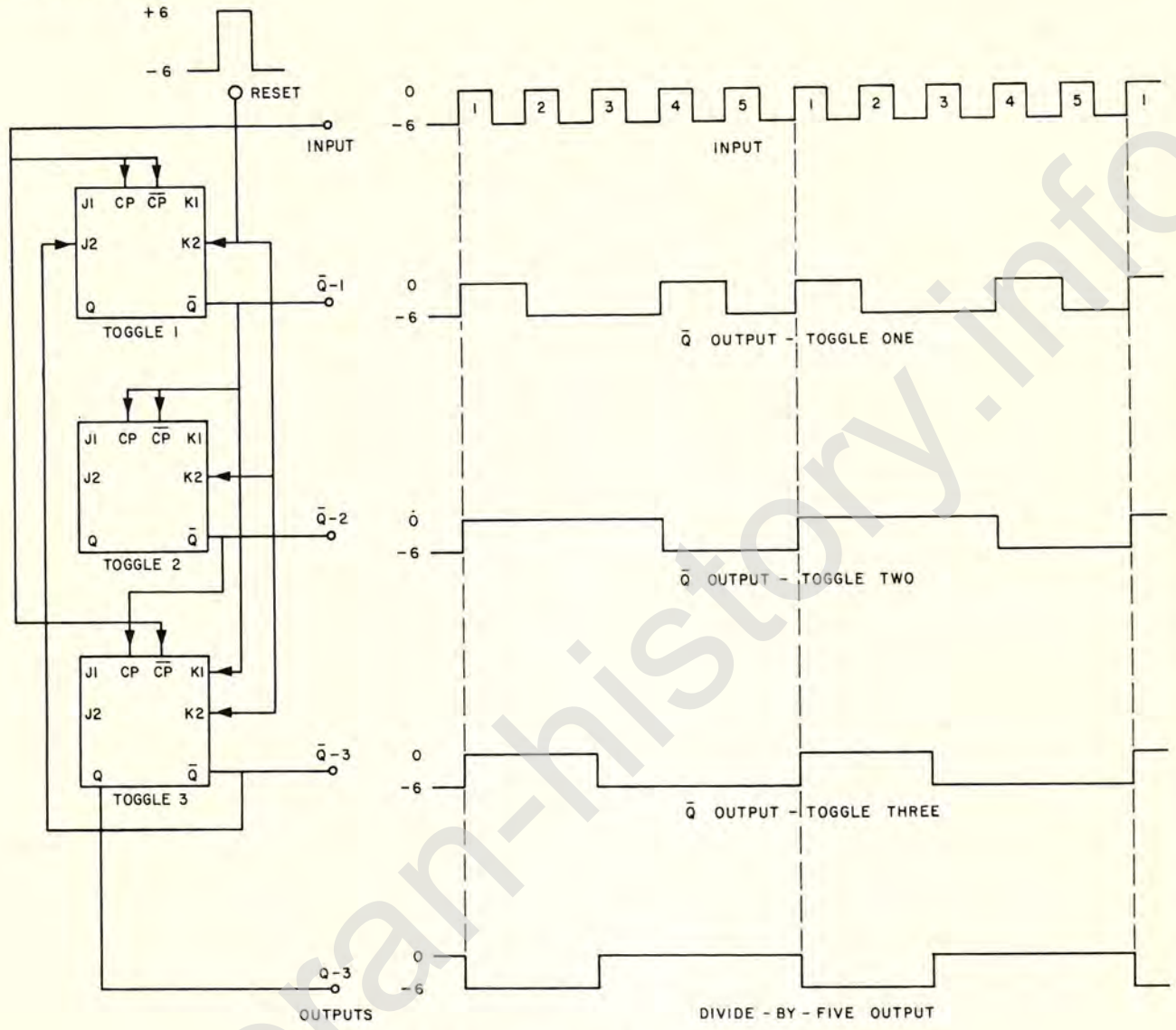


Figure 4-24. Divide-by-5 Circuit, Block Diagram

The fourth pulse triggers toggle 1 since the J2 inhibit voltage was removed by the switching of toggle 3 at the third pulse. The $\bar{Q}$-1 voltage variation from -6 volts to 0 volt switches toggle 2. The negative variation of the $\bar{Q}$-2 from 0 to -6 volts, however, has the wrong polarity to switch toggle 3, so $\bar{Q}$-3 remains at -6 volts.

The fifth pulse switches the $\bar{Q}$-1 output of toggle 1 from 0 to -6 volts. Since toggle 2 requires a positive-going trigger, the negative variation has no effect. The $\bar{Q}$-2 output remains at -6 volts. The $\bar{Q}$-3 output from toggle 3 also remains at -6 volts at the fifth trigger, since at this time it requires a positive variation in the $\bar{Q}$-2 signal to trigger.

The three toggles are now in the same state that existed immediately following the reset pulse, but prior to the first signal pulse. The sixth pulse begins a repetition of the sequence just described. For each sequence of five pulses applied to the input, the output (Q of toggle 3) completes one cycle. Thus, a frequency division of 5-to-1 is accomplished.

(5) 10-KC FILTER (A933). - The 10-kc filter circuit is contained on a single plug-in printed board which is found in the lower drawer of the Loran-C receiver. The purpose of this circuit is to accept a 10-kc square wave and produce a 10-kc sine wave output. See figure 6-132 for the schematic diagram of the 10-kc filter circuit.

The input to the circuit is applied through series impedance-matching resistor R1 and C2, which shunts any high-frequency harmonic content of the input to ground. The combination of L1 and C1 forms a parallel circuit tuned to 20-kc, which functions as a low-pass element and attenuates the second harmonic

TABLE 4-4. DIVIDE-BY-5 TIME SEQUENCE TABLE

1. First Pulse After Reset.			
Toggle 1 inputs -	CP	+	Switches Q Off
	J2	+	
	$\overline{CP}$	+	
Toggle 2 inputs -	CP	+	Switches Q Off
	$\overline{CP}$	+	
Toggle 3 inputs -	CP	+	Switches Q Off
	K1	+	
	$\overline{CP}$	+	
2. Second Pulse After Reset.			
Toggle 1 inputs -	CP	+	No Reaction - Q is Off
	J2	+	
	$\overline{CP}$	+	Switches $\overline{Q}$ Off
Toggle 2 inputs	CP	-	
	$\overline{CP}$	-	
Toggle 3 inputs -	CP	0	
	K1	-	
	CP	+	No Reaction - $\overline{Q}$ is On
3. Third Pulse After Reset.			
Toggle 1 inputs -	CP	+	No Reaction - Positive-going pulse is inhibited by negative-going pulse
	J2	-	
	$\overline{CP}$	+	No Reaction - $\overline{Q}$ is Off
Toggle 2 inputs -	CP	0	
	$\overline{CP}$	0	
Toggle 3 inputs -	CP	0	
	K1	0	
	$\overline{CP}$	+	Switches $\overline{Q}$ Off
4. Fourth Pulse After Reset.			
Toggle 1 inputs -	CP	+	Switches Q Off
	J2	0	
	$\overline{CP}$	+	No Reaction - $\overline{Q}$ is Off
Toggle 2 inputs -	CP	+	
	$\overline{CP}$	+	Switches $\overline{Q}$ Off
Toggle 3 inputs -	CP	-	
	K1	+	No Reaction - $\overline{Q}$ is Off
	$\overline{CP}$	+	
5. Fifth Pulse After Reset.			
Toggle 1 inputs -	CP	+	No Reaction - Q is Off
	J2	0	
	$\overline{CP}$	+	Switches $\overline{Q}$ Off
Toggle 2 inputs -	CP	-	
	$\overline{CP}$	-	
Toggle 3 inputs -	CP	0	
	K1	-	
	$\overline{CP}$	+	No Reaction - $\overline{Q}$ is Off
6. Sixth Pulse After Reset.			
Toggle 1 inputs -	CP	+	Switches Q Off
	J2	+	
	$\overline{CP}$	+	
Toggle 2 inputs -	CP	+	Switches Q Off
	$\overline{CP}$	+	
Toggle 3 inputs -	CP	+	Switches Q Off
	K1	+	
	$\overline{CP}$	+	

distortion elements. The combination of C3, L2, and C4 forms a parallel circuit tuned to the fundamental of 10-kc. The 10-kc tuned circuit shunts unwanted harmonics to ground and allows only the fundamental to appear across the output load resistor R2.

(6) 10-KC RESOLVER DRIVER (A934). - The 10-kc resolver driver plug-in printed board produces, from a sine wave input, quadrature outputs for the X-slave and Y-slave envelope resolvers and a single-ended reference signal output. The basic circuit is divided into an isolating input stage, a pair of phase-shift networks, and two output stages that drive the external resolvers. The input signal is phase-shifted +45° and -45° and is amplified to produce the outputs which have a total phase difference of 90°.

See figure 6-133 for the schematic diagram of the 10-kc resolver driver. The 10-kc input signal is applied to pin 13 of the printed board connector and, thence, to the base of Q1 where the signal is developed across R1. Input stage Q1 is an emitter follower. The signal is developed in the primary of T1, with C1 and R2 serving as a bias network. The signal is coupled through T1 to phase-shift networks R3-C2 and C3, R4, R5, and R6. Network R3 and C2 produces a -45° phase shift in the signal which is applied to driver amplifier Q5 and Q4 at the base of Q5. Network C3, R4, R5, and R6 produces a +45° phase shift in the signal, which is applied to driver amplifier Q2 and Q3 at the base of Q2. Potentiometer R6, in the +45° network, provides fine adjustment of the total phase shift so that exact quadrature (90° phase shift) can be maintained.

Driver amplifiers Q2 and Q3 and Q4 and Q5 are compound-connected as emitter followers to insure minimum distortion with maximum power transfer. The +45° signal is applied to the base of Q2 and the output is developed in one of the external resolver windings. The -45° signal is applied to the base of Q5 and the output is developed in the other external resolver winding. Emitter voltage for Q3-Q4 is supplied through the resolver-common connection. Networks C4, R8, and R9 and C5, R10, and R11 are the bias networks of Q3 and Q4, respectively. Adjustment is provided by potentiometer R10 so that the output signals from Q3 and Q4 will be of the same amplitude. Output transformer T2 bridges between the resolver outputs and couples out the 10-kc reference signal.

e. PULSE RATE GENERATOR. - Loran-C transmitting station groups each have a discrete pulse repetition rate so that one station group can be distinguished from another. The Loran-C receiver must be capable of generating these pulse rates. The pulse rate generator in the receiver has two front panel rate selector controls, the BASIC REPETITION RATE and the SPECIFIC REPETITION RATE. There are 48 possible pulse rates from which one rate at a time can be selected. The longest pulse rate has a time interval of 100,000 microseconds while the shortest pulse rate has a time interval of 29,300 microseconds. The total combination of rates is made up of six basic rates and eight specific rates. The six basic rates differ by increments of either 20,000 or 10,000 microseconds. The eight specific rates progress in 100-microsecond increments.

In order to establish the receiver pulse rates, a highly stable 50-kc signal source provides 20-microsecond pulses for the basic counter. The 50-kc signal is divided by 5 to produce highly stable 100-microsecond pulses for the specific counter. Each 20-microsecond pulse applied to the basic counter causes a change of one binary number generated by the counter. As an example, the number 500 represents a time of 10,000 microseconds, 501 represents 10,020 microseconds, and so on. Refer to table 4-2 for the complete set of pulse rate codes and time intervals.

A basic count is selected by a diode matrix connected to the binary outputs of the basic counter. A complete matrix that would be capable of selecting any one of the total possible binary combinations of a 13-stage counter would require 8192 separate selector lines. Only six selector lines are needed in this system since only six basic selections are made. A trunked matrix scheme is used in the Loran-C receiver. The trunked matrix is made up of a complex switch and only one selector line. This system reduces the number of diodes used to a minimum.

Discussion of the entire 48 possible rates would be quite lengthy. For the sake of brevity, only one of the basic rates is explained in the following discussions. For example, the S basic rate will be assumed. The basic counter matrix produces an output when the counter reaches the number 2465 or 49,300 microseconds. With the specific rate selector set in the 7 position, the specific counter is not brought into use and the resulting pulse rate (S-7) is 49,300 microseconds. Each step of the specific rate selector, from seven to zero, adds 100 microseconds to the basic count selected. Consequently, rate S-6 produces a rate interval of 49,300 plus 100 or a total of 49,400 microseconds. Rate S-5 produces a rate interval of 49,300 plus 200 or a total of 49,500 microseconds, and so on with S-0 producing a rate interval of 50,000 microseconds. Any other discrete rate is produced in a similar manner.

Figure 4-25 is a simplified block diagram showing the signal path in the pulse rate generator.

An analysis of the signal paths in the pulse rate generator will facilitate its discussion. First, the S-7 pulse rate (49,300 microseconds) should be studied. The master oscillator 100-kc output is applied through the MC and ME resolvers to a squaring amplifier. The resulting 100-kc square wave is applied to the slew gate and the divide-by-2 toggle. The monostable multivibrator is not active at this time, so the 100-kc input is blocked and the 50-kc signal is passed through the slew gate and applied to the basic counter. When the basic counter reaches the number that corresponds to 49,300 microseconds (2465), the diode matrix connected to the counter produces an output that is applied to the specific gate. The specific counter is set in the 7 position and its diode matrix produces an output that is also applied to the specific gate. The gate toggle remains stable and the basic counter output is passed to the reset and trigger blocking oscillator that produces an output. This output is

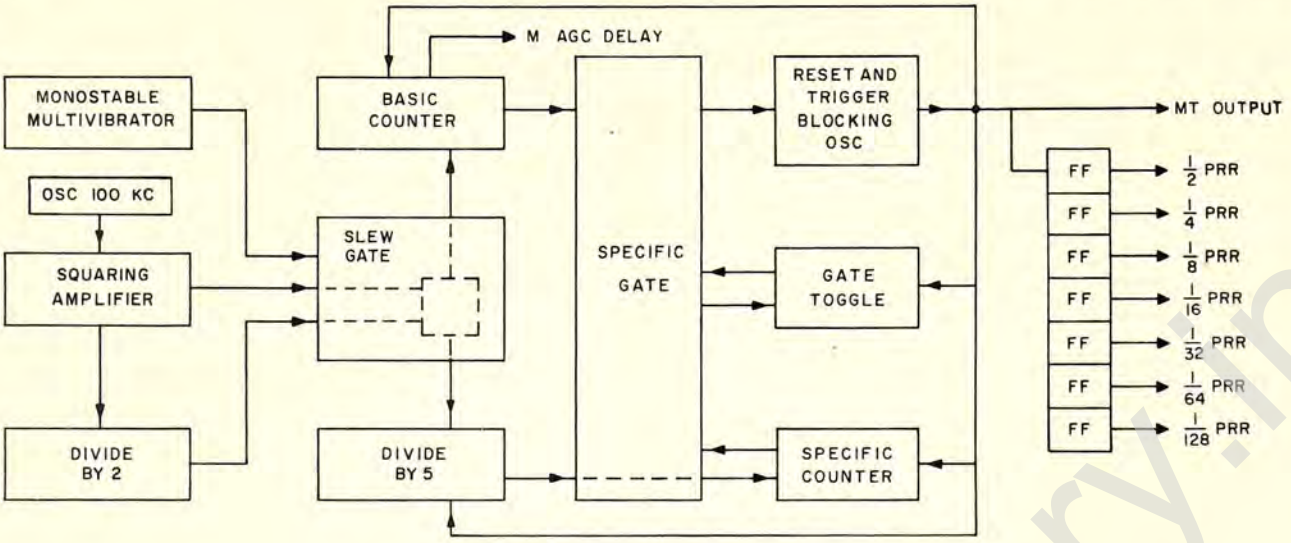


Figure 4-25. Pulse Rate Generator, Block Diagram

used to reset the pulse rate generator and to produce the master trigger for the Loran-C receiver.

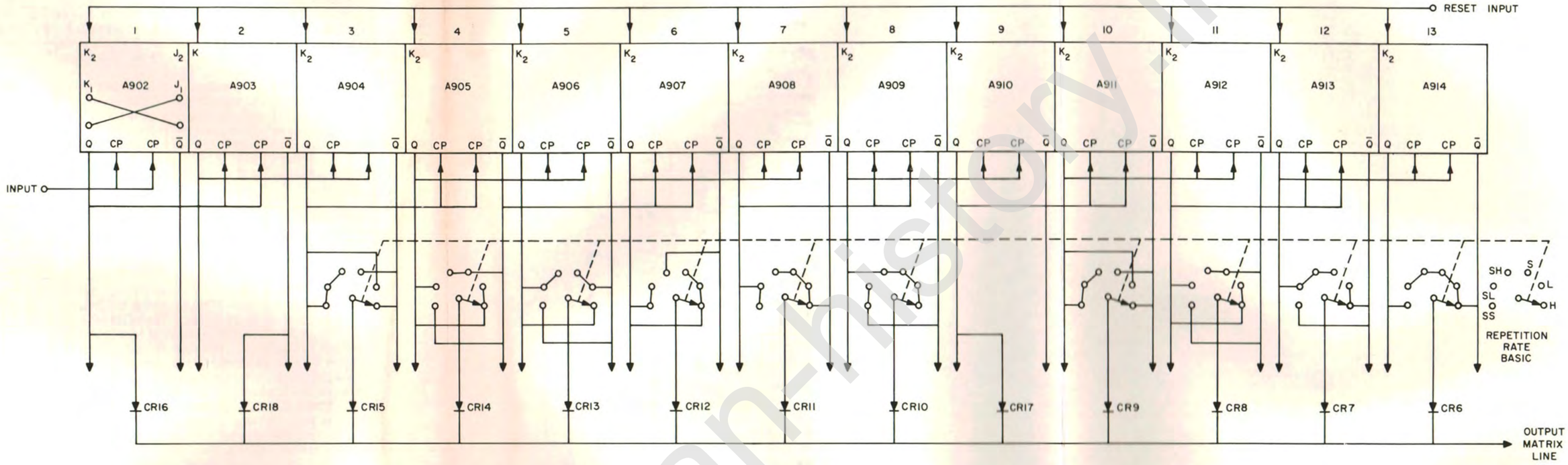
For the second example, the S-0 pulse rate (50,000 microseconds) should be studied. The 100-kc output of the squaring amplifier is applied to the slew gate along with the 50-kc signal. The monostable multivibrator is inactive, which blocks the 100-kc and passes the 50-kc signal. The 50-kc signal (20-microsecond pulses) is applied to the basic counter, which produces an output from its diode matrix at 49,300 microseconds. The specific counter does not produce an output at this time and the basic counter output is blocked in the specific gate. The basic counter output changes the state of the gate toggle, which allows the divide-by-5 output (10 kc) to pass through the specific gate. The divide-by-5 output is a series of pulses, 100 microseconds in duration. The specific counter is activated and produces an output after seven pulses are applied (700 microseconds). The specific counter output is applied to the specific gate, is allowed to pass through, and triggers the reset blocking oscillator. The receiver master trigger is produced and the counters and the gate toggle are reset.

For the third example, the action of the monostable multivibrator should be studied. Two front panel controls, RIGHT slew and LEFT slew, control the function of the slew multivibrator. Another front panel control, SEARCH SPEED, determines the frequency at which the monostable multivibrator can be activated. The speed control determines the rate at which the monostable multivibrator will operate when one of the slew buttons (RIGHT or LEFT) is actuated. The slew SEARCH SPEED control selects the output of a 5-stage divider or it selects the MTS (master time shared) gate directly. Consequently, the monostable multivibrator can be triggered at the same rate as the pulse repetition rate or it can be triggered at 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, or 1/128 of the pulse rate. Each of these trigger rates produces a successively slower slew rate. The slew LEFT control causes the monostable multivibrator to block, or delete, one 20-microsecond pulse on its way to the basic counter which effectively lengthens the pulse rate by 20 microseconds. The slew RIGHT control substitutes two 10-microsecond pulses for one normal pulse going to the basic counter, which effectively shortens the generated pulse rate. When viewed on the indicator scope of the Loran-C receiver, the received signal appears to move to the right (or to the left) with respect to the signal from the pulse group generated within the Loran-C receiver.

(1) BASIC COUNTER. - See figure 4-26. The basic counter consists of 13 toggle circuits connected in cascade. The Q and $\bar{Q}$ outputs from the toggle circuits are brought out, through diodes, to one common line, thereby making the basic counter a trunked matrix, as defined in paragraph 4-2*a*(5) and shown in figure 4-8. The BASIC REPETITION RATE switch selects the outputs of the counter stages as needed to sense the desired time delay corresponding with the proper binary count. The diodes from the toggle circuits effectively form an AND circuit, so that all 13 diodes must be -6 volts before there is a -6-volt output.

The toggles are connected within themselves so that the Q output of the toggle is connected to K1 and the $\bar{Q}$ output is connected to J1. This arrangement of the toggles means that the Q output of each toggle is connected to both the CP inputs of the following stage. The counter input (50 kc) is applied to the CP and inputs of the first toggle. By selecting the desired output from each toggle, the following basic rates may be selected.

RATE	TIME	DECIMAL	BINARY
H7	29,300	1465	0 0 1 0 1 1 0 1 1 1 0 0 1
L7	39,300	1965	0 0 1 1 1 1 0 1 0 1 1 0 1
S7	49,300	2465	0 1 0 0 1 1 0 1 0 0 0 0 1
SH7	59,300	2965	0 1 0 1 1 1 0 0 1 0 1 0 1
SL7	79,300	3965	0 1 1 1 1 0 1 1 1 1 1 0 1
SS7	99,300	4965	1 0 0 1 1 0 1 1 0 0 1 0 1



RATE	TIME IN USEC	DECIMAL NUMBER	BINARY NUMBER
H7	29300	1465	0 0 1 0 1 1 0 1 1 1 0 0 1
L7	39300	1965	0 0 1 1 1 1 0 1 0 1 1 0 1
S7	49300	2465	0 1 0 0 1 1 0 1 0 0 0 0 1
SH7	59300	2965	0 1 0 1 1 1 0 0 1 0 1 0 1
SL7	79300	3965	0 1 1 1 1 0 1 1 1 1 1 0 1
SS7	99300	4965	1 0 0 1 1 0 1 1 0 0 1 0 1

NOTES:
1. ALL Q OUTPUTS ARE ONE AND $\bar{Q}$ OUTPUTS ARE ZERO IN THE BINARY NUMBERING SYSTEM
2 SWITCH WAFERS ARE SHOWN VIEWED FROM FRONT

Figure 4-26. Basic Counter and Basic Repetition Rate Switch

The reset pulse for the basic counter is applied at the time of the master trigger (MT) to the K2 inputs of all 13 stages simultaneously.

Notice that the diodes connected to the matrix line may be switched to select either the Q or $\overline{Q}$ outputs of the various counter stages. Notice, also, that the diodes associated with toggles 1, 2, and 9 are not switched. This is because the output from these toggles is the same for each of the six basic rates. By comparing the binary number with the switch connections, it can be seen that the Q output represents a 1 in the binary numbering scheme and $\overline{Q}$ represents a 0. Toggle 1 and CR1 correspond to the units digit (right side) of the binary number.

Assume the master input signal of 50 kc is counting for the S7 rate. At the time of the 2465th count, the matrix line is released and a master trigger is produced. At the time of the master trigger (MT), the counter is reset and starts to count again. Consequently, when the S7 rate is selected, a master trigger is produced at the repetition rate of 49,300 microseconds.

(2) SPECIFIC GATE (A931). - The specific gate circuit operates in conjunction with several other circuits in the pulse rate generator section of the receiver. Its primary function is to sense the outputs of the basic counter and the specific counter and to produce an output signal that occurs at the selected pulse rate interval, ultimately producing the master trigger (MT) within the receiver. The master timing information in the receiver is derived from the 100-kc transistor oscillator. The specific gate circuit is associated with 20-microsecond (50 kc) and 100-microsecond (10 kc) signals applied to the basic and specific counters, respectively. By selecting the desired pulse rate, the counters sense the timing signals and produce outputs applied to the specific gate. For example, the S-7 rate has a time interval of 49,300 microseconds, and the S-6 rate has a time interval of 49,400 microseconds. The specific gate signal sequence for the S-7 rate occurs in this manner:

1) The basic counter output from the matrix is -6 volts.
2) The specific counter output from the matrix is -6 volts.
3) The output gating stage (Q2) passes negative-going pulses to the blocking oscillator to produce MT.

The specific gate signal sequence for the S-6 rate occurs in this manner

1) The basic counter output from the matrix is -6 volts.
2) The specific counter output from the matrix is 0 volt.
3) The basic gate (Q1) triggers the gate toggle which opens the 10-kc gating transistor (Q3) and closes the output gating stage (Q2).
4) The 10-kc signal is applied to the specific counter.
5) The specific counter matrix produces an output after 100 microseconds.
6) The specific counter matrix output opens the output gating stage (Q2).
7) A negative-going signal is applied to the blocking oscillator to produce the MT and to reset the counter and specific gate circuits.

It can be seen that the specific gate circuit accepts a number of signals, all associated with the master trigger time interval, and senses the proper combination of these signals to ultimately produce the master trigger (MT) in the receiver. For this discussion, the XTH and YTH toggle inputs to the specific gate will not be considered since these functions are used only during the Master Multiple function of the Station Selector Switch.

See figure 6-130 for the schematic diagram of the specific gate. Assume the S-7 rate is selected, and observe the input levels as shown in figure 4-27 below. First, observe the input signal levels at time (1). This is just before the counter has reached the designated number (2465) or 49,300 microseconds and the basic matrix produces its output of -6 volts. At time (2), the basic matrix level goes to -6 volts and is applied to the base of Q1. This level normally would appear at the emitter of Q1, however, the 50-kc signal is at a level of 0 volt at time (2). This is true for all of the seven basic rates. The emitter of Q1 is clamped to a level of 0 volt through CR1 while the input from the toggle gate is at a level of 0 volt.

Also at time (2), the specific counter matrix is ready to go to a level of -6 volts, but the specific matrix line is now clamped at a level of 0 volt by the 50-kc signal applied to CR3. At time (3), the 50-kc signal goes to a level of -6 volts which releases the specific matrix line to a level of -6 volts. At this time, the input from the specific matrix is applied to the base of Q2, and this level of -6 volts appears at the emitter of Q2 as a negative-going signal. A negative-going signal is required to fire the reset blocking oscillator that produces the actual trigger (MT) pulse. The MT pulse also acts as a reset function for the entire pulse rate generator section, and the conditions observed at time (1) are again produced. The actual time from the negative-going output of the specific gate circuit to the time of reset is extremely short, in the order of 0.5 to 1.5 microseconds. In figure 4-27, the time between time (3) and the reset is expanded to show what takes place. It is not the same time scale as the period from time (1) to time (3).

For any specific rate other than specific rate 7, a different sequence of events takes place at the inputs to the specific gate circuit. See figure 4-28, which shows the time relationship of input and output signal levels for the specific gate circuit. Time (1) is just before the time that the basic counter reaches the count of 2465 (49,300 microseconds). At time (2), the basic matrix line goes to a level of -6 volts. However, since the specific matrix line is clamped to a level of 0 volt by the specific counter, the negative-going signal at the emitter of Q1 is not present at the base of Q2, and no output from the specific gate results. At time (3), the negative-going 50-kc signal is blocked by CR3 and cannot appear at the base of Q2, therefore, the 50-kc signal does not cause an output at this time. At time (4), the positive-going signal from the basic matrix line is applied from the emitter of Q1 to the gate toggle. The output from the gate toggle goes from a level of 0 volt to -6 volts and is applied to the cathode of CR4. The base of Q3 is

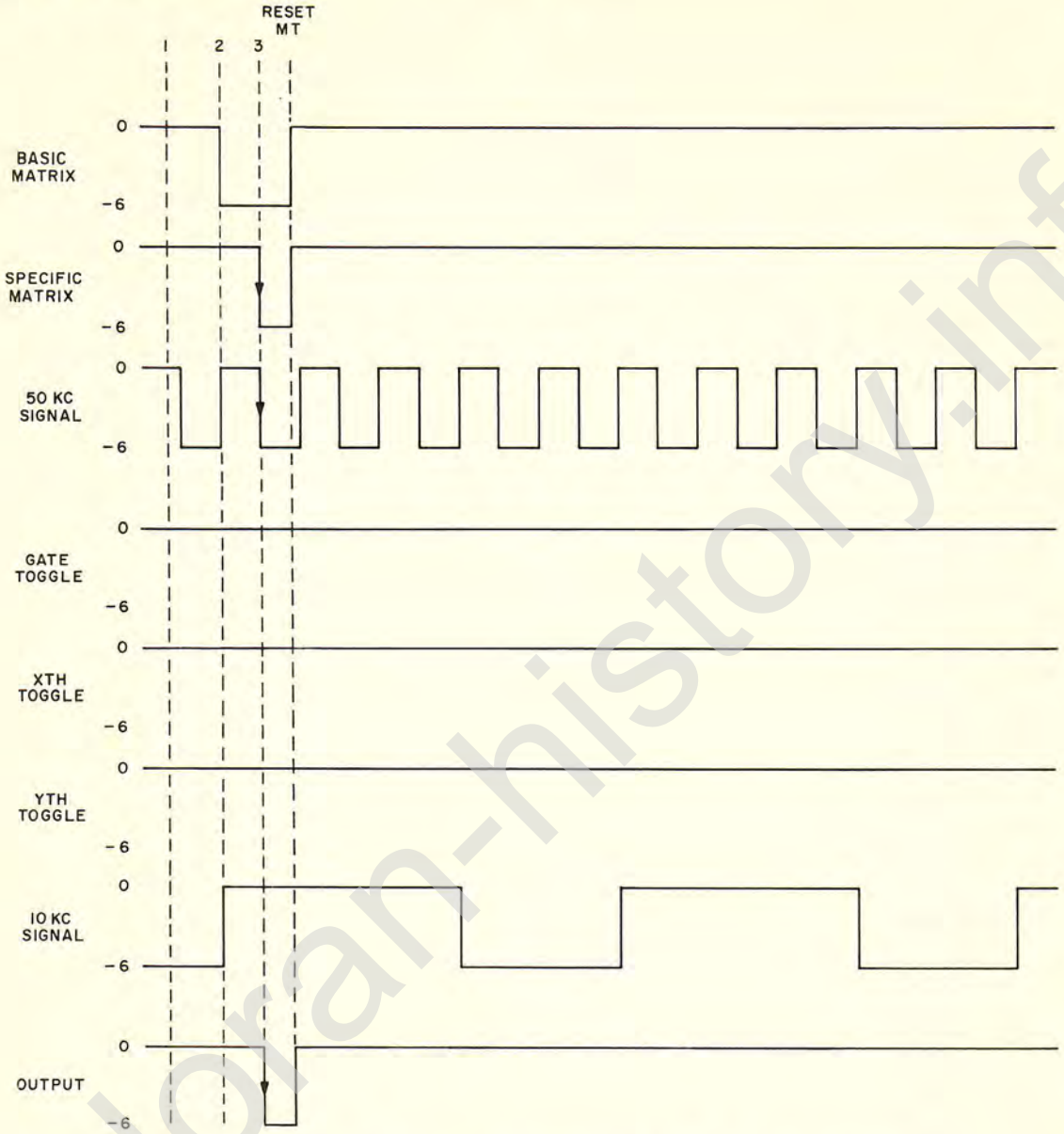


Figure 4-27. Specific Gate Waveshapes, S-7 Rate (49,300 microseconds)

now opened and will accept the 10-kc signal applied to the anode of CR8. The 10-kc signal is applied to the base of Q3 through CR8 and is coupled out of the specific gate circuit to the input of the specific counter. At time (5), the specific counter matrix line tries to release to a level of -6 volts after two counts, or 200 microseconds. However, the 50-kc signal goes to a level of 0 volt at time (5) and blocks the release of the specific matrix line. At time (6), the 50-kc signal goes to -6 volts and the specific matrix line is released to a level of -6 volts. This negative-going signal is applied to the base of Q2 and produces a negative-going signal at its emitter. This negative-going signal is applied to the reset blocking oscillator and produces the MT, causing the reset process to take place. At reset time, all input conditions to the specific gate circuit return to the condition shown at time (1).

The signals applied from the XTH and YTH toggles are noted. These toggles change state only when the Station Selector Switch is in the Master Multiple position. The XTH and YTH toggles are activated by an external signal that causes them to change state and apply negative-going signals through C1 and C2, respectively. These negative-going signals are differentiated by C1 and R4 or C2 and R5, are applied to diodes CR5 or CR7, and produce negative-going signals at the XTH and YTH output terminals of the specific gate circuit, respectively. The purpose of this provision in the specific gate is to allow the timing system to be reset if the receiver happens to lock in out-of-step with the received signal; that is, the

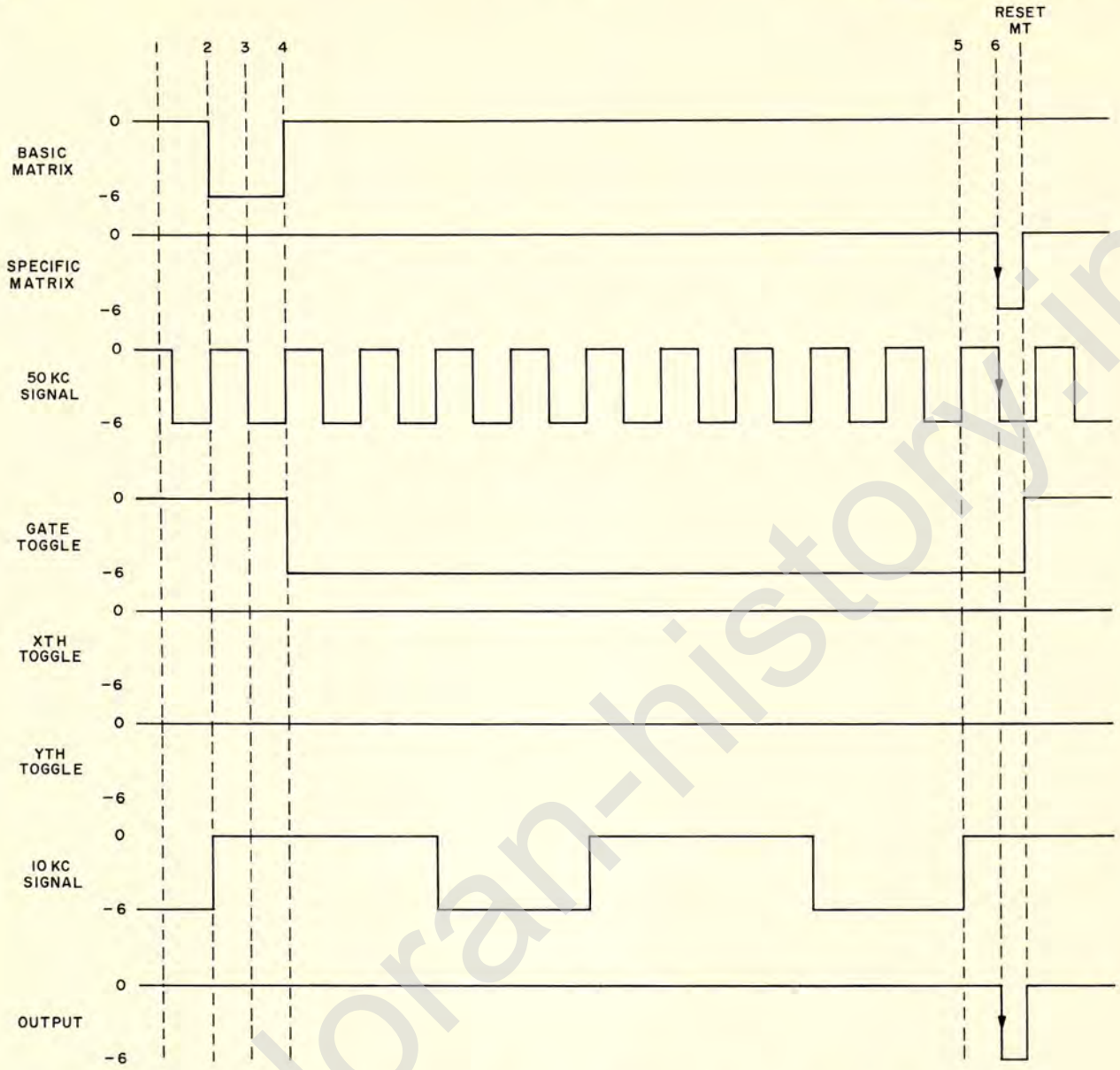


Figure 4-28. Specific Gate Waveshapes, S-5 Rate (49,500 microseconds)

master pulse group locked in on a slave pulse group.

(3) SPECIFIC GATE TRIGGER TOGGLE (A915). - The gate toggle is a standard toggle circuit, which functions in conjunction with the specific gate circuit. See figure 6-9. Its circuit action is described in paragraph 4-2*d*(1). The gate toggle has no special characteristics but functions only as a bistable multivibrator (flip-flop) in this application.

(4) SPECIFIC COUNTER AND MATRIX. The specific counter is made up of three standard toggle circuits connected in the same manner as the toggle circuits of the basic counter. The only basic difference between the specific counter and the basic counter is the application of the sensing matrix associated with the counter. The specific counter outputs (Q and $\overline{Q}$) are applied to a trunked matrix. This matrix is wired so that any of the possible binary combinations from the counter may be sensed. Since the applied frequency is 10-kc, the period between input pulses is 100 microseconds. Consequently, each successive binary produced in the specific counter represents a time increment of 100 microseconds. Figure 4-29 is a simplified block diagram of the specific counter and the specific matrix switch.

(5) RESET BLOCKING OSCILLATOR (A932).

(a) GENERAL. - The reset blocking oscillator produces a reset pulse for the counters in the

produced in T1 when Q2 cuts off. Filter capacitors C2 and C4 are placed in the circuit to prevent pulse spikes from being fed back into the power supplies.

(6) SEVEN STAGE DIVIDER. - The 7-stage divider circuit consists of seven standard toggle circuits. They are connected so that the input to each stage comes from the Q output of the preceding stage. The seven toggles are connected in cascade in the same manner as those of the basic counter with respect to the inputs and the cross connections from Q to K1 and $\overline{Q}$ to J1.

The action of the 7-stage divider is quite simple in that each toggle divides its input by 2. The input to the divider is the reset trigger from the blocking oscillator which is coincident with the master trigger (MT) time. The Q outputs of the seven toggles are selected by the slew SPEED SEARCH CONTROL switch to activate the slew monostable multivibrator. Slew speed is determined by the frequency of the slew trigger applied with respect to the master trigger repetition rate. The outputs from the 7-stage divider are 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, and 1/128 times the master trigger repetition rate which is generated in the pulse rate generator of the receiver.

(7) INDICATOR SWEEP-TIME DETERMINATION. - Diodes CR1050 through CR1063 form a gating circuit which applies a signal to the indicator to allow the scanning time to be sufficiently long so that all nine pulses of the master signal may be viewed. If the Loran-C signal is operating so that there are 1000 microseconds between the pulses, the scanning duration will be at least 8960 microseconds long. If the Loran-C signal is operating on 500-microsecond pulse spacing, the scanning duration will be a minimum of 4480 microseconds. The output signal from the circuit is also supplied to the agc toggles so that the agc level can be maintained at the proper value during the entire length of the master signal.

The change of connections to correspond with the pulse-spacing option of operation may be made as shown in figure 5-8 as explained in note 7 of the figure. A simplified schematic diagram of the diode connections is shown in figure 4-30. As explained in the discussion on binary counters, paragraph 4-2*a*(3), the complementary Q and $\overline{Q}$ outputs may be considered as representing logic 1 and logic 0, respectively, in the binary system.

The entire basic counter comprises 13 binary stages consisting of toggles A902 through A914. The output selected from each toggle represents a digit of a binary number which counts in 20-microsecond increments. The three least significant digits of the counter are the outputs from A902, A903, and A904. Diodes are not connected to these toggles but are connected to each of the other nine toggles as shown in the simplified diagram.

The decimal number that represents a sweep trace long enough for viewing 1000-microsecond pulse spacing is 448 (8960 microseconds). The decimal number that represents a sweep long enough for viewing 500-microsecond pulse spacing is 224 (4480 microseconds). In the binary scheme, these numbers are, respectively, 0 0 0 0 1 1 1 0 0 0 x x x and

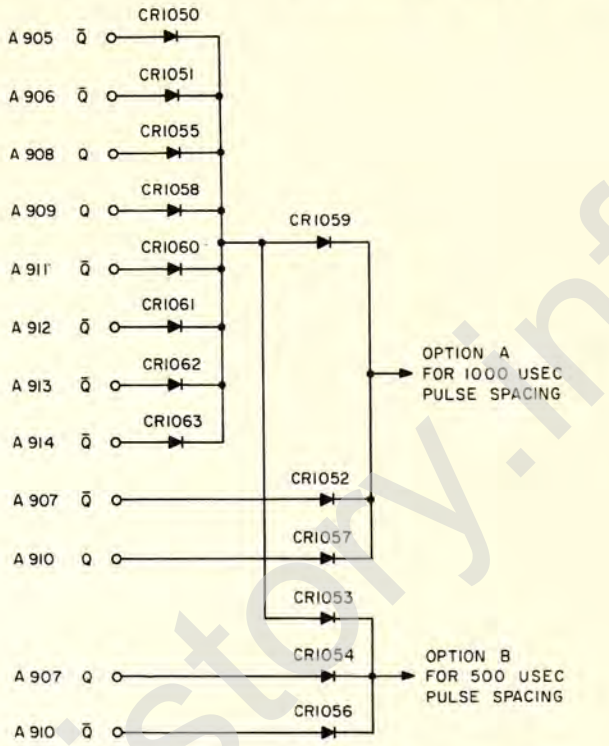


Figure 4-30. Diode Connections for Indicator Sweep Time Determination Circuit

0 0 0 0 0 1 1 1 0 0 x x x. The (x) represents outputs from the first three counters, the outputs of which are not connected to the circuit and are therefore undetermined. As may be noted, the two optional binary numbers differ only at two digits. To take advantage of this and to minimize the number of diodes, three AND gate arrangements are used. Outputs representing digits that are common to the two numbers are applied to the first AND circuit. For each option, the output of this first AND circuit is subsequently applied to another AND circuit along with the proper outputs from the two remaining digit stages to complete the desired binary number. For the higher of the two numbers (448) this is the $\overline{Q}$ output from A907 and the Q output from A910. For the shorter of the numbers (224) this is the Q output from A907 and $\overline{Q}$ output from A910.

Since the three least significant digits are not part of the count, the longest time would be the case where all three outputs were logic 1's, or an addition of 7 (1 + 2 + 4) to each of the equivalent decimal numbers. This makes the longest sweep possible for option A to be 9100 microseconds and the longest sweep possible for option B to be 4620 microseconds.

f. COINCIDENCE DETECTOR.

(1) GENERAL. - The basic purpose of the coincidence detector is to produce the X and Y slave delay triggers in the receiver. These triggers later produce the X and Y timing information, which establishes the time-shared sequence of the receiving system. See figure 4-31 for a simplified block diagram of the coincidence detector signal flow. The

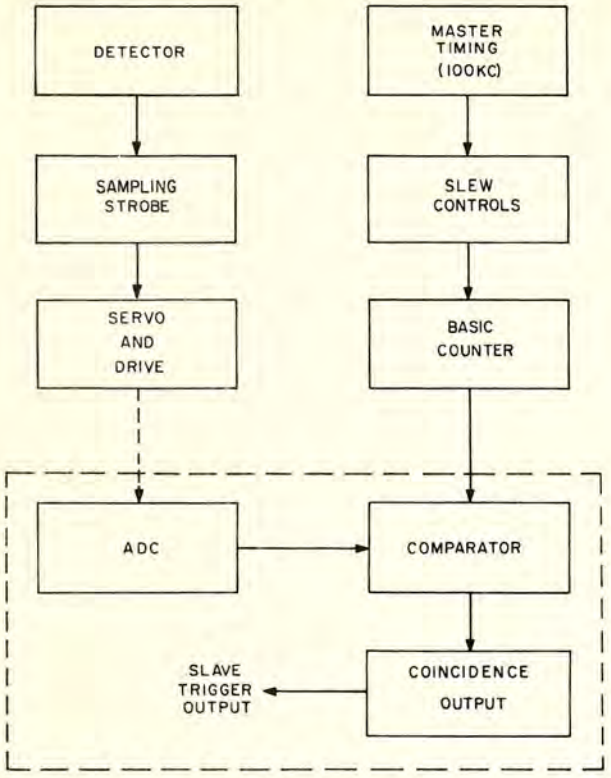


Figure 4-31. Coincidence Detector, Simplified Block Diagram

basic counter provides digital information for the coincidence detector comparator circuits which consist of 13 identical circuits. These circuits produce an output when the binary number from the basic counter is coincident with the binary number produced by the X and Y count encoders (ADC). Since the basic counter counts in increments of time (20 microseconds), X and Y trigger time is derived from this timing source. The ADC (analog-to-digital converter) converts shaft position to binary information, as determined by servomotors associated with each of the slave trigger loops.

Digital information is fed to the comparator circuits from the basic counter and from the ADC encoders. The basic counter circuit counts from zero time with each master trigger. However, the count encoders remain relatively close to the same position while searching, and remain locked-on when the generated timing sequence is coincident with the received timing sequence. In general terms, the count encoder supplies a reference input to the comparator circuits, and the basic counter supplies the variable input to the comparators. The comparator circuits sample the changing time information from the basic counter as it counts from zero time and produce a trigger output when the reference time and variable time coincide. When the delay trigger produced by the coincidence detector does not occur at the same time as the received delay, this time difference is detected by the detector and sampling strobe. The detected time difference is supplied as error voltage to the servo, which changes the reference delay time generated by the ADC encoder. When error exists, the generated delay time is changed until the generated delay time and the received delay time are coincident.

The coincidence detector contains two separate channels one for X delay time and one for Y delay time. Both the X and Y delay times are sampled and compared to the same time base generated by the basic counter. Since the basic counter produces timing information which is coincident with the master signal from the transmitting station, it is evident that the X and Y delay times will maintain a high degree of accuracy with respect to the received master signal.

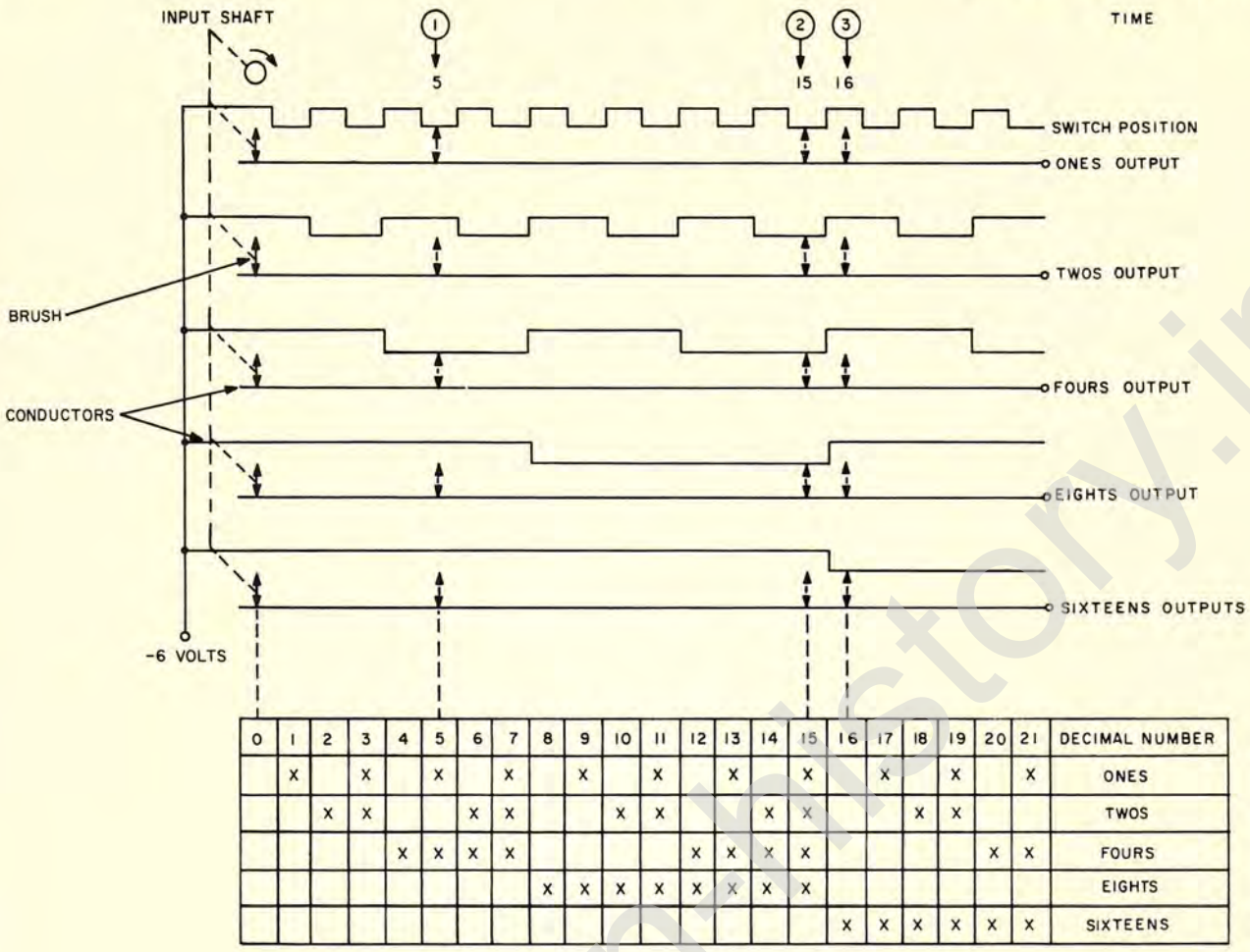
(2) ANALOG-TO-DIGITAL CONVERTER.

(a) GENERAL. - The analog-to-digital converter (ADC) is an electromechanical device which converts increments of mechanical rotation into electrical intelligence in the form of binary numbers. For an example, an ADC which is capable of producing binary numbers up to 36 would have an increment of 10° rotation for each decimal/binary equivalent. In the AN/SPN-30 receiver, the envelope delay readout, calibrated in microseconds, is derived from a drum-type mechanical counter which is mechanically coupled to an ADC unit.

A simplified diagram of a typical ADC is shown in figure 4-32 and the schematic diagram is shown in figure 6-173. As shown in the simplified diagram, an input of -6 volts is applied to each of the switch lines, and five outputs are taken from the slider lines of the ganged switches. As the switches advance from the left to right (actually the switch lines of the discs advance from right to left), various combinations of binary outputs will be obtained. In the table of figure 4-32, the notation X represents an output of -6 volts on the associated line (ones, twos, fours, etc.). These outputs may be compared to the decimal-to-binary table in paragraph 4-2*e* to show that the ADC outputs are equivalent to binary numbers.

With the switches in the zero position, all of the output lines are at a level of 0 volt. By advancing the switches (or discs) to position 5 (arrow 1) it can be seen that the outputs of -6 volts are present on the ONES and FOURS lines. The binary for 5 is 00101. When the switches are advanced to position 15 (arrow 2) the outputs of -6 volts are present on the ONES', TWOS', FOURS', AND EIGHTS', lines. The binary for 15 is 01111. When the switches are advanced to position 16 (arrow 3) an output of -6 volts is present on the SIXTEENS' line only. The binary for 16 is 10000. It can readily be seen that numbers of higher order can be generated by using more switch decks in the ADC.

The binary numbers used in the Loran-C receiver require that both the bit and the complement be present. It becomes necessary to establish both zero- and negative-voltage outputs for each binary digit. This is accomplished by using complementary switches to produce the digit bits (negative voltages) and digit complements (zero voltages) for each line. The actual ADC unit in the Loran-C receiver is capable of producing 8192 possible binary combinations for 64 revolutions of its drive shaft. That represents approximately 2.8° of shaft rotation for each digit.



0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	DECIMAL NUMBER
	X		X		X		X		X		X		X		X		X		X		X	ONES
		X	X			X	X			X	X			X	X			X	X			TWOS
				X	X	X	X					X	X	X	X					X	X	FOURS
								X	X	X	X	X	X	X	X							EIGHTS
																X	X	X	X	X	X	SIXTEENS

Figure 4-32. Analog-to-Digital Converter, Simplified Diagram

(b) DETAIL. - The operation of the analog-to-digital converter can best be explained by referring to the schematic diagram of figure 6-173. The analog information is applied to the circuit in the form of mechanical shaft position. The digit bit information is taken from the circuit of the even-numbered terminals of P2, terminal 2 being the least significant digit. The complementary digit information is taken from the odd-numbered terminals of P2, terminal 1 being the least significant digit complement.

In this system, a negative voltage (approximately between -12 and -8 volts) is one in the binary scheme, and a zero voltage is equivalent to zero. Zero voltage (count of zero) on a terminal of the ADC can be caused in two ways. One way is by the application of 0 volt. This is the technique used to apply 0 volt to the least significant digit of the ADC from the encoder driver. The other method for establishing 0 volt is by opening the circuit to the ADC output. This is done at the brush contacts and by diode placement. All of the zero-voltage outputs in the ADC circuit, other than the first, are established this way.

For an explanation of the drive bias on terminals C and O of the ADC, refer to the simplified schematic diagram shown in figure 4-33. The diagram shows the interconnection of the input stage to the encoder driver circuit and the connections of C and O on the plug of the ADC. When brush contact E1 in the ADC is closed, there is an effective divider which establishes a potential of approximately +8 volts at the input of the first transistor stage.

The base voltage of the transistor drops to about +3 volts when the circuit is open between C and O. An instantaneous voltage of approximately 12 volts would occur when the contact is closed again. But, Zener diode CR1 prevents the voltage at the top of the 20,000-ohm resistor from exceeding about +8 volts. Therefore, the difference in potential across the contacts at E1 will never exceed 5 volts. When E1 is closed, 0 volt (count of zero) appears on terminal 2 of P2 of the ADC, and approximately -8 volts (count of one) is applied to terminal 1 of P2. Zero voltage is applied to the encoder driver when the disc advances so that the brush on the drive disc is located opposite a space between the segments. This results in a large negative voltage (count of one) being applied to terminal 2 and zero voltage (count of zero) being applied to terminal 1 of the ADC.

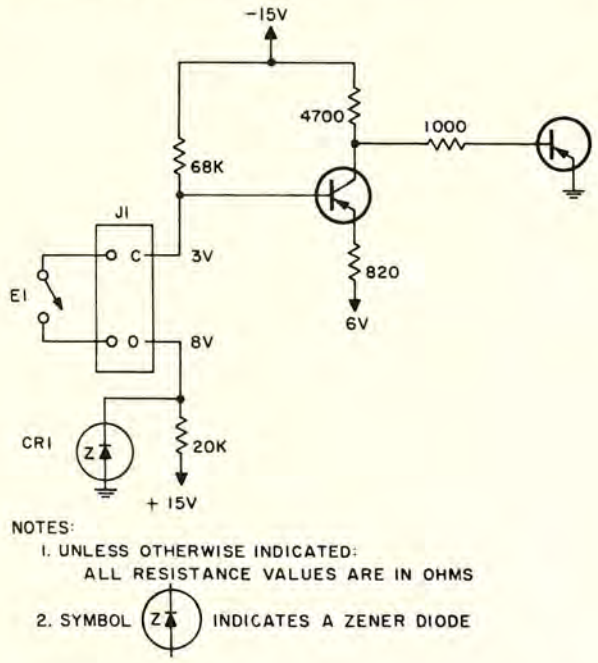


Figure 4-33. ADC-Encoder Driver, Interconnection of Drive Bias, Simplified Schematic Diagram

Notice that the first disc commutator spacing exactly corresponds to the commutator spacing of the drive disc. With the brushes placed in relation to the discs as shown on the schematic, the output on the digit bit side (left side) will be all 0' s, zero voltages; and the output on the digit complement side will be all 1' s, large negative voltages. To investigate the path for the negative voltage, as an example, study the path to terminals 3 and 5. The path starts at terminal 1 with the application of voltage from the encoder driver. It goes through brush contact E4, through the commutator segment, through the slip ring at E3 (to terminal 3 of P2), through diode CR3, through brush contact E8, through the commutator segment, through the slip ring at E7, to terminal 5 of P2. The negative voltage passes to the remainder of the odd numbered terminals of P2 in a similar progressive manner. Since there is a slight drop across the forward resistance of each diode, the voltage at terminal 25 of P2 is at a level of about - 8 volts. On the bit side, zero voltage is applied at terminal 2; therefore, no voltage is applied to any of the even-numbered terminals due to the open circuits.

For a mixing of voltages on the digit bit and the digit complement sides (for binary counts which include both 1' s and 0' s), investigate the first disc underneath the drive disc. When the shaft rotation positions the commutator segment shown under E5 so that it is under E4, there is a path to slip ring contact E6 from terminal 4 of J1. Since the commutator is selected to supply a negative voltage to terminal 4, the commutator segment feeding terminal 2 is not selected, resulting in a zero voltage at this terminal.

There is no possibility of the voltages progressing up the diagram (towards the least significant digits) but only toward the most significant digits. The back path is blocked by the diodes even when a commutator segment shorts two brush contacts together; for example, when a commutator segment is across both E8 and E9.

(3) ENCODER DRIVER (A1215).

(a) GENERAL. - The purpose of the encoder driver circuit is to produce ones digit and ones complement signals from the two levels of the input signals applied from the commutator ring (C and O connections) of the X and Y analog-to-digital converters (ADC). The encoder driver printed board contains two identical circuits, one for the X-ADC unit and one for the Y-ADC unit. The outputs of the encoder driver circuit are applied to the ones digit and ones complement connections of the ADC units which then produce the remaining 12 pairs of digital information to be applied to the comparator circuits.

(b) DETAIL. - Refer to figure 6-139, the schematic diagram of the Encoder Driver Card. Two complete drivers are included on each card. The circuits of transistors Q1 through Q4 comprise the X-ADC driver; the circuits of transistors Q5 through Q8 comprise the Y-ADC driver. Since the circuits are electronically identical the following description will consider only the X driver.

Basically the circuit consists of a Schmitt trigger (Q1, Q2) followed by an amplifier (Q3) and an inverter (Q4). Input to the circuit can be +6 volts or the input can be an open circuit. Commutator noise from the encoder is usually present, but has no effect on the trigger circuit. When the open circuit condition is present at the input, transistor Q1 is biased so that it conducts heavily. With Q1 in the highly conductive state, Q2 is cut off, and the potential at the base of Q3 is highly negative. This causes Q3 to conduct and produce a potential very close to 0 volt at the collector. The collector potential is the digit output and appears at terminal 10 on the plug.

When +6 volts is applied to the input terminal from the encoder, transistor Q1 stops conducting and transistor Q2 conducts heavily. When this occurs, the potential at the collector of Q2 approaches +6 volts and transistor Q3 is cut off. With Q3 not conducting, the potential at terminal 10 of the plug approaches -15 volts. Transistor Q4 is a simple inverter which makes the output at terminal 9 the complement of the output at terminal 10.

(4) COMPARATOR (A1201-A1213).

(a) GENERAL. - The purpose of the comparator circuit is to detect coincidence between two sets of input signals. These input signals are applied as digit and complement signals from the basic counter (Q and $\overline{Q}$) and from the ADC units (N and $\overline{N}$). There is a separate comparator circuit for each of the 13 digits (ones, twos, fours, eights, etc.) from the counter and the ADC. The X outputs of all 13 comparators are connected to a common source of - 6 volts, and the Y outputs of all 13 comparators are connected to a common source of - 6 volts (coincidence output). Also included on the printed board are

three indicator lamps which show the presence of input signals, X-ADC and Y-ADC, from the counter.

(b) DETAIL. - See figure 6-137 for the schematic diagram of the comparator circuit. The transistors are basically differential amplifiers with the collectors of Q1 and Q2 and Q3 and Q4 connected as pairs. A differential amplifier allows a variable signal to pass to the output depending on the level of another independent variable. Digit signals (Q and N) are applied to Q1 and Q3, and complement signals ($\overline{Q}$ and $\overline{N}$) are applied to Q2 and Q4. The desired output (-6 volts) is established when inputs Q and N are equal at the same time inputs $\overline{Q}$ and $\overline{N}$ are equal. Notice that when Q is at 0 volt, $\overline{Q}$ is at -6 volts; and when N is at 0 volt, $\overline{N}$ is at -6 volts.

First, the circuit conditions of Q1 - Q2 should be considered when Q=N and $\overline{Q}$=$\overline{N}$. It is assumed that the N and Q inputs to Q1 are both at a level of 0 volt. The emitter of Q1 is held at 0 volt by the input applied. The base of Q1 is at a level of approximately +2 volts, due to the voltage division of R1 and R2; and Q1 is cut off. The emitter of Q2 is held at a level of -6 volts. The base of Q2 is at a level of approximately -2 volt due to the voltage division of R3 and R4; and Q2 is cut off. Since both Q1 and Q2 are cut off, there is no conduction through CR1; and the output line is at a level of -6 volts. The X output line is clamped to -6 volts in the coincidence output when neither Q1 nor Q2 are conducting.

Next, the circuit conditions of Q1 and Q2 are considered when Q is not equal to N. It is assumed that the Q input is 0 volt and the N input is -6 volts. When Q is 0 and N is -6 volts, $\overline{Q}$ is -6 volts and $\overline{N}$ is 0 volt. The emitter of Q1 is held at 0 volt by the applied input. The base of Q1 is at a level of approximately -2 volts, due to the voltage division of R1 and R2; and Q1 is driven into hard conduction. This lowers the collector level to approximately 0 volt, the level of the emitter. Diode CR1 conducts and clamps the output line to 0 volt. When the circuit conditions of Q2 are examined under these input conditions, it is seen that the emitter of Q2 is held at -6 volts by the $\overline{Q}$ input, and the base of Q2 is at +2 volts due to the voltage division of the $\overline{N}$ input across R3 and R4. With its base at +2 volts, the transistor is cut off. However, the collector is held at 0 volt because of the conduction of Q1 through CR1.

Table 4-5 lists the possible input combinations of circuit conditions for the X comparator (Q1 and Q2).

TABLE 4-5. POSSIBLE INPUT COMBINATIONS OF CIRCUIT CONDITIONS FOR THE X-SLAVE COMPARATOR

INPUT SIGNALS	TRANSISTOR CONDITION	X OUTPUT LINE
N -6	Q1 Cutoff	
Q -6		
$\overline{N}$ 0		-6 volts
$\overline{Q}$ 0	Q2 Cutoff	
N 0	Q1 Cutoff	
Q 0		
$\overline{N}$ -6		-6 volts
$\overline{Q}$ -6	Q2 Cutoff	
N 0	Q1 Cutoff	
Q -6		
$\overline{N}$ -6		0 volt
$\overline{Q}$ 0	Q2 Conducting	
N -6	Q1 Conducting	
Q 0		
$\overline{N}$ 0		0 volt
$\overline{Q}$ -6	Q2 Cutoff	

When the comparators of the coincidence detector are considered as a group, the output line will be clamped to a level of 0 volt when any one of the comparator circuits has unlike signals applied. Consequently, since both the digit and complement are compared for each of the 13 stages of the counter, it is impossible to obtain a coincidence output which is erroneous or ambiguous. The sequence of events of the comparator circuits is shown below. Assume a period of 50,000 microseconds between master triggers, 15,000-microsecond delay to the X trigger, and 30,000-microsecond delay to the Y trigger.

1. The master trigger fires and the basic counter starts to count from zero time.
2. X-ADC is set for 15,000 microseconds and is applied to comparators.
3. Y-ADC is set for 30,000 microseconds and is applied to comparators.
4. The basic counter output reaches 750th count (750 x 20 microseconds).
5. The comparators release the X output line to -6 volts, and the X trigger is produced.
6. The basic counter continues to the 1500th count (1500 x 20 microseconds).
7. The comparators release the Y output line to -6 volts, and the Y trigger is produced.
8. The basic counter continues to count until the master trigger resets the timing circuits and the sequence starts again.

(5) COINCIDENCE OUTPUT (A1214). - The coincidence output plug-in printed board contains two identical circuits; one to produce an X coincidence output signal, and the other to produce a Y coincidence output signal. Each of the two circuits on the board has an input AND stage and an output stage. For purposes of discussion, only the X half of the board will be considered in detail.

See the schematic diagram, figure 6-138. Two inputs, the X comparator output line and a 50-kc square-wave signal, are applied to the X coincidence output circuit. Both the X comparator line input to the coincidence output circuit and the 50-kc square wave must be at -6 volts to produce an output. When the input from the X comparator is clamped to a level of 0 volt, the 50-kc signal is blocked by CR1; and no output from Q2 will result. When the input from the X comparator is released to -6 volts and the 50-kc signal goes to -6 volts, the base of Q1 is released and goes to a level of -6 volts. With its base at -6 volts, Q1 conducts; and the signal is developed across

R2 in the emitter of Q1. This signal is applied to the base of Q2 through network R3, R4, and C1. A negative signal on the base of Q2 causes it to conduct heavily and forces the level of the collector of Q2 to approach the emitter level of 0 volt. This positive-going (zero level) output has a duration of 10 microseconds.

Assume that the input from the X comparator is clamped to a level of 0 volt and the 50-kc input signal is blocked. The base of Q1 is now at a level of 0 volt and Q1 is cut off. Since Q1 is an emitter follower, this input signal will appear at the emitter of Q1. This signal is applied to the base of Q2 through network R3, R4, and C1, and the base of Q2 goes slightly positive. Transistor Q2 is cut off and its collector is clamped to -6 volts by R5 and CR2; and the XT output is now -6 volts.

The Y half of the coincidence output board operates in the same way. Both the Y comparator line input and the 50-kc signal must be at -6 volts to produce the YT output of 0 volt.

Combinations R3 and C1 and R8 and C2 are compensating networks which decrease the switching time of Q2 and Q4 and steepen the rise time of the respective output wave shapes.

g. CODE GROUP GENERATOR. - The code group generator section of the Loran-C receiver is made up of 19 printed board circuits that are in the lower section of the receiver drawer. The primary function of the code group generator is to produce the phase code information which is applied to the time-shared detector. While producing the phase code information, the code group generator section also produces several other time-shared signal functions. Among these are slew limit, strobe timing, and skywave guard strobe timing. A simplified block diagram is shown in figure 4-34.

The primary inputs to the code group generator are the M, X, and Y triggers and the master 10-kc, X-slave delay 10-kc, and Y-slave delay 10-kc signals. The M, X, and Y toggle boards initiate coding by translating the trigger pulses into time-shared gate waveforms. These toggles are part of a closed loop. That is, the toggles are turned ON by a trigger pulse that, in turn, allows a 10-kc signal to enter the generator. The 10-kc signal is processed and eventually turns OFF the same toggles. The time-shared gates (M, X, and Y) are approximately 7400 microseconds in duration for 1000 microsecond pulse spacing. The signal flow in the time-shared loop is as follows: (1) from the M, X, or Y toggle; (2) to the pulse group timing gate; (3) to the divide-by-10 circuit (or divide-by-5 circuit if operating on 500-microsecond timing); (4) to the code counter; and finally (5) feedback reset to the M, X, or Y toggle. It should be noticed in figure 4-35 that when the switch is in the 8 PULSE position, the reset pulse from the code counter is returned to all three toggles at the completion of the complete code count. However, in the SINGLE PULSE position, the trailing edge of the first toggle will reset the X toggle and Y toggle; and the trailing edge of the second toggle will reset the M toggle. The time-shared gates of the toggle circuits produced by the M, X, and Y toggles are used elsewhere in the receiver.

A second major signal flow path may be thought of as the phase code path. The time-shared gates (MTS, XTS, YTS) are combined with the group separation gates (1/2MT, $\overline{1/2MT}$) at the code logic circuit to produce a sequence of gates for the diode matrix input. For identification of the proper code and pulse groups, the system requires that M-1, S-1, M-2, and S-2 phase coding be generated within the receiver. The code logic circuit accomplishes this function and applies the information to the diode matrix. The diode matrix combines the code logic signals with the output from the code counter to produce the phase code signal. The phase code driver circuit then applies the phase code information, Phase Code and $\overline{\text{Phase Code}}$, to the detector circuit of the receiver.

The MTS, XTS, and YTS gates are also applied to the slew limit circuit and the strobe timing gate circuit. The slew limit functions to reverse the slave delay servo motors to prevent pulse group overlap. Since the signals are always received in the M-X-Y sequence, it is never necessary that X delay be larger than Y delay. Therefore, the automatic slewing of X is limited to the interval between M and Y, and Y automatic slewing is limited to the interval between X and M.

The strobe timing gate circuit produces the signals from which the actual strobe, or sampling, signals are derived. The strobe timing gate circuit is actuated by the monostable multivibrator and the time-shared gates so that the strobe time will fall at the desired portion (30-microsecond point) of the detection and sampling sequence.

The skywave time-sharing gate circuit function enables the receiver to detect the presence of skywave contamination at the detector. An erroneous delay readout would result if a skywave signal were sampled at the detector. Consequently, the skywave time sharing gate circuit provides a method for detecting the presence of skywave signals and for warning the operator by means of a front panel light of possible skywave contamination of the received signal. This is accomplished by slewing ahead of the detected (the erroneous skywave) waveform by 45-microseconds so as to detect the presence of the desirable ground wave.

(1) M, X, AND Y TOGGLES (A1308-A1310). - The M-X-Y toggle circuit is a combination of three basic toggle boards connected as shown in the partial block diagram, figure 4-36. Only the necessary connections for the simplified operation of the circuit are shown. This circuit combines the trigger pulses for the master, X-slave delay, and Y-slave delay so that the timing sequence of the generated code groups is established.

See figure 4-37 for a diagram of the time relationships of the wave shapes involved in the M-X-Y toggle circuit. Since the three (M, X, and Y) operate in sequence, only the time sequence of the master trigger will be discussed. The time sequence for the X and Y trigger operates in a similar manner.

First, it is assumed that the master trigger (MT) is the first signal applied and that all three of the toggles (M, X, and Y) are set so that the $\overline{Q}$ outputs are at -6 volts. In the discussion of the basic toggle board, it was shown that a positive-going pulse applied to an input of a toggle board attempts to turn the ON transistor to OFF. Since $\overline{Q}$ is at -6 volts, the

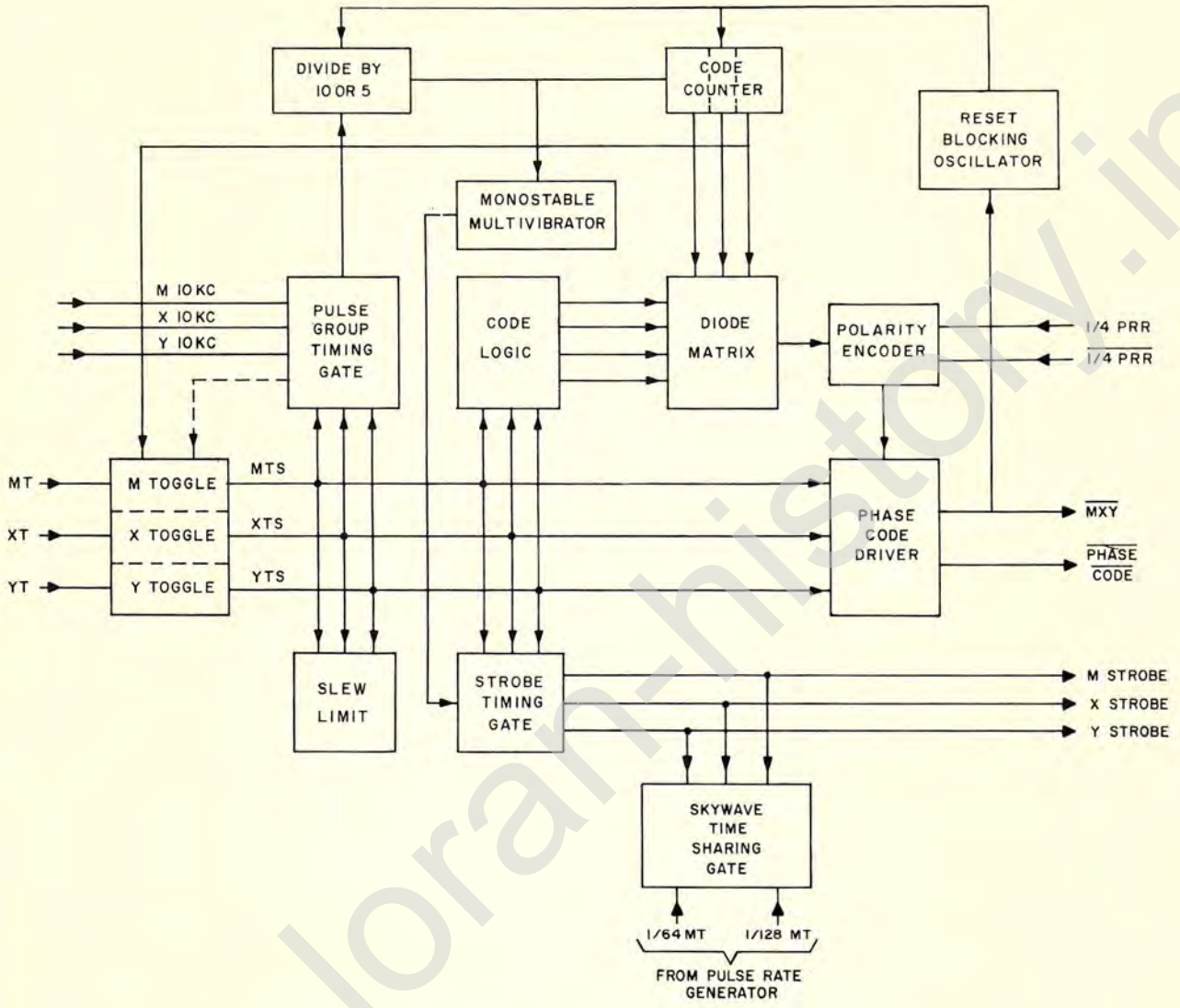


Figure 4-34. Code Group Generator, Block Diagram

Q output is at 0 volt and the transistor associated with the Q output is ON. When Q of the M toggle is ON, the MT pulse applied at CP will turn off the Q portion of the toggle. This causes the $\overline{Q}$ portion of the toggle board to turn on and to produce a level of 0 volt at the $\overline{Q}$ output. This is the $\overline{MTS}$ gate, which is applied to the pulse group timing gate circuit.

The pulse group timing gate circuit does two things: (1) it allows the master 10-kc to pass to the divide-by-10-circuit; and (2) it produces the K2 output for the X toggle, which goes from a level of -2 volts to approximately +4 volts.

During the time that the $\overline{MTS}$ gate is applied to the pulse group timing gate circuit, the master 10-kc signal is applied to the divide-by-10 circuit. The divide-by-10 circuit changes the 10-kc signal (100-microsecond period) to a signal of 1 kc (1000-microsecond period), which is applied to the 3-stage counter. The counter, if left to run free, will count eight 1-kc pulses before it produces the output applied to the $\overline{CP}$ input of the M toggle. However, additional circuitry causes the counter to reset and produce the positive-going output after only 7400 microseconds, rather than the 8000 microseconds that would normally be expected. Therefore, the input applied to $\overline{CP}$ of the M toggle has a duration of 7400 microseconds.

While the counter is running, the $\overline{MTS}$ gate applied to the pulse group timing gate circuit produces the

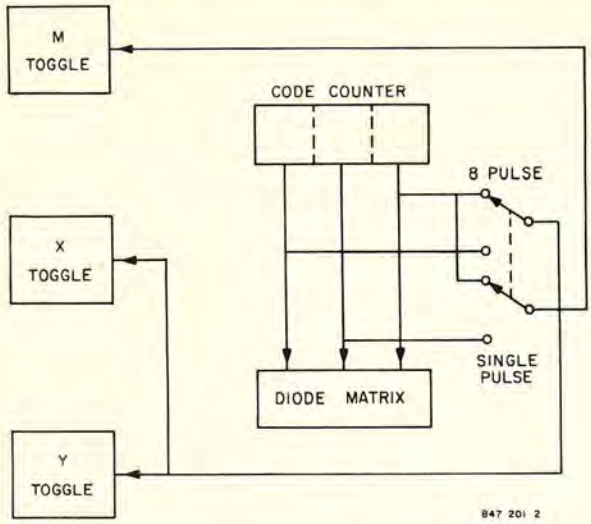


Figure 4-35. Reset Function Diagram for 8-Pulse or Single-Pulse Operation

K2 input gate for the X toggle, Since this signal (X-K2) is slightly positive, it blocks the X toggle so that the toggle cannot change state if a positive-going signal is applied to the CP input. Consequently, the master trigger and the X-slave trigger must be separated by at least 7400 microseconds.

When the counter has finished its timing function for the master time-shared signal (MTS), the X toggle is unblocked and is ready to accept the X-delay trigger. Notice that the counter output is applied to all three of the toggles. However, the X toggle and the the Y toggle are not disturbed when a positive-going signal is applied to the $\overline{CP}$ input while the master sequence is in progress (the $\overline{Q}$ portion is already cut off).

The following is the overall sequence of the M, X, and Y toggles:

(1) The M, X, and Y toggles are ready to accept trigger inputs.
(2) The master trigger is applied; the X toggle is blocked.
(3) The MTS gate is generated; the X toggle is released.
(4) The X trigger is applied; the Y toggle is blocked.
(5) The XTS gate is generated; the Y toggle is released.
(6) The Y trigger is applied; the M toggle is blocked.
(7) The YTS gate is generated; the M toggle is released.

(2) PULSE GROUP TIMING GATE (A1318).

(a) GENERAL. - See figure 6-144 for the schematic diagram of the circuit. The pulse group timing gate printed board is a dual purpose circuit. Transistors Q1, Q3, and Q5 are used to gate and combine three separate 10-kc inputs into a single time-shared output. Transistors Q2, Q4, and Q6 produce three separate blocking or inhibiting parts that are used in conjunction with the slew limit circuitry. The detailed circuit description of a single 10-kc gate ($\overline{MTS}$) and a single blocking gate (XK2) will be described.

The operation of Q1, Q3, and Q5 is identical as far as the inputs are concerned, but the outputs of these three transistors are connected in parallel to produce the single output for the combined 10-kc signal. Consider first the master 10-kc gate transistor, Q1. The master 10-kc signal is a square wave that is derived from the output of the 10-kc resolver driver through a squaring amplifier. This 10-kc square wave swings from 0 to -6 volts. The $\overline{MTS}$ input to the pulse group timing gate circuit is a square pulse of 7400-microsecond duration that is at a level of -6 volts during rest time, that goes to a level of 0 volt during gate time.

(b) DETAIL. - Assume that the MTS input is at -6 volts and that the 10-kc signal is also applied. With -6 volts applied through R1 to the base of Q1, the transistor is cut off and the emitter voltage is -6 volts, since no current flows through R4. At the same time, the 10-kc signal is applied to the cathode of CR1. However, the signal cannot pass through CR1 because it is reverse biased by the $\overline{MTS}$ input of -6 volts. The net result of this input condition is that none of the 10-kc signal passes through Q1 and the 10-kc output line remains at a level of -6 volts.

Assume that the $\overline{MTS}$ input is at a level of 0 volt and that the master 10-kc signal is also applied. Transistor Q1 conducts when 0 volt is applied to the base, causing the emitter voltage to rise to 0 volt. At the same time, the master 10-kc signal is applied to the cathode of CR1. Each time the 10-kc signal goes to a level of -6 volts, CR1 conducts and clamps the base of Q1 to -6 volts. The emitter voltage closely follows the base voltage since Q1 is connected as an emitter follower. Consequently, when the MTS input level goes to a level of 0 volt, diode CR1 is allowed to conduct and pass the 10-kc input to the base of Q1. A burst of 10-kc energy appears at the output, TP4, each time the $\overline{MTS}$ time-shared gate is applied.

The emitters of Q1, Q3, and Q5 are connected in parallel to the output line through CR2, CR4, and CR6, respectively. The action of these diodes is to isolate the emitters of Q1, Q3, and Q5 and to eliminate interaction.

The second function of the pulse group timing gate circuit is to produce the blocking signals (XK2, YK2, and MK2). These gating signals are supplied to the K2 inputs of the M-X-Y toggles in order to block any change in state of the toggles while the gate signals are applied. The individual circuits associated with Q2, Q4, and Q6 are identical, so that only the circuit of Q2 is discussed in detail.

The $\overline{MTS}$ signal is applied at the junction of R1 and R2. Resistors R2 and R3 form a voltage divider, and the base of Q2 is connected to the junction of these resistors. The base is at approximately -2 volts and Q2 is conducting during the time that the applied input level is at -6 volts. The signal applied at the

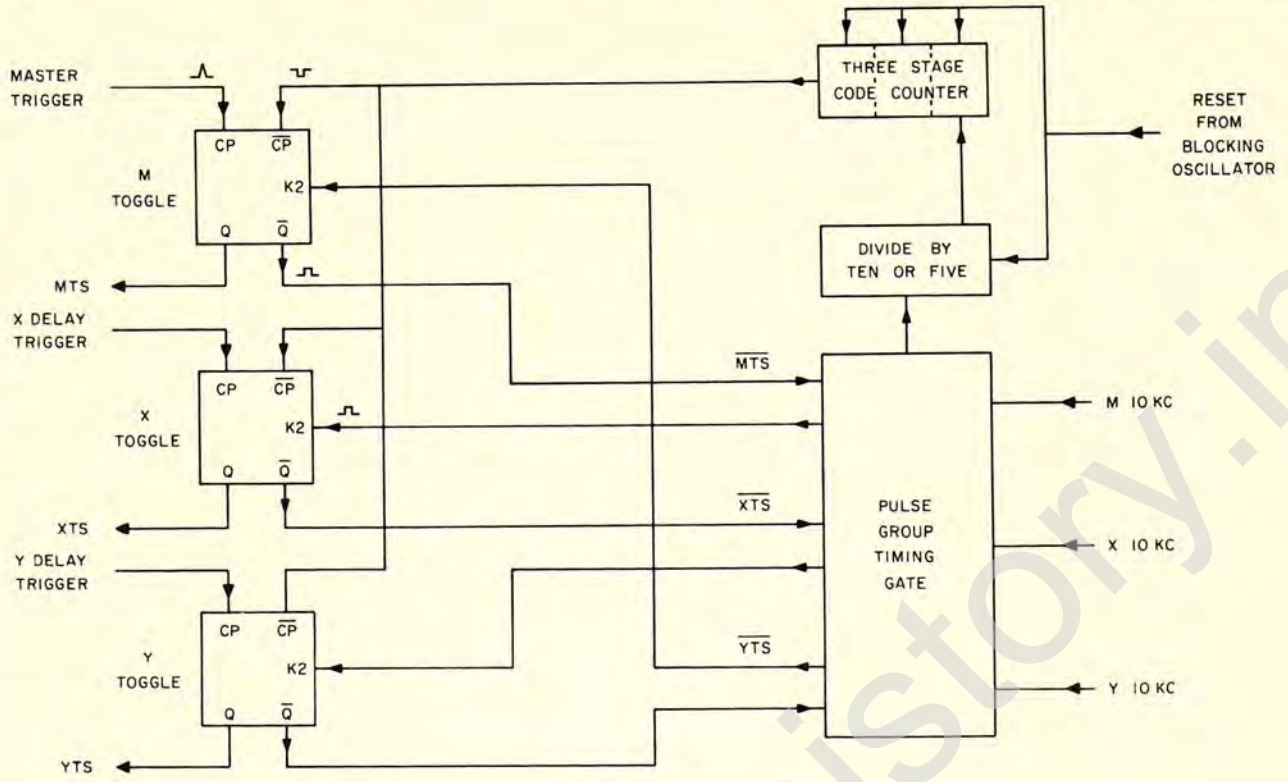


Figure 4-36. M, X, and Y Toggles, Block Diagram

base also appears at the emitter since Q2 is connected as an emitter follower. The $\overline{MTS}$ gate signal input next goes to a level of 0 volt. This level is divided across R2 and R3, and the resulting level applied to the base of Q2 is approximately +4 volts. The level of +4 volts appears at the emitter and is coupled out as the XK2 output. The purpose of Q2, Q4, and Q6 is essentially to raise the level of the $\overline{MTS}$, $\overline{XTS}$, and $\overline{YTS}$ gates from -6 and 0 volt to -2 and +4 volts, respectively.

(3) DIVIDE-BY-10 AND DIVIDE-BY-5 CIRCUITS. - As shown in the discussion of the divide-by-5 circuit, paragraph 4-2*d*(4), three toggle circuits are connected in such a manner to produce a division of 5. That is, five input cycles must be applied to obtain each output cycle.

In order to produce a division of 10, a single toggle circuit is added to the signal path in front of the divide-by-5 circuit. This toggle provides an initial 2-to-1 division of the incoming signal frequency before it is applied to the divide-by-5 circuit. There is also a switch which allows the operator to choose either 500-microsecond or 1000-microsecond pulse spacing. In general use, pulse spacing of 1000 microseconds will be used.

(4) CODE COUNTER. - The code counter consists of three toggle circuits connected for counter operation. Basic counter circuits are discussed in paragraph 4-2*e*(1) of the discussion of the pulse rate Generator. The code counter supplies the diode matrix with a series of binary numbers, each having a duration of 1000 microseconds. The binary inputs to the diode matrix are combined with the code logic inputs to produce the phase code information as required for the remaining circuits.

(5) CODE LOGIC (A1315).

(a) GENERAL. - The code logic circuit is contained on a single printed board. The purpose of this circuit is to combine the five input timing gates (MTS, XTS, YTS, 1/2MT, and $\overline{1/2MT}$) to produce the logic timing outputs. The logic timing gates (M-1, S-1, M-2, and S-2) are then applied to the diode matrix where the phase coding information is procured. Figure 4-38 shows the time relationships of the input and output waveforms with respect to the master trigger, X-delay trigger, and the Y-delay trigger.

(b) DETAIL. - See the schematic diagram of the code logic circuit shown in figure 6-141. The transistors in this circuit are all connected as emitter followers. The voltage applied at the base will also appear at the emitter. Transistor Q1 is preceded by an OR circuit which consists of CR1, CR2, and R1, while Q2, Q3, Q4, and Q5 are preceded by AND circuits. First, consider the action of Q1. Assume that levels of 0 volt are applied at the cathodes of CR1 and CR2. There is no potential difference across the diodes and the base of Q1 is at a level of 0 volt, which places the emitter voltage also at 0 volt. Assume that a level of -6 volts is applied to the cathode of either CR1 or CR2. The diode conducts through R1 to ground, and the base voltage goes to -6 volts with the emitter level following. Next, consider the action of Q2. The AND circuit at the base of Q2

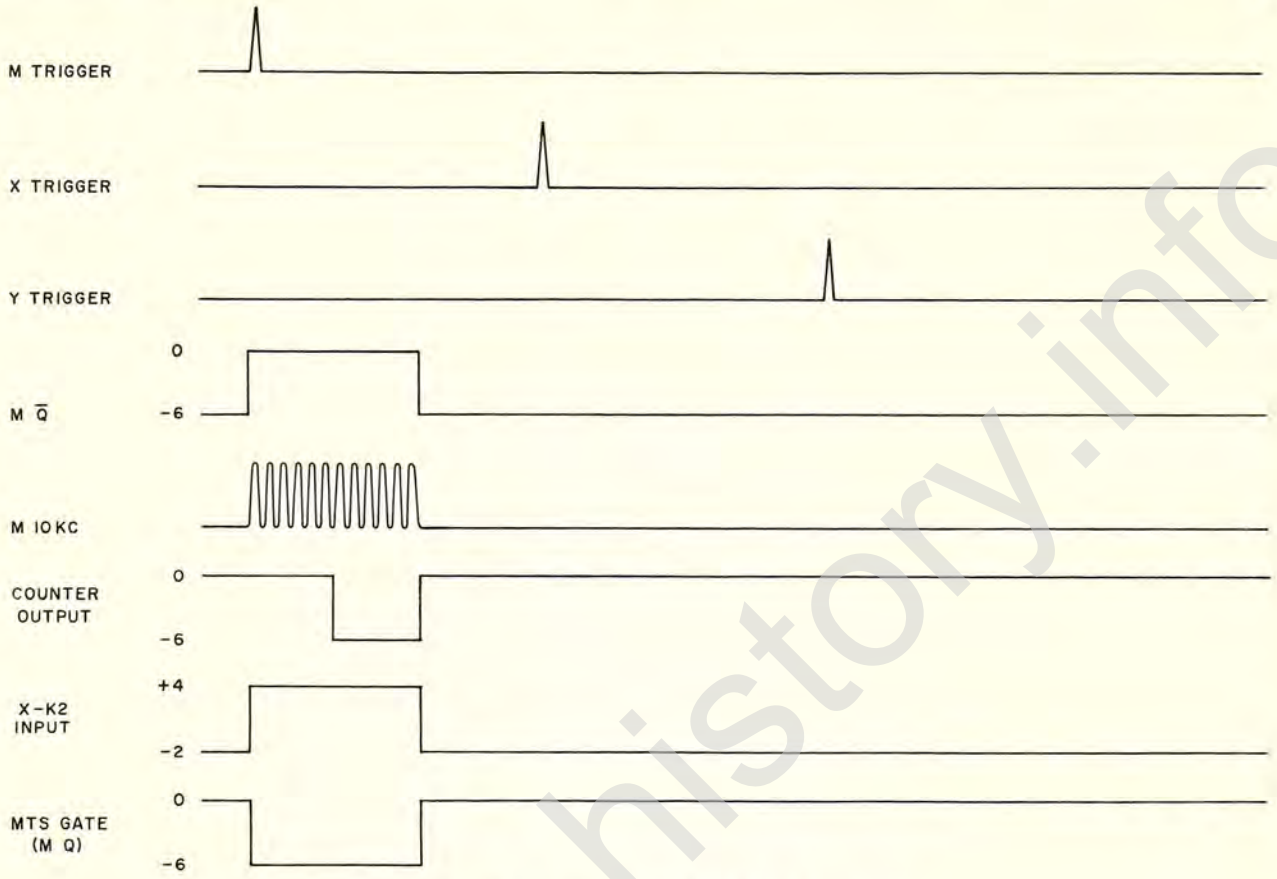


Figure 4-37. M, X, and Y Toggles, Waveshapes

consists of CR3 and R4. Assume that levels of 0 volt are present at the anode of CR3 and at the junction of R4 and R5. The resulting level at the base of Q2 is 0 volt. Assume that a level of 0 volt is applied to the anode of CR3 and a level of -6 volts to the junction of R4 and R5. The diode conducts (short circuit) and keeps the base of Q2 at 0 volt with the 6 volts being dropped across R4. However, when a level of -6 volts is applied at both the anode of CR3 and at the junction of R4 and R5, there is no potential difference between the inputs. The base of Q2 is at a level of -6 volts and the emitter follows to the same level.

The operation sequence of the code logic circuit should now be clear. At time 1, only the group separation gate, $\overline{1/2MT}$, is at -6 volts. Since only one signal of -6 volts is applied to the AND circuit of Q5, all outputs remain at a level of 0 volt.

At time 2, inputs of -6 volts are applied to CR3 and to the junction of R4-R5 (MTS and 1/2MT). The input requirements of only the Q2 AND circuit are satisfied, and an output of -6 volts appears at the emitter of Q2 (M-1).

At time 3, inputs of -6 volts are applied to CR1 and to the junction of R4 and R5 (XTS and 1/2MT). The XTS input is transferred to the anode of CR4 through Q1. The requirements of the Q3 AND circuit are satisfied, and an output of -6 volts appears at the emitter of Q3 (S-1).

At time 4, inputs of -6 volts are applied to CR2 and to the junction of R4 and R5 (YTS and 1/2MT). The YTS input is transferred to the anode of CR4 through Q1. The requirements of the Q3 AND circuit are satisfied, and an output of -6 volts appears at the emitter of Q3 (S-1).

At time 5, inputs of -6 volts are applied to CR5 and to the junction of R8 and R9 (MTS and $\overline{1/2MT}$). The input requirements of only the Q4 AND circuit are satisfied, and an output of -6 volts appears at the emitter of Q4 (M-2).

At time 6, inputs of -6 volts are applied to CR1 and to the junction of R8 and R9 (XTS and $\overline{1/2MT}$). The XTS input is transferred to the anode of CR6 through Q1. The requirements of the Q5 AND circuit are satisfied, and an output of -6 volts appears at the emitter of Q5 (S-2).

At time 7, inputs of -6 volts are applied to CR2 and to the junction of R8 and R9 (YTS and $\overline{1/2MT}$). The YTS input is transferred to the anode of CR6 through Q1. The requirements of the Q5 AND circuit are satisfied, and an output of -6 volts appears at the emitter of Q5 (S-2).

At time 8, the input conditions are the same as discussed during time 1, and the cycle of the code logic circuit is completed. This cycle is repeated once during the time interval of two master triggers.

(6) DIODE MATRIX (A1314). - In an earlier discussion, paragraph 4-2*e*(1), it was explained how the

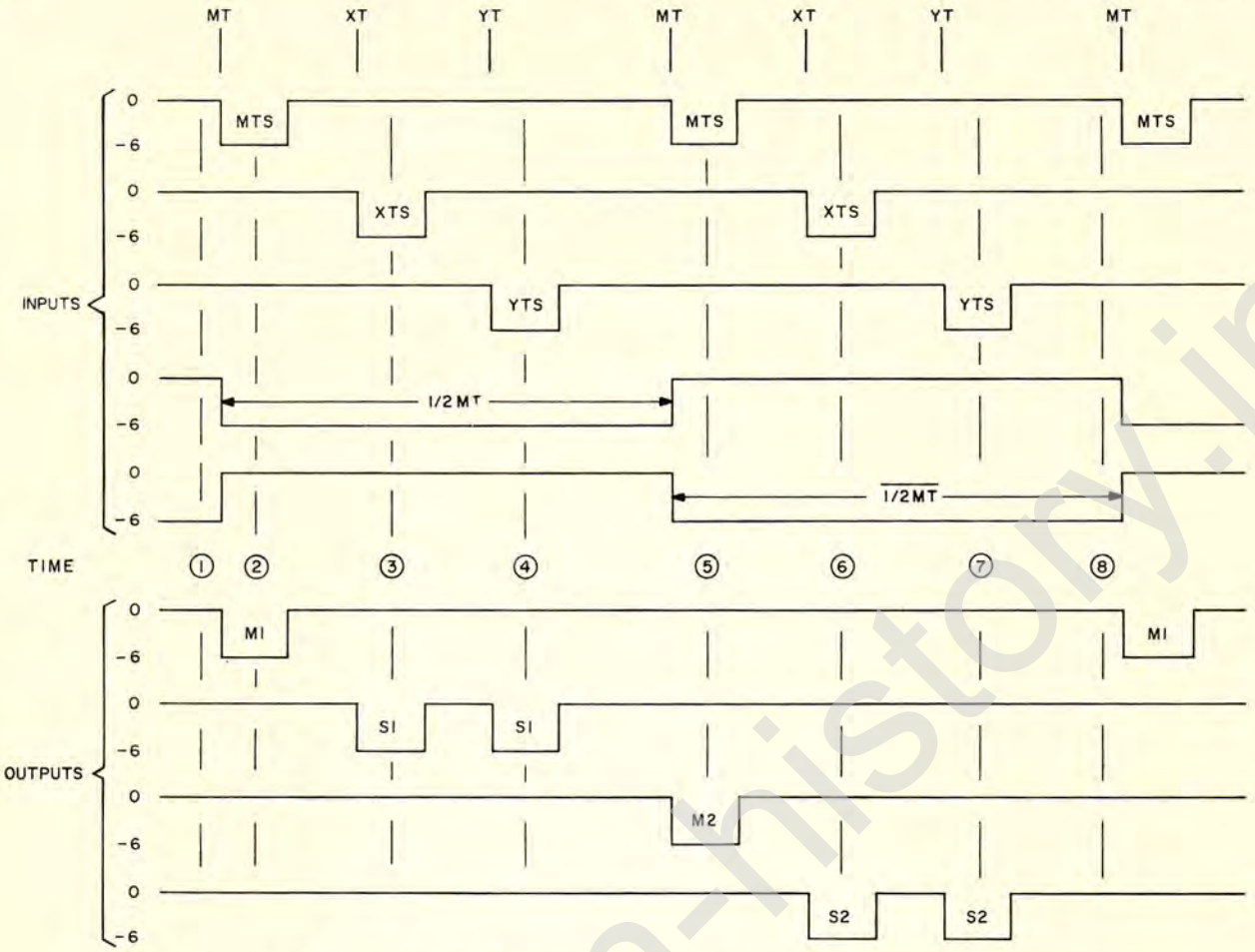


Figure 4-38. Code Logic Circuit, Waveshapes and Time Relationship Diagram

basic diode matrix functions. The diode matrix used in the code group generator section of the Loran-C receiver is a 6-line matrix with added gating circuits preceding each matrix line. The outputs of the matrix lines are connected through an OR circuit to a common output. The purpose of the diode matrix is to produce the actual phase-code information that is later applied to the time-shared detector. The output level of the diode matrix is either 0 volt or -6 volts. The 0-volt level represents a 0° phase shift, and the output of -6 volts represents a 180° phase shift.

Each code group consists of eight pulses, each having a specific phase code. The phase code of the code groups is shown in table 4-6.

Notice that pulse number 1 and pulse number 5 are always zero phase. Since there is no need to produce an output of -6 volts from the matrix for the first or the fifth pulse, these lines are deleted from the matrix and only the remaining six lines (2, 3, 4, 6, 7, and 8) are needed to perform the desired phase coding functions.

The output from the 3-stage code-group counter is in the form of binary numbers from 0 through 7. However, the pulse numbers are referred to as 1 through 8. Therefore, the binary output 0 represents pulse number 1, binary output 1 represents

TABLE 4-6. LORAN-C PHASE CODING

CODE GROUP	PULSE PHASE							
	1	2	3	4	5	6	7	8
M-1	0	0	180	180	0	180	0	180
M-2	0	180	180	0	0	0	0	0
S-1	0	0	0	0	0	180	180	0
S-2	0	180	0	180	0	0	180	180

pulse number 2, etc. Since the first and fifth pulse are always zero phase, the horizontal matrix lines are referred to as line 2, line 3, line 4, line 6, line 7, and line 8 from top to bottom, with line 1 and line 5 deleted. The line number refers to its corresponding pulse number.

See the schematic diagram of the diode matrix shown in figure 6-140. Observe that the M-1 input to the diode matrix is applied to lines 3, 4, 6, and 8 through diodes CR3, CR5, CR7, and CR11. Lines 3, 4, 6, and 8 are energized during the time that the M-1 gate of -6 volts is applied at the input. As

binary inputs are applied from the counter, the energized lines will be released from a level of 0 volt to a level of -6 volts and the proper binary number is applied to the proper line. Lines 3, 4, 6, and 8 are released in sequence as the counter counts from 0 to 7. An output level of -6 volts is produced during the time each line is released. Each binary number is applied from the counter for a duration of 1000 microseconds, and the energized lines are released for a time of 1000 microseconds. The matrix outputs during each of the code logic gates are shown in figure 4-39.

Notice that the M-2 logic gate is applied to lines 2 and 3 through CR2 and CR4. Consequently, only lines 2 and 3 can be released to -6 volts while the M-2 gate is applied. Only lines 6 and 7 are energized while the S-1 code logic gate is applied. They correspond to the 180-degree phase code of the sixth and seventh pulses. The S-2 code logic gate is applied to lines 2, 4, 7, and 8 through diodes CR1, CR6, CR9, and CR12.

It can be seen that the combination of the code logic gates and the code group counter outputs produces wave shapes that are translated into phase-coding information. These functions are dependent on the master and slave timing triggers and on gating functions derived from these triggers. The diode matrix itself detects a specific group of inputs to produce the desired output.

(7) POLARITY ENCODER (A1321).

(a) GENERAL. - Polarity Encoder A1321 receives the two complementary outputs from the fox-trot generator and the output from the diode matrix. The matrix output level gates the circuit so that the output is either the fox-trot output or its complement. The resultant is, therefore, polarity coded for application to the phase code driver.

The polarity encoder schematic may be represented by the block diagram of figure 4-40.

When the input from the diode matrix is 0 volt (ground potential), the complementary output from

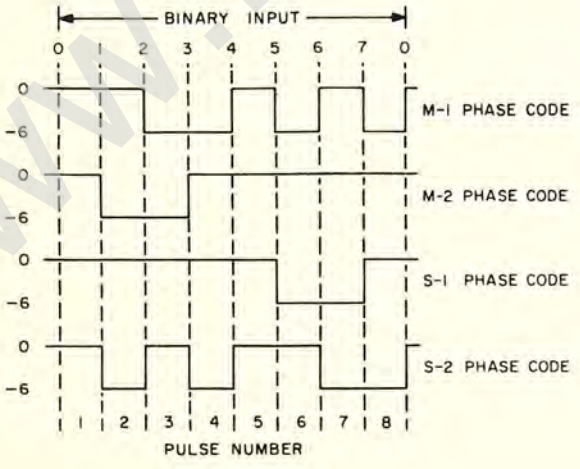


Figure 4-39. Matrix Output for Code Logic Gates

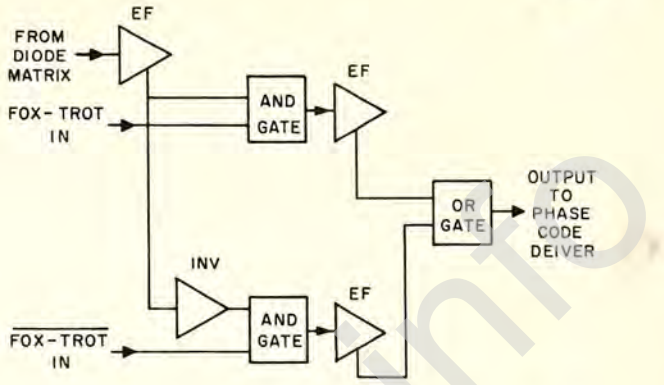


Figure 4-40. Polarity Encoder, Block Diagram

the fox-trot generator appears at the output to the phase code driver. When the input from the diode matrix is -6 volts, regular output from the fox-trot generator appears at the output to the phase code driver.

(b) DETAIL. - See the schematic diagram shown in figure 6-147. The polarity encoder contains one emitter follower circuit (transistor Q1), one inverter amplifier (transistor Q2), two AND gates (diodes CR2 and CR3 followed by emitter follower transistor Q3 and diodes CR5 and CR6 followed by emitter follower transistor Q4), and one OR gate (diodes CR4 and CR7). The 0-volt (ground potential) or -6-volt input from the diode matrix is coupled to the base of emitter follower transistor Q1.

When the input from the diode matrix is 0 volt (ground potential), Q1 conducts and the emitter of Q1 is also 0 volt. Diode CR3 is forward biased since the emitter of Q1 is coupled to its anode. This inhibits the AND gate comprised of diodes CR2 and CR3 and grounds the base of transistor Q3. The Q3 emitter is now also at ground potential since the transistor is an emitter follower. Thus, no input is provided to the cathode terminal of diode CR4, which is one of the two inputs of the OR gate (CR4 and CR7). The emitter of transistor Q1 is also coupled to the base of inverter transistor Q2. Since the emitter of Q1 is 0 volt (ground potential), the collector output of inverter transistor Q2 is -6 volts. Diode CR1 clamps the collector to -6-volt maximum negative polarity. This -6 volts is the input to the anode terminal of diode CR5 and reverse-biases the diode, thus enabling the AND gate. The complementary fox-trot input from the fox-trot generator is now allowed to control the output of the emitter follower transistor Q4 and, hence the output of the OR gate (output from terminal 6 to the phase code driver).

When the input from the diode matrix is -6 volts, -6 volts is applied to the base input of inverter transistor Q2. The collector output of Q2 is 0 volt (ground potential), which grounds the anode of diode CR5 (forward-biases the diode) and inhibits the AND gate. Ground potential is now present at the emitter of transistor Q4, which is the input to the cathode of diode CR7. The emitter of transistor Q1 also furnishes -6 volts to the anode of diode CR3. This

enables the AND gate, allowing the regular fox-trot signal to appear at the emitter of transistor Q3 (which is the cathode input of diode CR4). Thus, the regular fox-trot signal now controls the input to the OR gate and appears at output terminal 6, the input to the phase code driver.

(8) PHASE CODE DRIVER (A1316). - The phase code driver plug-in board performs two separate functions. The first portion of the circuit acts as a combiner wherein the master time-shared gate, the X-slave time-shared gate, and the Y-slave time-shared gate are combined on a single time base and inverted to produce the $\overline{MXY}$ TS signal. See the schematic diagram of the phase code driver shown in figure 6-142. The three inputs to Q1 are applied through an OR circuit composed of diodes CR1, CR2, and CR3. These inputs are the MTS, XTS, and YTS signals. The emitter of Q1 is grounded and the collector is clamped to a level of -6 volts through the combination of dropping resistor R3 and diode CR4. When 0 volt is applied at all inputs, the base of Q1 is biased to a positive voltage by R1 and R2 through the +6-volt d-c supply, holding the transistor cut off. When the MTS, the XTS, or the YTS input is applied (-6-volt gates), the base of Q1 goes to a negative voltage, causing Q1 to conduct heavily. The heavy conduction (switch-on) condition brings the collector voltage to approximately 0 volt for the duration of each of the input gates. By this action, the three inputs, on separate time bases, are inverted and combined on a single time base.

The circuits associated with Q2, Q3, and Q4 receive the polarity encoder code input and produce outputs of phase code and $\overline{\text{phase code}}$ that are of identical time duration and relationship, but are complementary. The base of Q2 is connected to the diode matrix line which will deliver either 0 volt or -6 volts. Transistor Q2, which is connected as an emitter follower, is used in the circuit as an isolation stage and impedance-matching device. The Q2 emitter is at 0 volt when an input of 0 volt is applied to the base. This signal is coupled through R6 and C2 to the base of Q3. Capacitor C2 is used in the circuit as a balancing component to equalize the inherent capacity of the transistor. This compensating capacity minimizes phase shift through the amplifier and helps to increase the steepness of the leading edge of the wave shape. Resistors R6 and R7 form a divider network to establish a positive voltage on the base of Q3 when the emitter of Q2 is at 0 volt. Therefore, transistor Q3 is cut off. The collector is clamped to -6 volts by the action of R8 and CR5. The phase code signal is coupled out of the plug-in board from the collector of Q3. This signal is also applied through R9 and balancing capacitor C3 to the base of Q4, a simple inverter. Transistor Q4 conducts heavily when the negative voltage is applied to the base, causing the collector voltage to approach the emitter voltage. The collector output, $\overline{\text{phase code}}$, is 0 volt and is coupled out of the plug-in board.

When the diode matrix input voltage on the base of Q2 changes to -6 volts, phase code and $\overline{\text{phase code}}$ reverse and become 0 volt and -6 volts, respectively.

(9) RESET BLOCKING OSCILLATOR (A1312). - The reset blocking oscillator receives a square-wave input from 0 to -6 volts from an OR circuit. The reset blocking oscillator applies a -6-volt to +3-volt signal to reset the toggle circuits in the divide-by-10 (or 5) circuit and the toggle circuits that work in conjunction with the diode matrix. For a discussion of the reset blocking oscillator, refer to paragraph 4-2*e*(5).

(10) MONOSTABLE MULTIVIBRATOR (A1313). - The monostable multivibrator obtains a trigger signal from the divide-by-10 circuit (or the divide-by-5 circuit if the pulse timing switch is set to 500 microseconds). It applies a -6-volt, 45-microsecond pulse to the strobe timing gates. The station strobe triggers and guard triggers are produced when the MTS, XTS, or YTS signal is applied to its respective strobe timing gate at the same time the monostable multivibrator pulse is applied. For a discussion of the circuit operation for the monostable multivibrator, refer to paragraph 4-2*d*(3).

(11) STROBE TIMING GATE (A1317). - The strobe timing gate plug-in printed circuit board contains three identical transistor gating circuits. A schematic diagram of the circuit is illustrated by figure 6-143. The strobe timing gate has four inputs: the master time-shared gate (MTS); the X time-shared gate (XTS); the Y time-shared gate (YTS); and the output pulse from the monostable multivibrator. The multivibrator pulse is applied in parallel to all three transistor stages. The MTS, XTS, and YTS gates are each applied to a separate transistor. The outputs of the strobe timing gate consists of three groups of trigger pulses for the M, X, and Y guard strobe and three groups of trigger pulses for the M, X, and Y sampling strobe.

Only the Q1 stage will be discussed since the three gate circuits are electrically identical. The collector load resistor R2 and emitter resistor R3 are approximately the same value. NPN transistor Q1 conducts heavily and both the emitter level and the collector level approach 0 volt when 0 volt is applied at the base. The transistor cuts off when a negative voltage (-6 volts) is applied to the base. The collector voltage changes to +6 volts and the emitter voltage changes to -6 volts. Thus, for a given change at the transistor base, the stage provides an in-phase change at the emitter output and a complementary change at the collector output.

See figure 4-41 for the time relationship of the waveforms involved in the following discussion. Prior to zero time, the two Q1 inputs (MTS signal and monostable multivibrator input) are at a level of zero volts. Diodes CR1 and CR2, resistor R1, and the -6-volt d-c input of the circuit board form an AND circuit at the input of Q1. With 0 volt applied at their anodes and -6 volts applied through R1 to their cathodes, both diodes conduct heavily (short circuits). Consequently, the 6-volt d-c input is dropped across R1, and the Q1 base potential is clamped at 0 volt through the conducting diodes. As previously mentioned, 0 volt at the base of Q1 causes heavy conduction in the transistor and provides output levels of 0 volt at both emitter and collector.

At zero time, the MTS signal changes to -6 volts. The monostable multivibrator input, however,

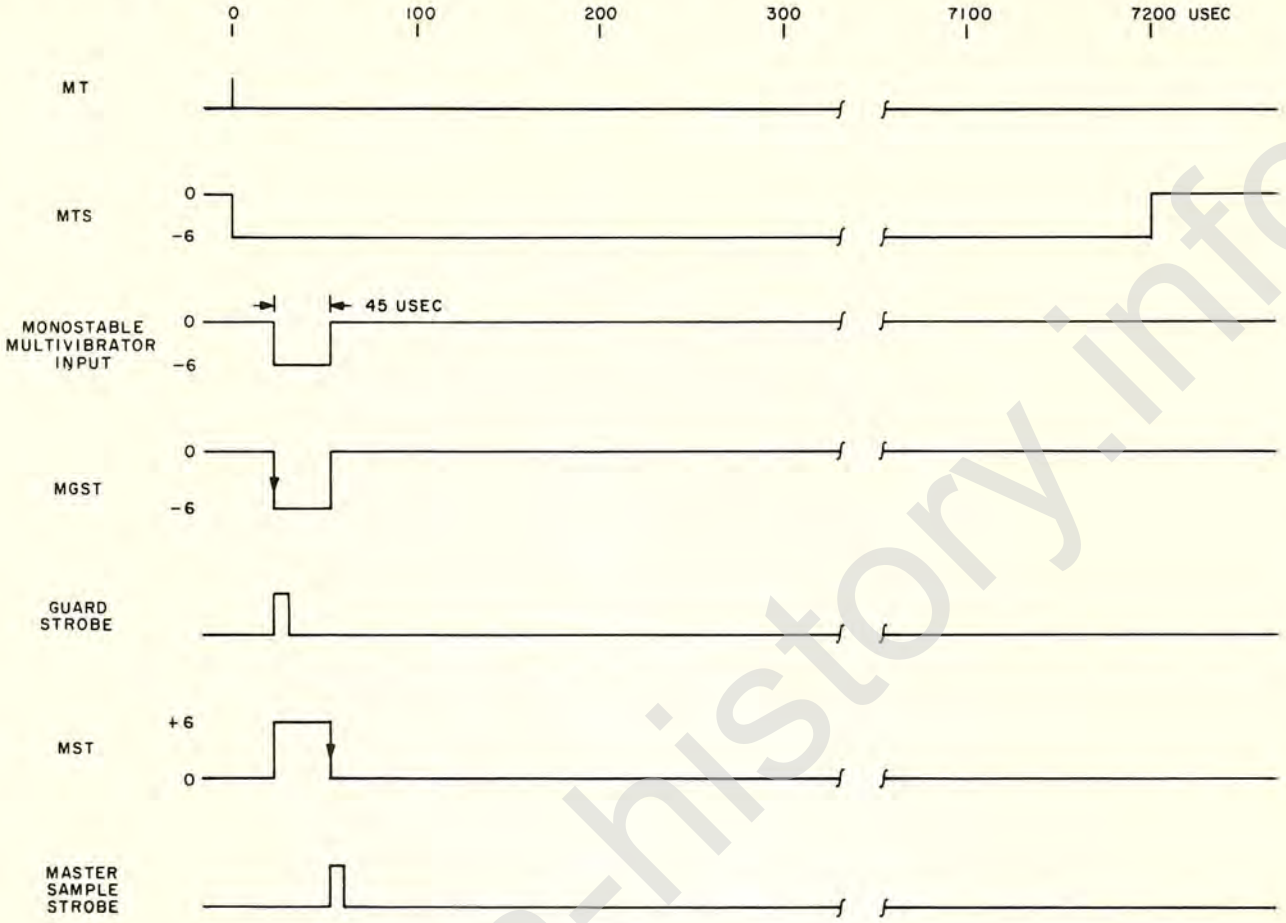


Figure 4-41. Strobe Timing Gate, Waveshapes

remains at 0 volt. Conduction still occurs from the -6-volt d-c source through R1 and CR2 to clamp the Q1 base potential at 0 volt. Therefore, the Q1 outputs remain at 0 volt. A short time later, the monostable multivibrator input level also changes to -6 volts. Both of the AND circuit diodes are now cut off by -6 volts applied to their anodes. The base potential of Q1 changes to -6 volts and the transistor cuts off since conduction no longer occurs through R1. The emitter level changes from 0 to -6 volts and the collector level changes from 0 to +6 volts.

The monostable multivibrator input returns to 0 volt 30 microseconds later, causing diode CR2 to conduct and clamping the base of Q1 to 0 volt. The transistor returns to heavy conduction, causing both collector output and emitter output to return to zero volts.

To summarize briefly, the monostable multivibrator pulse and the MTS signal are applied simultaneously to the input of transistor Q1. The Q1 stage provides two output pulses which coincide in time with the 45-microsecond monostable multivibrator pulse, and which are complementary in phase. The negative-going MGST output is used to trigger the guard strobe blocking oscillator, and the positive-going MST output is used to trigger the master strobe blocking oscillator. Since the two blocking oscillators are triggered by negative-going variations at their inputs, the guard strobe blocking oscillator is triggered when the leading edge of the monostable multivibrator input occurs. The master strobe blocking oscillator is triggered 45 microseconds later, when the trailing edge occurs.

The X-strobe trigger circuit, Q2, and the Y-strobe circuit, Q3, function in a manner similar to the master strobe trigger circuit just described, but at a later time.

The code logic board, E1007, is a group of AND and OR gates that prevent the buildup of a d-c offset caused by uneven coding cancellation of interfering signals during interfering signal conditions. The problem arises only for the M2 signal and for the S1 signal. In each of these cases, there are four positive pulses more than negative pulses. The code logic board prevents four positive pulses from being strobed for each of these signals under track condition.

See the schematic diagram, figure 6-181. There are two identical AND circuits (R1030-CR1049 and R1029-CR1046) which operate identically to the signals applied to them. The signal applied to terminal 7 is the Q output from toggle A1307, and the signal applied to terminal 6 is the M2 signal. A1307 triggers on the fourth pulse of any of the gates (MTS,

XTS, or YTS). M2 is the gate for the M2 period only. A gate signal is zero (ground) potential during a complete cycle except for the period of the gate, when it is -6 volts. By applying M2 to an AND gate with a signal which is ground during the last four pulses, only the first four are passed through to the strobe timing gate circuit. The other AND gate has the $\overline{Q}$ signal of toggle A1307 along with S1 applied to it. The $\overline{Q}$ signal is -6 volts during the last four pulses of S1, but is 0 volt during the first four. Therefore, the first four pulses of S1 are inhibited.

The AND gate consisting of CR1045, CR1047, and CR1048 insures that the signal to the output will never be more positive than ground potential. Diode CR1044 receives a ground potential through station selector switch S1003 to inhibit the logic board circuitry when it is desired to strobe all eight pulses (e.g. when searching for the signal).

The network consisting of Q4 and Q5 raises the input (-6 to 0 volt) applied to terminal 14 of the strobe timing gate circuit to a level from 0 to +6 volts. The signal from Q5 applied through diodes CR3, CR6, and CR9 cuts off the Q1, Q2, and Q3 stages at the time inhibiting is desired.

(12) SKYWAVE TIME SHARING GATE (A1319). - The skywave time sharing gate circuitry time-shares the three guard strobe functions so that a single strobe board can be used to perform the three sampling actions desired. The master, X, and Y guard strobe triggers (MGST, XGST, and YGST) are all applied to the skywave time-sharing gate at the same time. However, only guard strobe triggers from one source at a time are allowed to pass through to the output of this board. The output sequence of the triggers is MGST (16 groups), XGST (8 groups), and YGST (8 groups). This time-sequence output is produced by applying gate signals to the skywave time-sharing gate.

See figure 4-42. The gating function is accomplished by applying both trigger signals and the gate signals

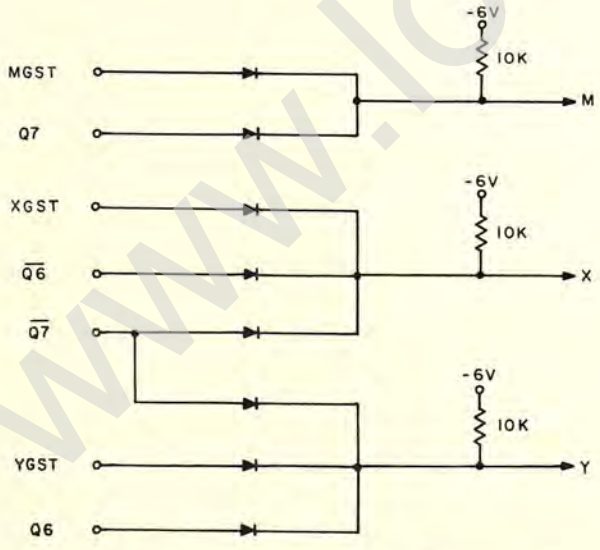


Figure 4-42. AND Gates in the Skywave Time Sharing Gates

to the three AND circuits. The AND circuits, as used here, allow an output to be produced only when all inputs are at a level of -6 volts. If any one of the inputs to an AND circuit is not at -6-volts, the AND circuit is blocked and no output is produced. The skywave time-sharing gate employs three separate AND circuits, each being applied to separate emitter follower stages.

Since the three portions of the circuit operate in a similar manner, consider only the master portion of the circuit. The MGST pulse signal is passed when the Q7 input gate is at -6 volts. See the schematic diagram of figure 6-145. For the output wave shapes from the skywave time-sharing gate, see figure 4-43. During time 1, the Q7 gate input of -6 volts is applied to the anode of CR2. The MGST signal pulses of -6 volts are applied to the anode of CR1. If either the anode of CR1 or CR2 is at 0 volt, the base of transistor Q1 is clamped to 0 volt. However, with -6 volts applied at CR2 (Q7 gate), the base of Q1 is released to -6 volts each time an MGST signal pulse is applied. The emitter level of Q1 follows the level applied at the base since the transistor is connected as an emitter follower. These pulses (MGST) are developed across R2 and applied to the cathode of CR3. The anode of CR3 is connected through R7 to ground. Diode CR3 conducts when a level of -6 volts is applied to its cathode, causing flow through R7 and a signal of -6 volts to be produced at this output. During time 1, transistors Q2 and Q3 are blocked by the zero level $\overline{Q7}$ gate signal applied to CR4 and CR8.

During time 2 the following conditions exist:

1. The Q7 gate signal is at 0 volt which blocks the AND circuit of transistor Q1.
2. The $\overline{Q6}$ gate signal is at 0 volt which blocks the input AND circuit of transistor Q3.
3. The $\overline{Q7}$ gate signal of -6 volts is applied to CR4 and CR8.

Also during time 2, the Q6 gate signal is at -6 volts on the anode of CR5. Two gate signals of -6 volts are applied to the AND circuit of transistor Q2 along with the -6-volt pulses of the XGST signal. This condition satisfies the requirements of the AND circuit for transistor Q2 and its base is released to -6 volts when each XGST pulse is applied. The emitter follower produces an output which is applied to CR7, which conducts. The output voltage is then developed across R7 and appears at the output of the printed board.

During time 3 the following conditions exist:

1. The Q7 gate signal of 0 volt blocks the AND circuit of transistor Q1.
2. The Q6 gate signal of 0 volt blocks the AND circuit of transistor Q2.
3. The $\overline{Q7}$ and Q6 gate signals of -6 volts release CR8-CR9 in the AND circuit of transistor Q3.

This condition allows the AND circuit of transistor Q3 to pass the YGST signal pulses of -6 volts and produce an output.

The output of each transistor is isolated from the others by CR3, CR7, and CR11 on the output line. For example, when the emitter of Q1 is at -6 volts, the emitters of Q2 and Q3 are at 0 volt. The output line goes to -6 volts and CR7 and CR11 are reverse biased, thus isolating Q2 and Q3 from the output of Q1.

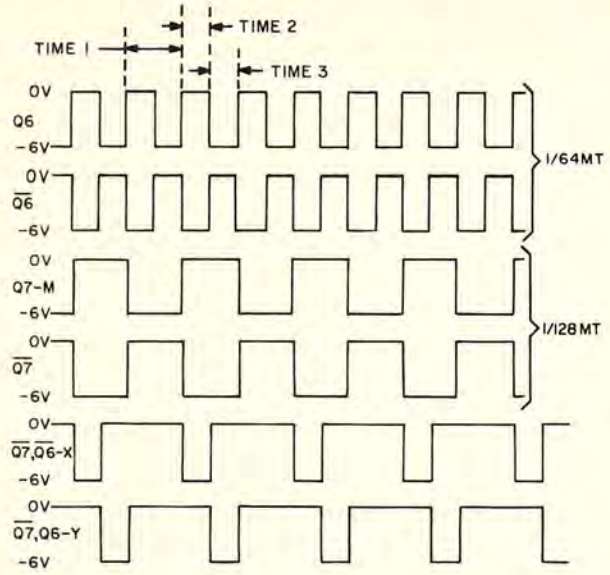


Figure 4-43. M, X, and Y Signal Development in the Skywave Time Sharing Gate

(13) SLEW LIMIT (A1320). - The slew limit circuit produces information that prevents overlap of any two of the time-shared gates (MTS, XTS, and YTS). The information supplied by this circuit is applied to relays that turn the various gates when they are overlapped. In the slewing process, the spacing between the X or Y time-shared gates and the M time-shared gate increases or decreases, depending on the direction of slewing. Time overlap of these gates must be prevented to keep from upsetting the logic of the agc switching circuit. The slew limit circuit is composed of three electrically identical 3-stage transistor circuits. See the schematic diagram, figure 6-146. The master slew limit (MSL) portion consists of Q1, Q2, and Q3. The X and Y slew limit portions (XSL and YSL) are composed of Q4, Q5, and Q6 and Q7, Q8, Q9, respectively.

The time-shared signals (MTS, XTS, and YTS) swing from a level of 0 volt to -6 volts during the time interval of the respective gate. When the gate is missing (when the MTS, XTS, or YTS line is zero), a level of 0 volt is applied to the base of the first transistor through its respective 2200-ohm resistor. See the first of the figures in 4-44. Example A shows the normal state of the three time-sharing waveforms without overlap. Example B shows the X-slave delay increased to the point that it overlaps Y. The dotted lines indicate what position YTS would occupy if XTS were further to the left. In the third figure, example C, the XTS waveform is locked out since its delay was reduced to the point that it overlapped MTS. The last diagram, example D, shows that too much delay in YTS will lock out MTS.

Figure 4-45 is the schematic diagram of the peak detector that senses the absence of a time-shared waveform. Three of these circuits are required, one for each of the three pulse trains. The voltage on the capacitor is held close to -6 volts as long as there is an input signal. This voltage keeps transistor Q3 cut off, thus keeping relay K1 deenergized. The constants of the circuit have been chosen to work under the worst condition; that is, single-pulse operation.

Absence of YTS indicates that the X delay has increased too much or the Y delay has decreased too much. Absence of the XTS waveform indicates that the X delay has decreased too much. Absence of the MTS waveform indicates that the Y delay has increased too much.

The relays in the peak detectors are used to reverse the direction of slewing in the proper slave delay unit. For instance, if Y delay was set at 35,000 microseconds, as shown in the second diagram, and the X delay was being increased from some low value, the slewing of the X-delay channel would reverse upon reaching about 27,800 microseconds.

h. DETECTOR-STROBE SECTION.

(1) GENERAL.- The detector-strobe section in the receiver is where the signals from the r-f portion and the internally generated signals are combined to produce error information for detection to achieve lockon, and to maintain track. The circuits in this section are the following:

Envelope deriver
Strobe blocking oscillator
Strobe timing gate
Fox-trot generator
Reference driver
Chopper driver
Line polarity coder
Detector-strobe
Strobe amplifier
Guard strobe amplifier

The block diagram of this section appears in figure 4-46. To understand the method of detection used, the nature of the r-f information must be understood.

(a) RECEIVED R-F SIGNAL.- The received r-f information is master 1, slave 1, master 2, and slave 2. The order in which these signals are transmitted is: master 1 (from the master station); slave 1 (from the X station); slave 1 (from the Y station); master 2 (from the master station); slave 2 (from the X station); and slave 2 (from the Y station). Each of the four signals is comprised of eight coded pulses. (There is a ninth pulse transmitted from the master station, but it is not used in the receiver.) Each of the eight coded pulses consists of a 100-kc carrier for 200 microseconds, while between pulses, no carrier exists. The coding of the pulses is determined by the phase of the pulse 100-kc carrier (figure 4-47).

(b) CODING.- The coding of the pulses is either positive or negative. A positive-coded pulse may be represented by $\sin \theta$. A negative-coded pulse may then be represented by $\sin (\theta + 180°)$. An example of the received r-f signal is shown in figure 4-48. An example of one of the coded pulses is shown in figure 4-49.

(c) ENVELOPE. - The envelope is the output from the envelope detector (when the 100-kc reference and received r-f signal inputs are in-phase). The envelope is shown in figure 4-50. Notice that the 100-kc signal is removed by a low-pass filter, leaving only the envelope.

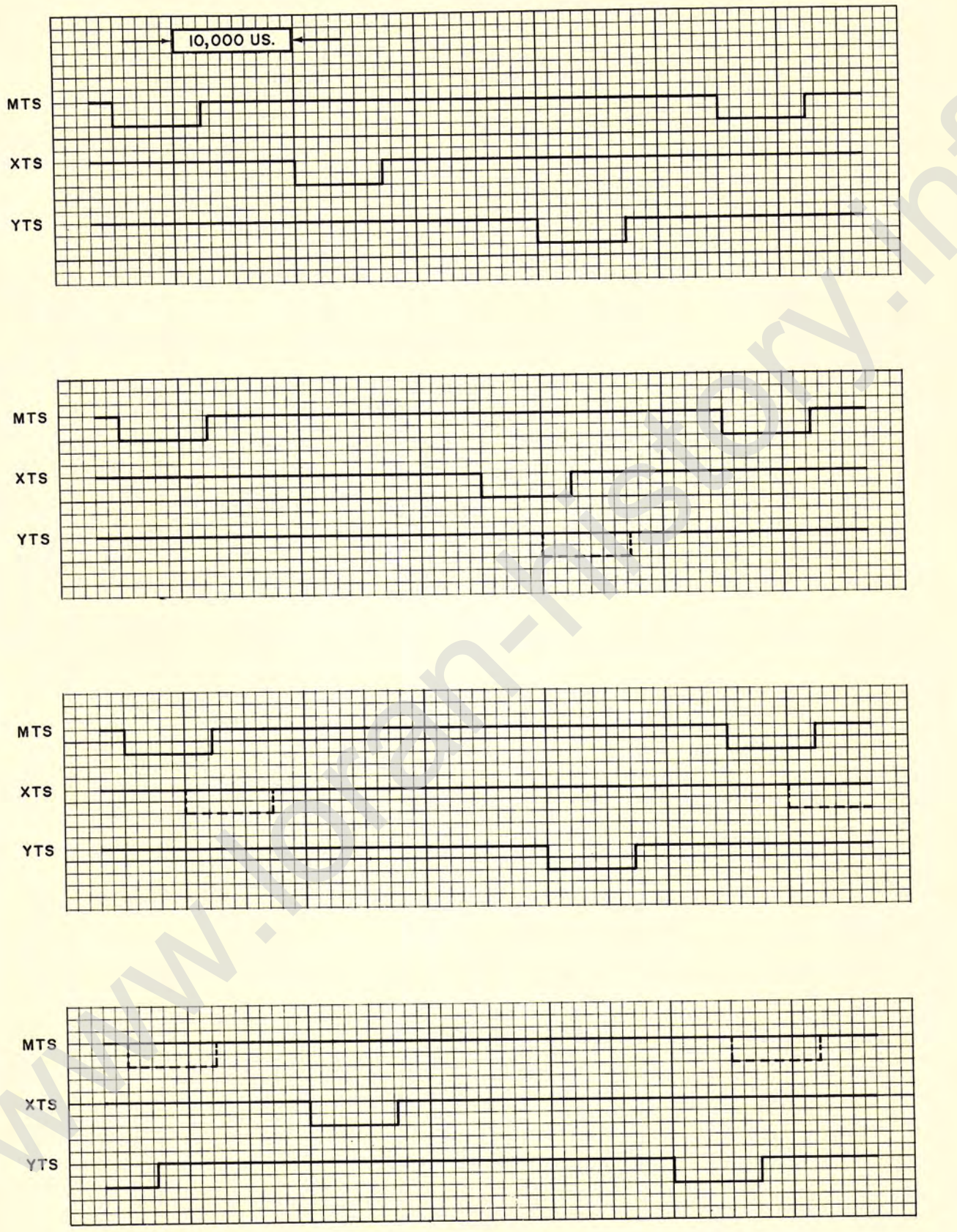


Figure 4-44. Slew Limit, Waveforms

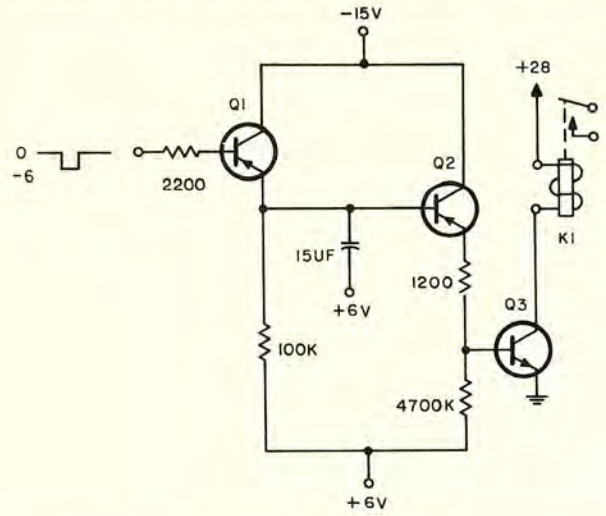


Figure 4-45. Peak Detector, Partial Schematic Diagram

(d) REFERENCE SIGNAL. - The reference 100-kc signal from the oscillator is continuous. To allow the coding (polarity) of the reference signal to correspond to the desired coding of the master or slave signal, as many as six phase changes (180°) in the reference signal may occur during the period that a master or slave signal is being received. For example, the master 1 signal is coded ++--+-+-. Each of the eight coded carrier pulses are 200 microseconds in duration. For the purpose of this discussion, it is assumed that the no-carrier spacing between each of the coded pulses is 800 microseconds. (This is actually determined by the chain of Loran-C stations being received.) An example of this 100-kc reference signal is shown in figure 4-51. The reference signal for the master 1 signal would be as follows: 400 microseconds of positively coded 100-kc reference carrier; 1000 microseconds of positively coded 100-kc reference (the combination of which would be observed as 1400 microseconds of positively coded 100-kc reference); 1000 microseconds of negatively coded 100-kc reference; 1000 microseconds of negatively coded 100-kc reference (a combination that would be observed as 2000 microseconds of negatively coded 100-kc reference); 1000 microseconds of positively coded 100-kc reference; 1000 microseconds of negatively coded 100-kc reference; 1000 microseconds of positively coded 100-kc reference; and 1000 microseconds of negatively coded 100-kc reference. The initial reference for all the possible pulse groups is the same since the first pulse of the master and slave received r-f signals are, in every case, coded positively.

(2) ENVELOPE DERIVER (A501).

(a) GENERAL. - The envelope deriver is utilized to shift the phase of each received pulse by 180° after the 30-microsecond point. This allows the derived envelope detector to obtain the output described in the detector strobe unit and to control the associated servoloop.

(b) DETAIL. - See the schematic diagram shown in figure 6-125. The input signal is applied to terminals 12 and 13 of P501 and connected to a 5-microsecond delay line. This 5-microsecond delay is equivalent to a 180° phase shift for the 100-kc received r-f signal. The delayed signal is added to the originally received signal. The addition of these two signals produces the desired waveform. The position at which the crossover point occurs is dependent upon the relative amplitude of the two signals. For example, see figure 4-52.

The point at which crossover occurs may be set by adjusting potentiometer R501. For the crossover point to occur at the 30-microsecond point (30 microseconds after the beginning of the received r-f signal), the amplitude of the received signal and the received signal shifted in-phase by 180° must be equal at the 30-microsecond point. When the amplitude adjustment is set so that the crossover point occurs at the 30 microsecond point, the combined signal will be in-phase with the received signal for the first 30-microseconds and 180° out-of-phase for the remaining portion of the received signal. Notice that when the amplitudes are not equal at the 30-microsecond point, the phase change will occur at some point other than the 30-microsecond point.

Tube V501 is a twin triode with the two sections connected in parallel. The combined signal is coupled directly to grid pin 3 and across R512, a small resistor, to grid pin 7 of V501. Grid resistor R512 eliminates any tendency for the grid circuit to become self-resonant, while plate resistor R511 eliminates any tendency for the plate circuit to become self-resonant. The plate tank circuit consisting of L501, C501, and R506 provides the plate impedance which is resonant at 100 kc. Resistor R513 and capacitor C505 provide decoupling of the amplifier circuits from the power supply.

Tube V502 is connected as a squeegee driver which is utilized to produce the current swing necessary to develop a reasonable voltage across a low-impedance load. The signal is r-f coupled from the plates of V501 to grid 3 of V502. For the following discussion, see figure 4-53.

Equal current is flowing through V502A and V502B during the quiescent condition, thus no load current flows. The current through V502A increases as the input from V501 swings positive. A negative-going potential is applied to the grid of V502B from the plate of V502A, thereby causing less current to flow through V502B. This action effectively causes a current to flow from V502A through the load to ground.

By a similar analysis, it may be shown that as the grid of V502A swings negative, a current flows from the a-c load through tube V502A. The output to the a-c load is available at terminal 9 of V502B.

(3) STROBE BLOCKING OSCILLATOR (A1401-A1404).

(a) GENERAL. - The four strobe blocking oscillators (one for master, X-slave, Y-slave, and guard) receive an input from the monostable multivibrator in the code group generator, and, on the negative-going edge of the monostable multivibrator pulse, allows a strobe gate in the detector-strobe circuit to conduct. Depending upon the application of the circuit, either one of the monostable multivibrator

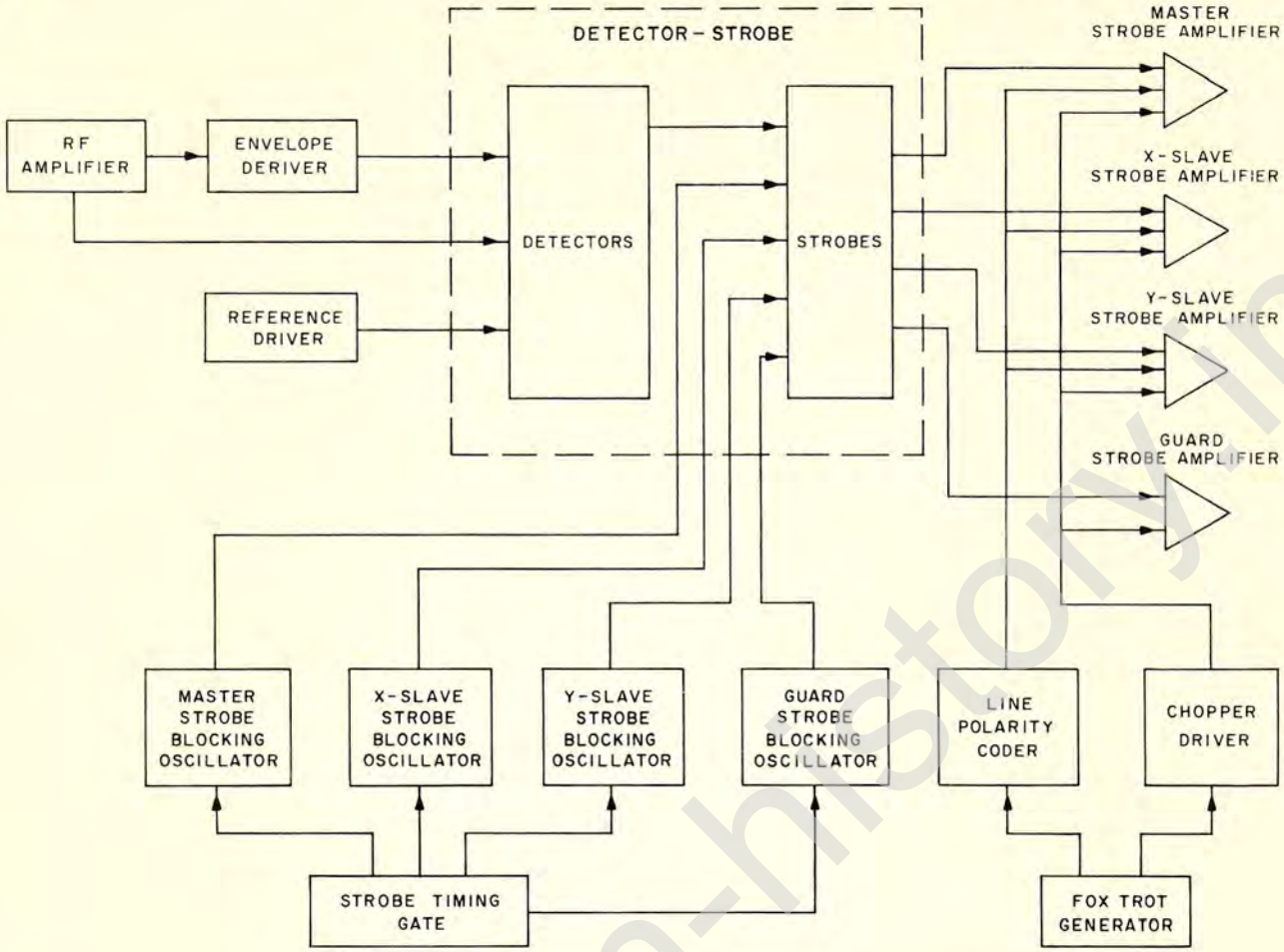


Figure 4-46. Detector-Strobe Section, Block Diagram

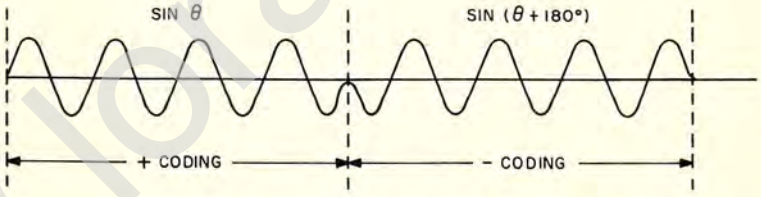


Figure 4-47. Coding in Loran-C System

inputs may be used to trigger the strobe blocking oscillator.

(b) DETAIL. - See the schematic diagram shown in figure 6-149. The input to the strobe blocking oscillator circuit may be one of two inputs, as shown in figure 4-54.

Emitter follower PNP transistor Q1 is coupled to PNP transistor Q2. Transistor Q2 will receive an output only on the negative pulses (positive-going edges cut off Q1) because of the a-c coupling employed. Transistor Q2 will conduct only when a negative signal is applied to its base. When Q2 begins to conduct, a current begins to flow in the primary of T1, which is in the collector of Q2. This coil is transformer coupled to the emitter coil (ratio of 5-to-1), which drives the emitter in a negative direction. Transistor Q2 will conduct even harder when this happens to rapidly saturate the transistor. The action will reverse when saturation of the transformer is reached. The coupling will now help cut off Q2 quickly. The resulting output is a rapidly rising and declining waveform. Resistor R4 determines the width of the pulse at the top by limiting the current flow.

The output from the oscillator stage is applied to Q3. The coupling is essentially dc, but capacitor C7 helps speed up the action by assisting Q3 to conduct

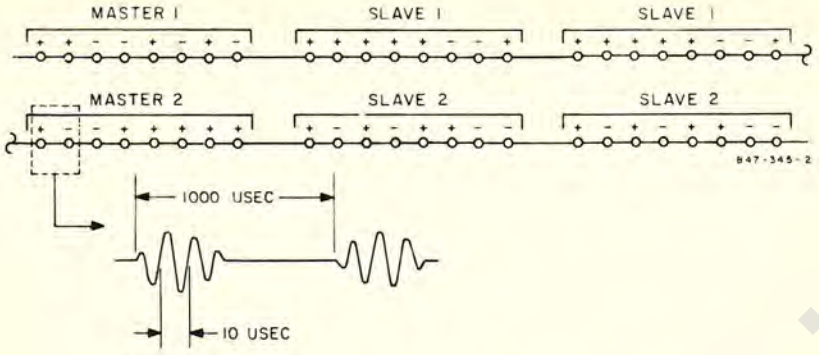


Figure 4-48. Received R-F in Loran-C System

on the a-c switching. Transistor Q3, an NPN transistor, will only conduct when its base becomes positive. This means that the -15 volts normally across R5 and R11 is raised to a positive value at the base of Q3 by the action which occurred in Q2. Transistor Q3 conducts and the collector will start dropping from its stable condition of +15 volts. This negative transient is applied to transformer T2.

The coupling of T2 applies the blocking oscillator pulse to three strobe gates. The strobe gates are located in the detector-strobe. To understand the action of the components in one of these circuits, they must be considered together with a strobe gate. See figure 4-55 for a simplified schematic.

The transformer windings of T2 are wound so that the secondary of T2 will be positive in the direction shown on the diagram. When the voltage of pulses applied to the gate exceeds the stored voltage of the capacitor, the Zener diode will conduct and current will flow in the diode gate. The detector output will then be permitted to pass through the gate to the remainder of the circuit. Since this is only for the very brief period of time that the strobe blocking oscillator is in action, the effect is that the strobe can be accurately timed to sample the detector output at the same portion of every cycle.

Diodes CR1 through CR5 in the strobe blocking oscillator circuit limit the peaks of any surging transients that may occur.

(4) STROBE TIMING GATE (A1317). - The strobe timing gate circuit provides triggering pulses for the strobe blocking oscillators. For a discussion of this circuit, refer to paragraph 4-2*g*(11).

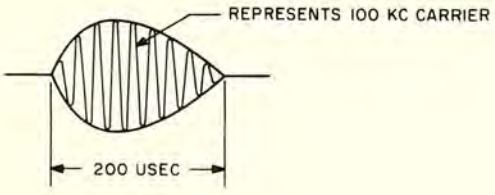


Figure 4-49. Example of a Loran-C Pulse

(5) FOX-TROT GENERATOR (A1322).

(a) GENERAL. - The fox-trot generator uses the MTS, 1/2 PRR, 1/4 PRR signals, and a standard toggle circuit to produce a particular switching waveform of 0 and -6 volts. The block diagram of the fox-trot generator is shown in figure 4-56 and the relationship of the output and the input signals is shown in figure 4-57. The output signals from the fox-trot generator are used in the detector-strobe portion of the receiver as polarity coding information.

(b) DETAIL. - The schematic diagram of the fox-trot generator is shown in figure 6-148 and the time relationships of the pertinent waveforms are shown in figure 4-57. The input zero AND gate is shown in figure 4-58. The inputs to the gate are either 0 or -6 volts. The +15 volts applied to resistor R15 is dropped to a slightly positive voltage at the anode junction of the diodes. When either one or both of the cathodes of CR3 and CR10 are at -6 volts, the output at the anode junction will be established at -6 volts. Both the cathodes must be at 0 volt before the output will be zero.

The zero OR circuit of figure 4-56 is composed of the components shown in figure 4-59. Again, the two inputs are either 0 or -6 volts. The -15 volts applied to resistor R14 is dropped to a value slightly more negative than -6 volts at the junction of the diodes. When either one or both of the anodes of CR13 and CR12 are at 0 volt, the output at the diode junction will be 0 volt. The output will only be -6 volts when both inputs are -6 volts.

Diodes CR2 and CR9 are the inputs to the toggle circuit on the board. Notice that their anodes are connected together to trigger the circuit regardless of the state the toggle was in at rest. For an explanation of the toggle, refer to paragraph 4-2*d*(1). The toggle will change state on any positive-going trigger. Both outputs from the toggle are applied to an inverter stage. This inverter isolates the output from

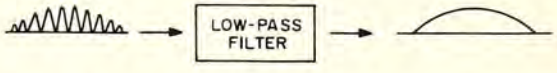


Figure 4-50. Output from Envelope Detector with Inputs in Phase

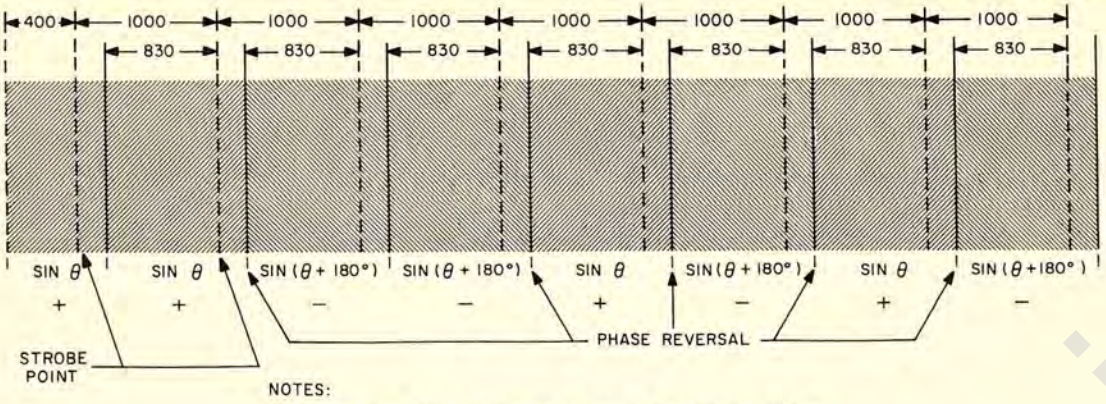


Figure 4-51. Master-1 100 Kc Reference Signal Coding

the toggle and insures that the -6 volt output is precisely -6 volts. Diodes CR5, CR6, CR11 and CR14 are -6-volt clamps.

(6) REFERENCE DRIVER (A2703).

(a) GENERAL. - The reference driver module receives the $\overline{MXY}$ TS, the M100KC, the X100KC, and the Y100KC signals, phase codes these signals, and applies the phase-coded output to the detector-strobe. The circuit consists of an input OR gate, a 200-kc filter, an emitter follower, a coupling transformer, another OR gate, and an output emitter follower.

(b) DETAIL. - See the schematic diagram shown in figure 6-172. The initial OR gate consists of CR1 through CR4 with the following inputs applied to the respective diodes: M100KC MTS, X100KC XTS, Y100KC YTS, and $\overline{MXY}$ TS. The relative waveforms and their time relationships are shown in figure 4-60.

Each of the individual station inputs (MTS, XTS, and YTS) are at a level of -6 volts superimposed with 100 kc. When none of the station inputs are at -6 volts, then $\overline{MXY}$ TS is at -6 volts. The output of the OR gate is then applied to a tuned circuit consisting of L1 and C1. The resonant frequency of this tank circuit is 200 kc. Therefore, the circuit is effectively a second harmonic filter for the 100-kc frequency.

Transistor Q1 is an ordinary emitter follower which provides isolation, but leaves the waveform unchanged. The output circuit in the emitter of Q1 includes a biasing resistor, R2, bypassed by capacitor C2, and the primary of transformer T1. The transformer is wound to a 1-to-1-to-1 ratio, with the coupling directions as marked on the diagram. The output from one secondary is in-phase with the signal on the primary and the output from the other secondary is 180° out-of-phase with the input. These secondary outputs are combined in an OR gate. Inputs PC (Phase Code) and $\overline{PC}$ (Phase Code complement) are the means of triggering the OR gate to permit the phase coding to occur. These two inputs are complementary so that while one is 0 volt, the other is -6 volts. To follow the action of the gate, it is assumed that PC is -6 volts and $\overline{PC}$ is 0 volt at a given instant of time. The secondary between terminals 5 and 6 of transformer T1 appears as a short to dc and -6 volts is applied to the cathode of CR6. This diode conducts and applies -6 volts superimposed with the output of secondary 5-6 to the base of transistor Q2. This is the phase coding which is 180° out-of-phase with the input. At the same time, $\overline{PC}$ is 0 volt and the other secondary, between terminals 3 and 4, is blocked from the output. This is because diode CR5 will not conduct to allow this output to be applied on the base of Q2.

During the time $\overline{PC}$ is -6 volts and PC is zero, output from secondary 3-4 (the in-phase secondary) will be applied to Q2, and secondary 5-6 will be blocked. The net output to Q2 is 100 kc from MTS, XTS, and YTS, properly coded, and at a level of -6 volts. Transistor Q2 is an emitter follower. Capacitor C3 a-c couples the combined output to terminal 4, from where it is subsequently applied as the reference driver input to the detector-strobe.

(7) CHOPPER DRIVER (A2702).

(a) GENERAL. - The chopper driver is a switching module that provides the necessary switching current to drive four, series-connected chopper coils. A square-wave input (0 to -6 volts at a rate determined by the fox-trot generator) to the printed circuit board provides the drive current that triggers the 7-stage transistor chopper driver. The output from the board is applied to the chopper coils. When the input is 0 volt (ground potential), the first output terminal is 0 volt (ground potential) and the second output is +24 volts. When the input is -6 volts, the first output is +24 volts, while the second output is 0 volt (ground potential). Thus, in the two cases, current flows first in one direction through the chopper coils and then in the opposite direction.

(b) DETAIL. See the schematic diagram shown in figure 6-171. The input signal is coupled to the base of NPN transistor Q3 and the base of PNP transistor Q7. The collector output of NPN transistor Q3 is coupled to the base of both transistors Q1 and Q2 to control the bias current to these two transistors. The collector output of PNP transistor Q7 is coupled to the base of NPN transistor Q6 and controls its bias current. The collector output of NPN transistor Q6 is coupled to the base of both PNP transistors Q4 and Q5 and controls the bias current to both transistors. When the input signal to terminal 1 is 0 volt (ground potential), transistor Q3 is biased into

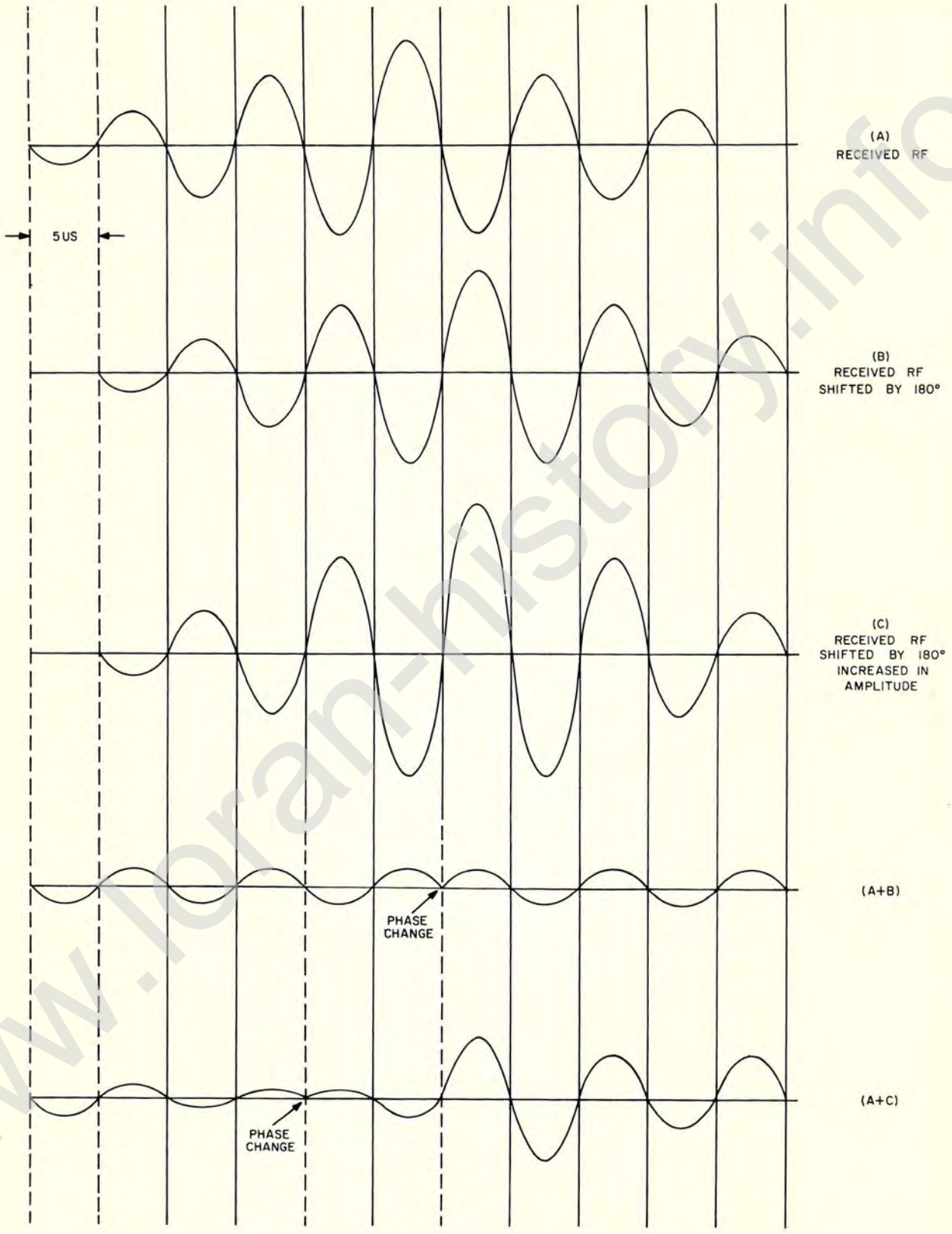


Figure 4-52. Shifting Crossover Point by Waveform Audition

the saturated condition while transistor Q7 is biased at cutoff. Transistor Q3 collector now supplies -6 volts to the base of both transistors Q1 and Q2, placing both transistors into saturation. When transistor Q1 is in the saturated state, ground potential is applied to output terminal 12. At the same time, transistor Q2 is in the saturated state and +24 volts is applied to output terminal 14. Since transistor Q7 is in the cutoff condition, transistor Q6 is cut off, which, in turn, places transistor Q4 and Q5 in the cutoff condition.

Transistor Q3 is placed in the cutoff condition and transistor Q7 is saturated when the input to terminal 1 is -6 volts. When transistor Q3 is in the cutoff condition, the -6 volts is removed from the collector, thereby placing transistors Q1 and Q2 in the cutoff condition. This removes the ground potential applied to output terminal 12 and the +24 volts applied to output terminal 14. Since transistor Q7 is in the saturated condition, ground is applied from the collector of Q7 to resistor R11, saturating transistor Q6. This places -6 volts on the collector of transistor Q6, which, in turn, saturates transistors Q4 and Q5. The output at terminal 12 is +24 volts when transistor Q4 is in the saturated condition. The output at terminal 14 is ground potential when transistor Q5 is in the saturated condition.

Zener diode CR3 is utilized to produce a 4-volt drop from the 28-volt supply in order to supply +24 volts to the emitter of both transistors Q1 and Q4. This is the + 24 volts which eventually appears at output terminal 12 or output terminal 14.

Diodes CR1 and CR2 supress any negative transient spikes that might occur when the current is reversed through the coils of the chopper unit.

(8) LINE POLARITY CODER (A2701).

(a) GENERAL. - The line polarity coder drives one set of choppers in the strobe amplifiers with a 400-cps signal to provide an easily amplified signal which is later rectified. The driving signals produced in the line polarity coder are a 6-volt, 400-cps signal and its complement (another 400-cps signal shifted by 180°). The 6-volt a-c output signal is derived from the 115-volt, 400-cps input line. This 115-volt input is applied to the primary winding of a stepdown transformer that produces 12 volts on the secondary. The secondary is center-tapped to produce a 6-volt output between the center-tap and either end terminal of the secondary winding.

With 0 volt (ground potential) applied to the input from the fox-trot generator, the 6-volt ac is received across the center-tap and terminal 5 of the secondary of transformer T1. This 6-volt a-c signal will be considered as the reference, or 0°. The 6-volt a-c signal, which is shifted by 180°, is received across the center tap and terminal 3 of the secondary of transformer T1.

(b) DETAIL. - See the schematic diagram shown in figure 6-170. The 115-volt, a-c input is received by terminals 1 and 2 of the printed circuit board and connected to terminals 1 and 2 of the primary of transformer T1. Terminal 1 is also connected to diode rectifier CR6, filter C1 and R15, and Zener diode regulator CR5. The +28 volts dc obtained across Zener diode regulator CR5 furnishes the collector supply voltage for transistors Q5 and Q6. Bias current for the base of transistors Q1 and Q2 is obtained from the collector of transistor Q5 while the bias current for the base of transistors Q3 and Q4 is obtained from the collector of transistor Q6. The input from the fox-trot generator (0-, -6-volt square wave) is received by terminal 13 of the printed circuit board, and coupled through resistor R7 to the base of NPN transistor Q5. This input is also coupled through resistor R12, one-half of a voltage divider with resistor R13, to the base of transistor Q7.

When 0 volt (ground potential) is received from the fox-trot generator, transistor Q7 is biased in the cut-off condition. The base-emitter junction of transistor Q5 is forward biased to saturation; therefore, the collector voltage is established at approximately -5.5 volts. Transistor Q6 is cut off since it receives base voltage from the cut-off collector of Q7 through resistor R10. This voltage is -6 volts. Transistors Q3 and Q4 are subsequently kept cutoff by the +28-volt supply.

Transistors Q1 and Q2 are not kept cutoff by the +28-volt supply since the collector of Q5 has been established at approximately -5.5 volts. This voltage is applied across resistor R1 to the base of transistor Q1 and across resistor R2 and CR7 to the base of transistor Q2. Terminal 5 of the secondary of transformer T1 is connected in series with diode CR1 to the emitter of transistor Q1 and in series with diode CR2 to the collector of transistor Q2.

When terminal 5 of the secondary of transformer T1 is a negative potential, diode CR1 is reverse biased while diode CR2 is forward biased, allowing negative potential to be applied to the collector of transistor Q2. Since the base-emitter junction of transistor Q2 is forward biased, the transistor is saturated and grounds terminal 5 of the secondary of transformer T1. When terminal 5 of the secondary of transformer T1 is at a positive potential, diode CR2 is reverse biased while diode CR1 is forward biased. Diode CR1, therefore, applies the positive potential to the emitter of transistor Q1. The base-emitter junction of transistor Q1 is forward biased, placing the transistor in the saturated condition and grounding terminal 5 of the secondary of transformer T1. Thus, when the fox-trot generator input is 0 volt (ground potential), the output voltage is generated across the center-tap terminal 4 and terminal 5 of the secondary of transformer T1.

When the fox-trot generator input to terminal 13 of the printed circuit board is -6 volts, transistor Q5 is biased to cutoff and Q7 is biased in the saturated condition. The collector of Q5 returns to the potential of the +28-volt supply when Q5 cuts off. In turn, this establishes a positive voltage on the bases of Q1 and Q2, cutting off these transistors. When Q7 saturates, the collector of Q7 becomes very near to ground potential. The voltage applied through R10 to the base of Q6 is less negative than the -6 volts applied to its emitter. Therefore, Q6 conducts to near saturation, establishing its collector potential at approximately -5.5 volts. The 5.5 volts is placed across resistor R5 to the base of transistor Q3 and across resistor R6 and diode CR8 to the base of transistor Q4. Terminal 3 of the secondary of T1

is connected in series with diode CR3 to the emitter of transistor Q3 and in series with diode CR4 to the collector of transistor Q4. When terminal 3 of transformer T1 secondary swings negative, diode CR3 is reversed biased while diode CR4 is forward biased, applying the negative potential to the collector of transistor Q4. Transistor Q4 base-emitter junction is forward biased; therefore, terminal 3 of the secondary of transistor T1 is grounded. When terminal 3 swings positive, diode CR4 is reverse biased while diode CR3 is forward biased; applying the positive potential to the emitter of transistor Q3. Transistor Q3 base-emitter junction is now forward biased, saturating the transistor, and applying ground to terminal 3 of the secondary of transformer T1. Thus, when the fox-trot generator input is -6 volts, the output voltage is generated across center-tap terminal 4 and terminal 3 of the secondary of T1. This output is 180 degrees out-of-phase with the output generated across terminals 5 and 4 of the secondary of transformer T1.

Diodes CR1 and CR3 eliminate the negative voltage from appearing at the emitter of transistors Q1 and Q3. Diodes CR7 and CR8 are 10-volt Zener diodes that limit the maximum positive voltage applied to the bases of Q2 and Q4 to +18 volts. These diodes protect the circuit from exceeding the base-emitter reverse bias breakdown voltage when the transistors are in the cut-off condition.

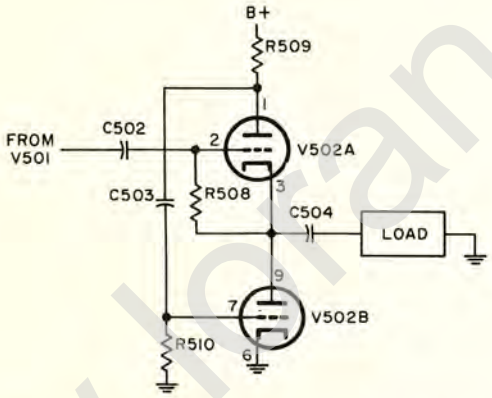


Figure 4-53. Squeegee Output Stage, Partial Schematic Diagram

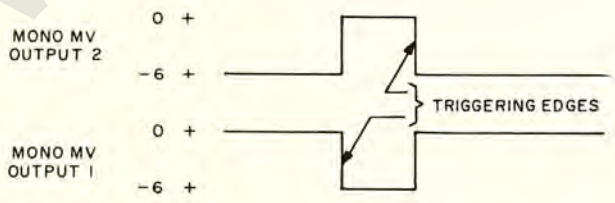


Figure 4-54. Triggers for Strobe Blocking Oscillators

(9) DETECTOR-STROBE (A401).

(a) GENERAL.

1. DETECTOR-STROBE DETECTORS. - The detector-strobe unit contains three detectors. These detectors are: (1) the cycle detector, (2) the envelope detector, and (3) the derived envelope detector.

The cycle detector compares the 100-kc signal from the r-f amplifier with a 100-kc signal from the reference driver. The output of the cycle detector is sampled and the information obtained is delivered to a servoloop. The servoloop adjusts the phase of the reference driver until a 90° phase relationship with the r-f amplifier signal is obtained. This 90° phase relationship is maintained since any other phase relationship would be detected as an error signal and produce corrective signaling to the servoloop. If the phase is continuously changing, this may be observed as a change in the reference oscillator frequency. Therefore, this servoloop is known as the automatic frequency control. The envelope detector provides information which is sampled and supplied as signaling through a servoloop to adjust the gain of the r-f amplifier.

When a cycle lock is obtained and the action which initiated the slewing of the reference signal is removed, the reference signal and the received r-f signal are positioned with respect to each other by the action of the derived envelope sampling. This allows the sampling pulse to occur at the 30-microsecond point of the envelope. The detected envelope output must be positive to obtain a cycle lock. A positive output indicates that the reference and received r-f signal coding is coincident. The derived envelope sampling pulse is now sampling a portion of the derived envelope. The sampled information will determine the cycle of the received r-f signal on which the reference signal is locked. This allows the received r-f signal and the reference signal to be cycle-locked so that the sampling pulse will occur at the 30-microsecond point of the received r-f signal.

2. GUARD STROBES. - The guard sample pulse occurs approximately 45 microseconds before each reference master and slave signals. This guard sample pulse controls a visual indication that warns the operator when the detector-strobe unit is synchronized with a reflected sky wave. See figure 4-61.

3. OUTPUTS. - The three sampling pulses that sample the output of the cycle detector, the envelope detector, and the derived envelope detector occur at a fixed time relation with respect to the reference signal. This time relation is fixed so that the sampling pulse occurs 830 microseconds after the beginning of each of the eight parts of the reference signal (if the Loran-C pulses are spaced 800 microseconds apart as in the example). See figure 4-51. The action of sampling the detector outputs is termed strobing.

The derived envelope detector input signal is obtained from the envelope deriver, which is described

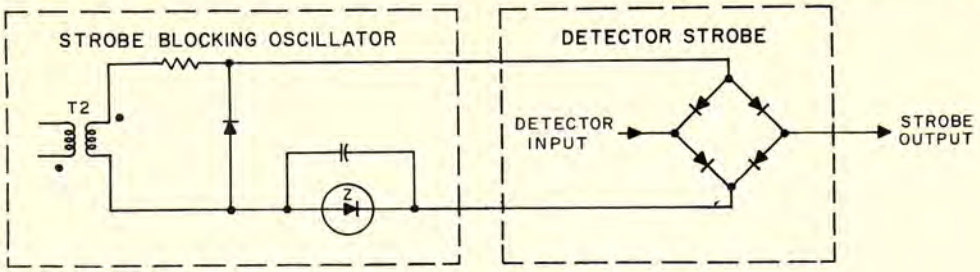


Figure 4-55. Strobe Gate, Simplified Schematic Diagram

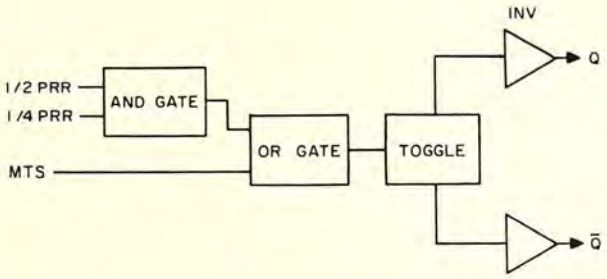


Figure 4-56. Fox-Trot Generator, Block Diagram

in paragraph 4-2*h*(2). After a cycle lock is obtained, the derived envelope detector provides an output that causes the servos to position the strobe point at the 30-microsecond point on the pulse. The output of the derived envelope detector output, after filtering, is shown in figure 4-62.

(b) DETAIL.

1. DETECTOR UNITS. - An example of the detector circuits is shown in figure 4-63. Outputs are shown for the three combinations of inputs which are utilized by the detector strobe unit.

When the inputs are in-phase, terminals A of transformers T1 and T2 are both either positive or negative. When terminals A of T1 and T2 are positive, terminals C of T1 and T2 are positive while terminal E of T1 and terminal D of T2 are negative. This places a positive potential at the junction of diodes CR1 and CR3, the junction of CR6 and CR8, and the junction of CR5 and CR6. A negative potential is applied to the junction of diodes CR1 and CR2, diodes CR2 and CR4, and CR5 and CR7. The four diodes of bridge II are reverse-biased, and may be considered as an open circuit. The diodes of bridge I are forward-biased, approximately grounding terminal E of T1. Output terminal D is placed at a positive potential since it is effectively at the midpoint between terminal E and the positive potential at C.

When the A terminals of T1 and T2 are negative, the junction of diodes CR5 and CR6, CR1 and CR3, and CR6 and CR8 are negative. Terminal E of T1 and terminal D of T2 are positive, which places the junction of diodes CR1 and CR2, CR2 and CR4, and CR5 and CR7 at a positive potential. The four diodes of bridge I are reverse-biased, and may be considered as an open circuit. The diodes of bridge II are forward-biased. Output terminal D is again placed at a positive potential since it is effectively at the midpoint between the approximate ground on terminal C and the positive potential at terminal E.

Similar analysis may be applied to the circuit for inputs 90° and 180° out-of-phase to determine the output waveshapes.

2. INPUTS.

a. 100-KC REFERENCE. - For the schematic diagram of the detector-strobe, see figure 6-124. The 100-kc reference signal is received by terminal 13 of plug P401-3 and connected to the base of transistor Q401. The secondary of transformer T401 (with resistor R401 connected in parallel) is the collector load for transistor Q401. The secondary of T401 is connected directly to the base of transistors Q402 and Q403. Transistors Q402 and Q403 are connected in push-pull, with the primary of transformer T402 as the output load. Secondary output terminal 6 of transformer T402 furnishes the 100-kc reference signal to the junctions of diodes CR467 and CR468, and CR463 and CR464. Secondary output terminal 4 of transformer T402 furnishes the 100-kc reference signal to the junctions of diodes CR465 and CR466, and CR461 and CR462. These eight diodes form the cycle detector.

Secondary output terminal 6 of transformer T402 is connected to the delay line, consisting of inductors L401 and L402 and capacitors C403, C404, and C424, which shifts the phase of the 100-kc reference signal by 90°. The output of the delay line is applied to the envelope detector (junctions of diodes CR455 and CR456, and CR459 and CR460) and the derived envelope detector (junctions of diodes CR451 and CR452, and CR447 and CR448).

The secondary output terminal 4 of transformer T402 is also connected to the delay line, which shifts the phase of the 100-kc reference signal by 90°. The output of this delay line is applied to the envelope detector (junctions of diodes CR458 and CR457, and CR454 and CR453) and the derived envelope detector (junctions of diodes CR450 and CR449, and CR446 and CR445).

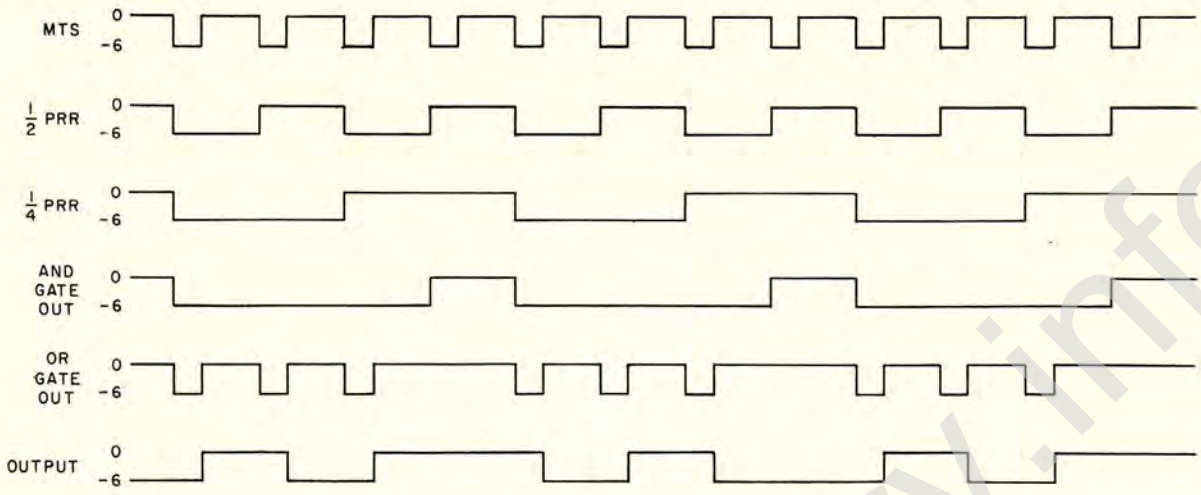


Figure 4-57. Fox-Trot Generator, Waveshapes

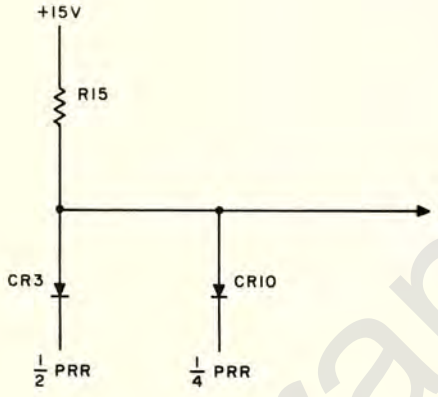


Figure 4-58. Fox-Trot Generator, Zero AND Gate

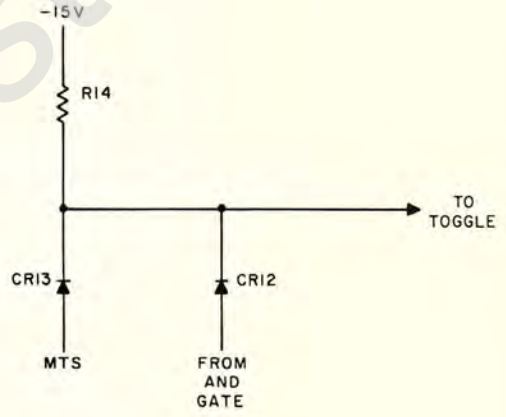


Figure 4-59. Fox-Trot Generator, Zero OR Gate

b. 100-KC R-F SIGNAL. - The 100-kc signal is received from the r-f amplifier at terminals 17 and 18 of P401-3 and coupled to terminals 1 and 2 of transformer T403. The secondary of transformer T403 consists of two separate windings. Secondary output terminal 4 of T403 furnishes the received 100-kc rf to the junction of diodes CR462 and CR463 of the cycle detector, while secondary output terminal 6 of T403 furnishes the received 100-kc rf to the junction of diodes CR465 and CR468 of the cycle detector.

Secondary terminal 6 of T403 furnishes the received 100-kc r-f signal to the junction of diodes CR454 and CR455 of the envelope detector while secondary output terminal 5 of T403 furnishes the received 100-kc r-f signal to the junction of diodes CR457 and CR460 of the envelope detector.

c. DERIVED ENVELOPE. - The derived envelope input is received from the envelope deriver unit at terminals 9 and 10 of jack P401-3 and connected to primary terminals 1 and 2 of transformer T404. The derived envelope signal across the secondary is detected in the same manner as in the cycle and envelope loops.

3. OUTPUTS. - The cycle detector outputs are obtained from terminals 3 and 4 of transformer T403 secondary. Resistors R443 and R444 form a voltage divider, the midpoint of which is used as the output. This output is applied through a filter consisting of capacitors C409, C410, and C419, inductor L405, and resistors R447 and R430, to four diode bridge gates. The four diode bridge gates receive the master, slave, and guard strobing pulses and allow these strobing pulses to sample the data output of the filter.

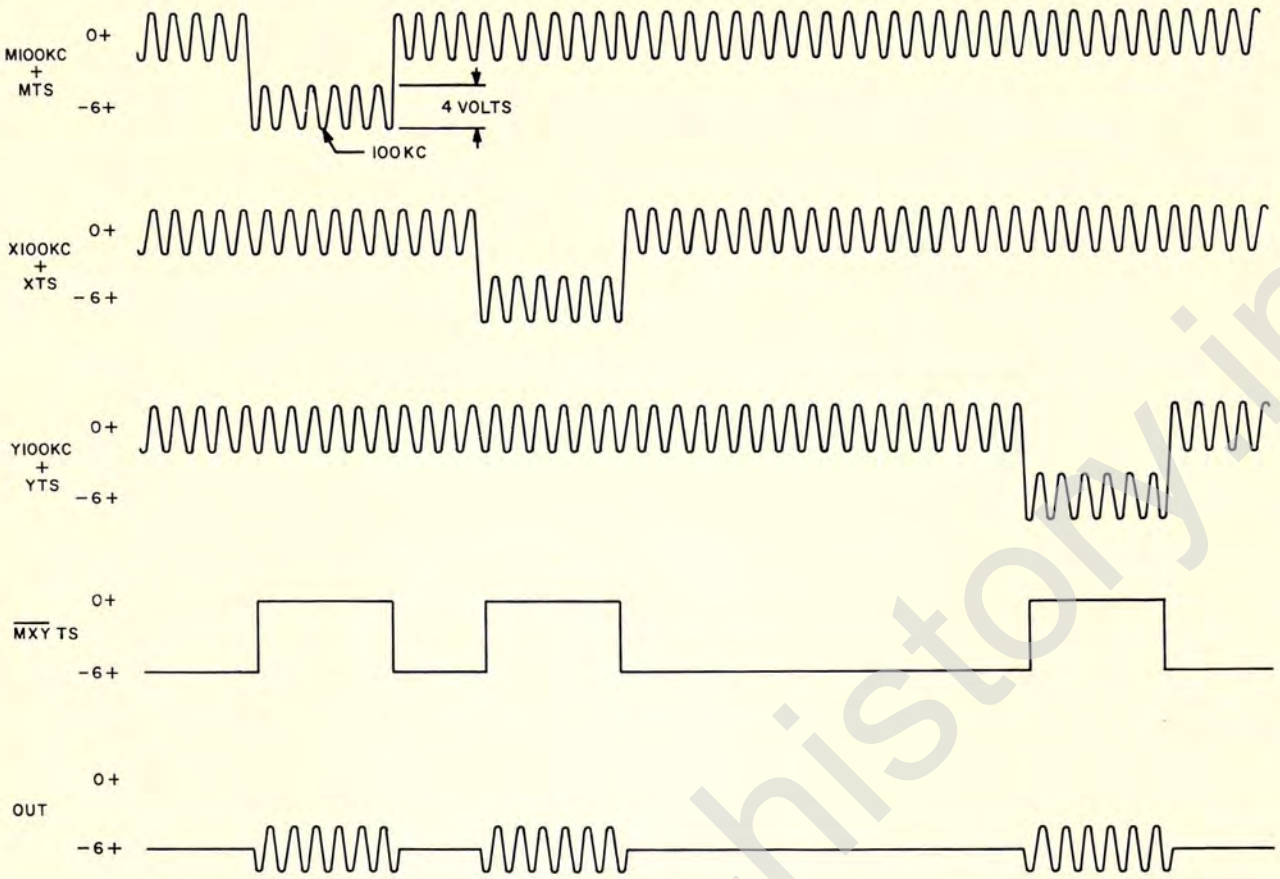


Figure 4-60. Reference Driver, Waveshapes

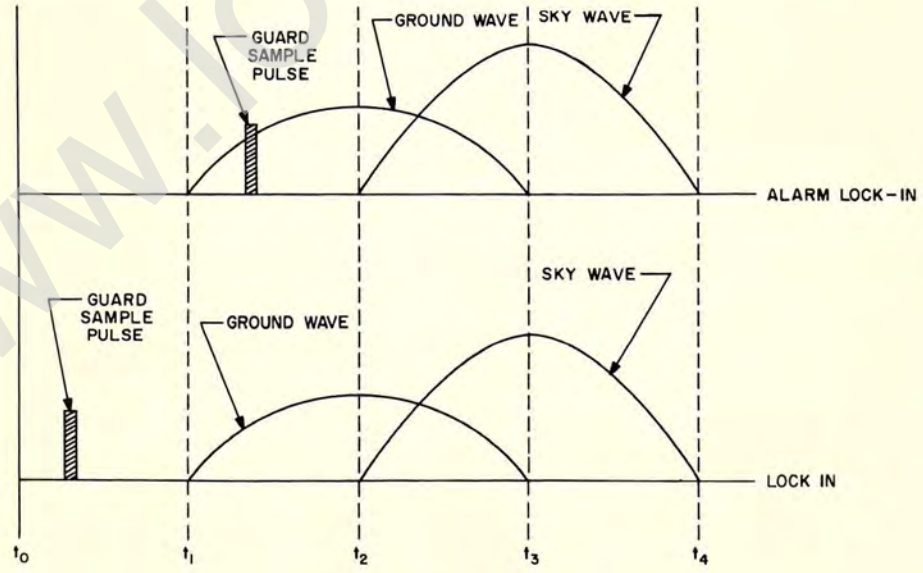


Figure 4-61. Guard Strobe Action

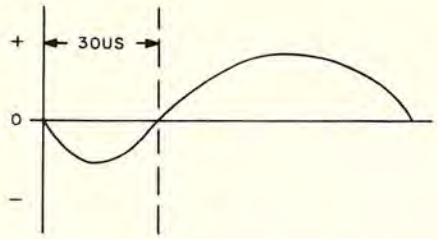


Figure 4-62. Derived Envelope Detector Output

The envelope detector outputs are obtained from terminals 5 and 6 of transformer T403 secondary. Resistor R441 and R442 form a voltage divider, the midpoint of which is used as the output. This output is applied through a filter consisting of capacitors C407, C408, and C418, inductor L404, and resistor R446, to four diode bridge gates. The four diode bridge gates receive the master, slave, and guard strobing pulses and allow these strobing pulses to sample the data output of the filter.

The derived envelope detector output is obtained from the secondary of transformer T404. Resistors R439 and R440 form a voltage divider, the midpoint of which is used as the output. This output is applied through a filter consisting of capacitors C405, C406, and C417, inductor L403, and resistor R445, to three diode bridge gates. These three diode bridge gates receive the master and slave strobing pulses and allow these strobing pulses to sample the data output of the filter.

The filter output of the derived envelope detector is coupled through R426 and C411 to the base of transistor Q404. The collector output of Q404 is directly coupled to the base of transistor Q405. One output is coupled through capacitor C416 (from the emitter of transistor Q404) and one output is coupled through C420 (from the emitter of transistor Q405). These outputs, separated by 180°, are available at terminals 2 and 4 of plug P401-3 as the derived envelope signal. They may be used as monitor signals for the indicator.

Similarly, the filter output of the envelope detector is coupled through R428 and C412 to the base of transistor Q406. The collector output of transistor Q406 is directly coupled to the base of transistor Q407. One output is coupled through capacitor C422 (from the emitter of transistor Q406) and one output is coupled through C423 (from the emitter of transistor Q407). These outputs, separated by 180°, are available at terminals 6 and 8 of jack P401-3 as the envelope signal. They may be used for monitor signals by the indicator.

4. STROBES. - The strobing action of the strobe portion of the detector-strobe module is described in paragraph 4-2*h*(3)*(a)*.

5. OPERATION. - First in the operating order of the receiver is the synchronization of the master reference signal with the received r-f master signal. This action will synchronize both the master 1 and master 2 signals. After the operator has initiated the necessary action, the reference signal position is moved with respect to the received r-f signal. This action is referred to as slewing.

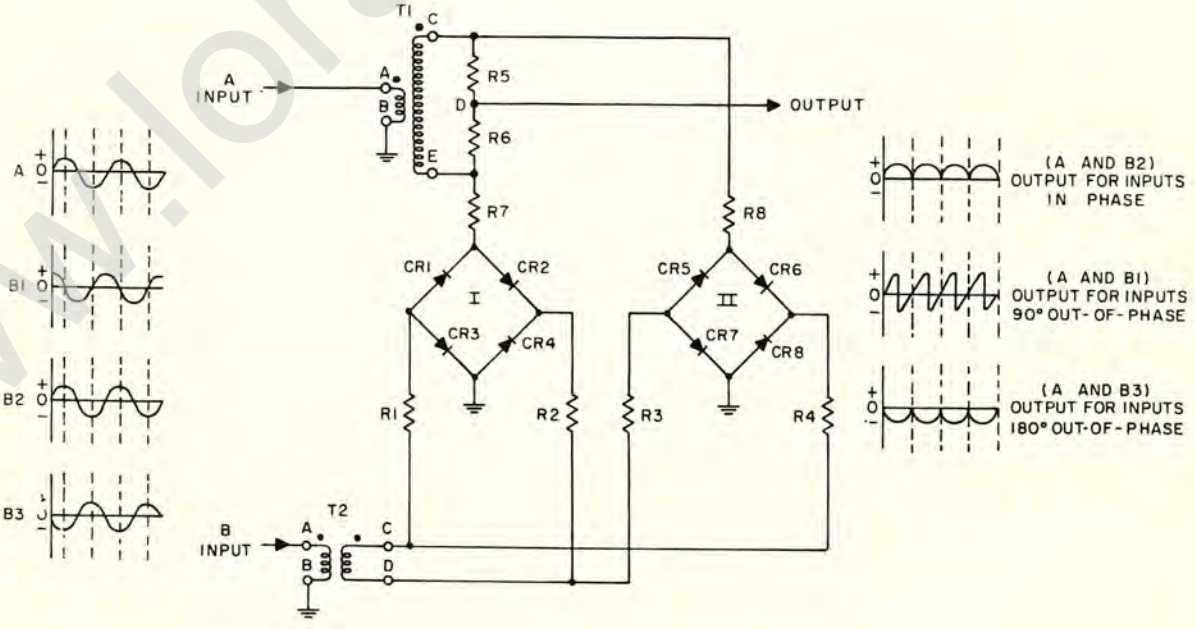


Figure 4-63. Detector Contained in Detector-Strobe Unit, Example Schematic Diagram

The correct integrated outputs of the derived envelope detector are present only when coincidence occurs between the received master r-f signal and the master reference. When the signals begin to coincide, the strobe pulses sample some portion of the derived envelope detector output, the envelope detector output, and the cycle detector output. The initiated slewing action may now be removed, the slewing being transferred to the servoloop that receives the sampled derived envelope detector output. The servoloop that receives the sampled output of the cycle detector sets the phase of the master reference signal 90° from the received master r-f signal. When this phase difference is exactly 90°, the cycle detector output is an a-c signal which, when filtered, produces no output. Thus, the cycle detector servoloop is in the null condition.

A cycle lock has now been obtained and the master reference signal is 90° out-of-phase with the received r-f signal. The reference master signal is coupled through a 2.5-microsecond delay line, which changes the signal phase by -90° so that it is again in-phase with the received master r-f signal. This shifted signal is applied as the reference input signal to the derived envelope and envelope detector.

The outputs to the derived envelope and envelope strobing pulses are as shown in figures 4-50 and 4-62.

The servoloop that receives the sampled output of the derived envelope detector continues the slewing action (while the cycle detector servoloop maintains the 90° phase relation between the received master r-f signal and the master reference signal) until the strobing pulses occur at the 30-microsecond point of the received master r-f signal. At this point, the derived envelope detector strobing pulse is occurring at the 30 microsecond point of the derived envelope detector output. This output is zero; thus, the servoloop is in the null condition. The master signal servoloop will automatically maintain these conditions while the above procedure is repeated for the slave signals.

Each slave phasing may be adjusted independently of the other and of the master phasing, as shown in figure 4-64.

(10) STROBE AMPLIFIER (A1405-A1407).

(a) GENERAL. - The strobe amplifier module consists of three separate subcircuits, one in each of three different loops. Although not identical, the three subcircuits are quite similar and generally operate in the same manner. A simplified schematic diagram of one of these subcircuits appears in figure 4-65.

The input to each one of the subcircuits is an error signal which has been detected in the detector-strobe module. The signal consists of an a-c component containing the error information, and an unwanted d-c offset. This input is chopped at a slow repetition rate to produce a square wave of irregular time duration. For the purpose of this discussion, the rate of this chopper-input circuit may be thought of as being approximately 5 cycles per second. Actually, the rate is determined by the fox-trot generator that drives the chopper. The output from the contacts of the chopper is a square wave about a zero reference. The chopper action removes the d-c offset. A second chopper, driven by a 400-cps signal, superimposes a further signal on the waveform. The combined signal is now a 5-cps square wave modulated with a 400-cps square wave.

This combined signal is a-c coupled to a high impedance circuit and then to a 2-stage amplifier. A-c coupling is employed throughout the circuit. The peaks are removed as the 400-cps square wave passes through the amplifier stages, and the smoothed signal is applied to the output transformer. The diode gates, acting as switches, apply grounds to either end of the output transformer at the 400-cps rate, phase-reversed at the rate of the fox-trot generator. The signal that drives the diode gate is applied from the line polarity coder. The resultant output is all positive, rectified error information which is used in subsequent circuits in the receiver.

As mentioned above, all three subcircuits are similar. However, there is one difference which is peculiar to the subcircuit in the derived envelope loop. A tachometer phase signal is inserted at the base of Q13. This signal is added to the regular signal and is used later in the derived envelope loop to provide damping. The tachometer signal is corrected by balance control R62.

The amplifier stages are standard a-c coupled amplifiers, employing partially bypassed emitter resistors. The chopper-input circuit and the diode gate switches are discussed in detail below.

(b) DETAIL.

1. CHOPPER INPUT. - The chopper operating at an approximate 5-cps rate (actually determined by the rate of the fox-trot generator) applies ground first at the top and then at the bottom of the circuit shown in figure 4-66 to produce a square-wave output. Any d-c offset present at the input of the circuit will be removed at the output.

Assume an infinite time constant and a sufficient length of operating time for the conditions to become stabilized. Also, at the first instant of time, assume the application of -1 volt at the input and ground at the top. Since there is no d-c offset, the square-wave voltage will be as follows. A charge of -1 volt will build up between the two capacitors and ground, as shown in A of the figure. During the second interval, the application is as shown in B of the diagram. The ground is removed from the top and applied at the bottom. The input voltage is now +1 volt. With respect to ground, the voltage is as shown across the previously charged capacitor so that the voltages across the two capacitors are in the same direction. This results in a +2 volts at the top of the circuit. The two resistors are of equal value, resulting in an effective voltage divider to ground and an output of +1 volt.

During the third interval, the conditions return to the state of the first interval. Ground is now applied at the top and -1 volt is applied to the input. The capacitor at the top charges to -1 volt in the direction shown and the bottom capacitor retains a charge from the previous interval. The potential is -2 volts between the bottom of the circuit to the ground at

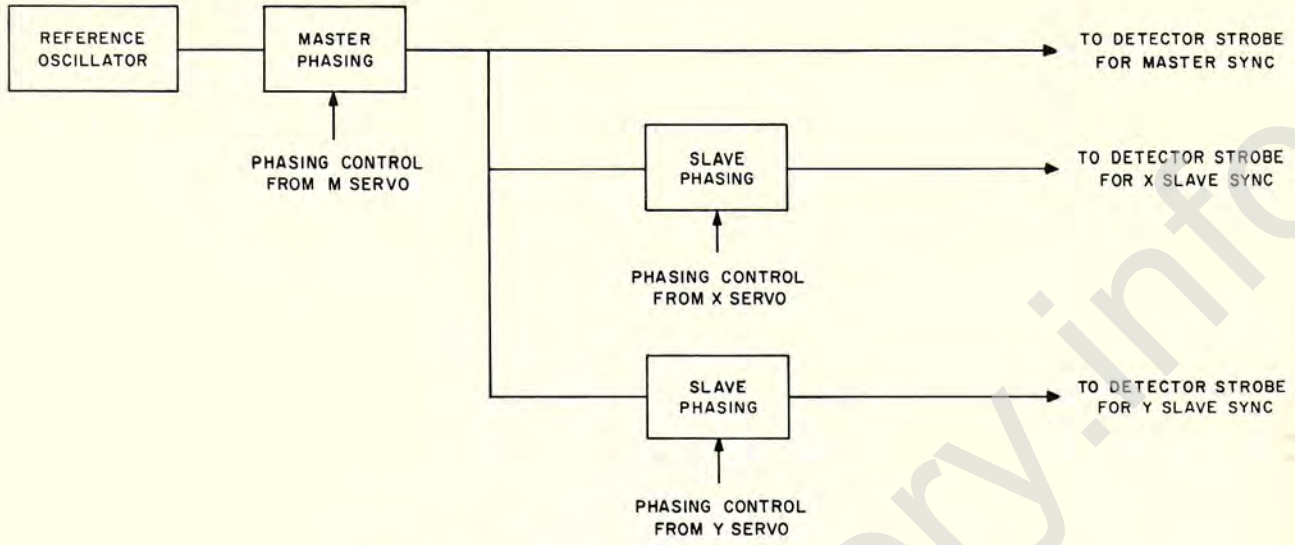


Figure 4-64. Phasing Control of Detector-Strobe Unit

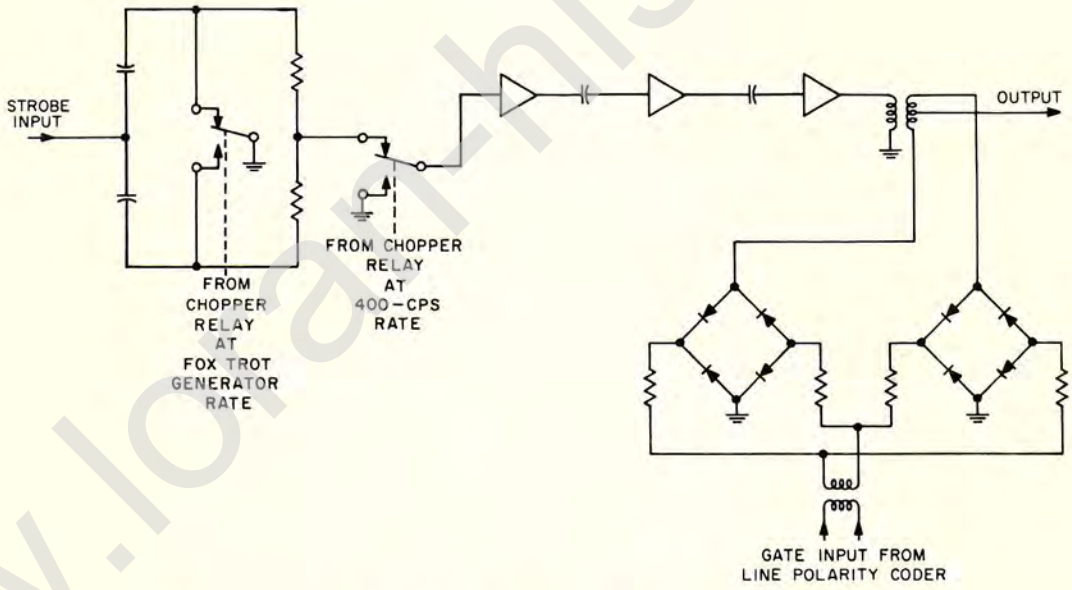


Figure 4-65. Strobe Amplifier, Simplified Schematic Diagram

the top. The resistive voltage divider again establishes the output at one-half of the total value, or -1 volt.

See figure 4-67 and assume only a d-c offset level of +10 volts. During the first interval, the ground is applied at the top and the top capacitor charges to +10 volts in the direction shown. During the next cycle, the ground is removed from the top and applied to the bottom. Now, the bottom capacitor charges to +10 volts. Because of the long time constant, the top capacitor remains charged at 10 volts in the direction shown, resulting in 0 volt at the top (charges oppose each other) and, hence, a zero output. At the third interval, the conditions will be the same as they were during the first interval. The capacitors will again both be charged to opposing +10-volt levels and the output will still be zero.

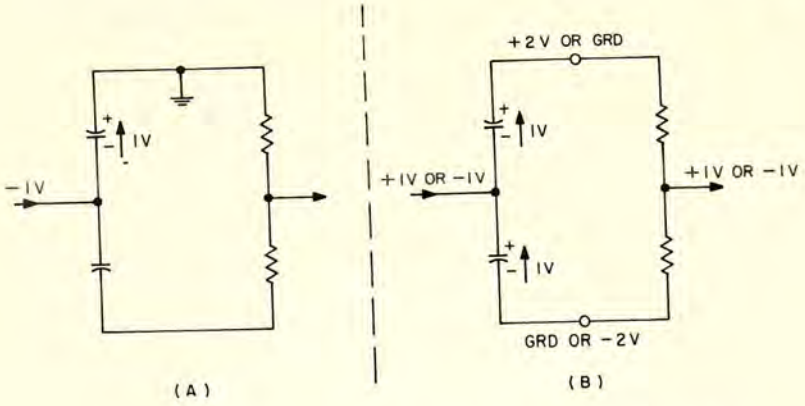


Figure 4-66. Chopper Input Circuit, A-C Chopping Action

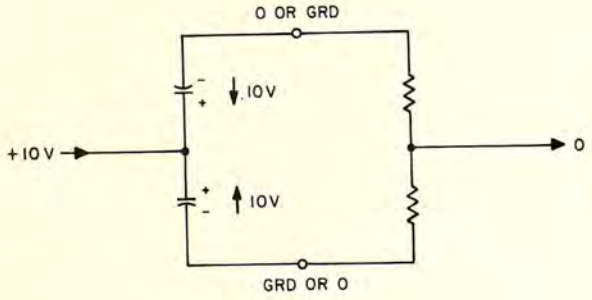


Figure 4-67. Chopper Input Circuit, D-C Chopping Action

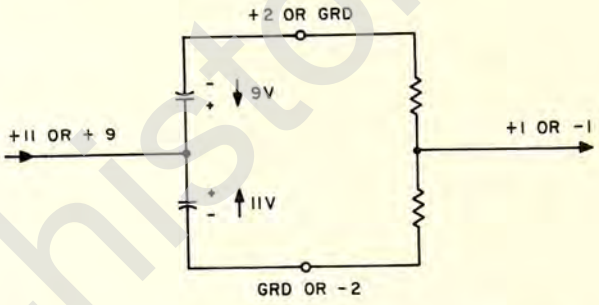


Figure 4-68. Chopper Input Circuit, Combined Chopping Action

Now, assume that the square-wave voltage and the d-c offset voltage are superimposed. In this case, the voltages will be shown as in the diagram of figure 4-68.

Assume that the ground is applied at the top and an input of +9 volts (+10 -1) is applied to the input. A 9-volt charge builds up on the capacitor in the direction shown. During the next interval, the ground is at the bottom and +11 volts (+10 +1) is applied. A charge of +11 volts builds up on the bottom capacitor in the direction shown. The first capacitor retains its charge of 9 volts and now opposes the 11 volts just applied. The voltage at the top is a positive 2 volts. The output is +1 volt after division.

During the third interval, the applied voltage is +9 volts and the ground is applied at the top. A charge of +9 volts builds up across the top capacitor in the direction shown. The +11 volts previously applied is still established across the bottom capacitor. However, with respect to ground, the voltage is in a negative direction. Again, the 9 volts and the 11 volts oppose each other, resulting in -2 volts at the bottom. The voltage divider causes the output to be a -1 volt.

The net effect of the chopper action is to leave the a-c square wave unaffected and to eliminate the d-c offset.

2. DIODE GATE SWITCHES. - The diode gate in the output of each of the three subcircuits in the strobe amplifier are actually high-speed switches used to achieve rectification. In figure 4-69 a typical transformer of the type used in the strobe amplifier is shown. Assume an input signal is applied as a sine wave of 2 volts, peak-to-peak. Assume that the transformer is perfect, all three windings are equal, and that there is no loss through the transformer. When the input signal is applied to the primary (A-B), a signal of the same amplitude will appear across each of the secondaries (C-D and D-E). The output is taken from common terminal D between the secondaries. The input signal is referenced to ground since the primary is grounded on one side (terminal B). The transformer is wound so that terminals A, C, and D will be of the same polarity at any given instant of time.

Figure 4-69 shows terminal E of the transformer connected to ground through switch S1. During the first half cycle of the input, terminal A and terminal D are both at some positive value. Since the transformer has a 1:1 transfer ratio, the signal at terminal D will be one half of a sine wave with a maximum amplitude of +1 volt. As the input crosses the reference in a negative direction, assume that S1 is

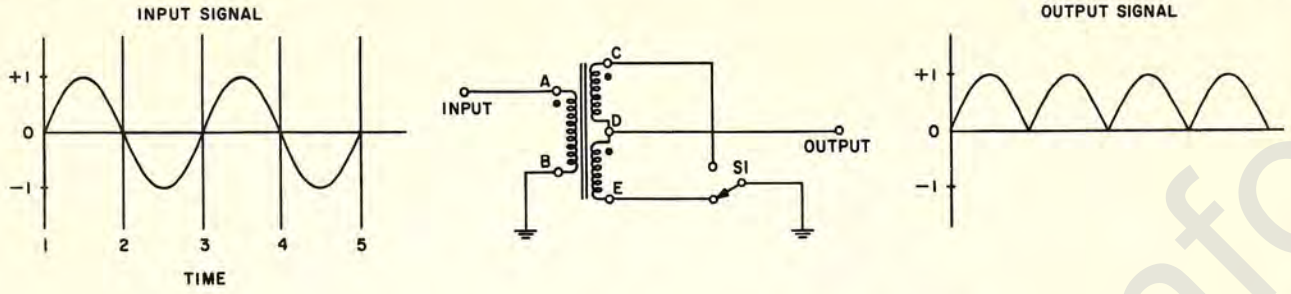


Figure 4-69. Rectification by Use of Mechanical Switching

placed in the upper position, grounding terminal C. During the second half cycle, terminal A and terminal D are out-of-phase. As the input swings on the negative side of the reference level, terminal D is swinging on the positive side of the reference level. It can be seen that if S1 is switched from terminal E to terminal C at the same rate as the applied input, the resulting output at terminal D will be a series of positive half cycles; or the resultant waveform will be full-wave rectified. Electronic switches are used in this circuit where the power and the voltages can easily be handled by diodes.

Figure 4-70 shows a simplified diagram of an electronic switch which is employed in the strobe amplifier module. Assume that the transformer in this example has a 1:10 step-up ratio. The secondary voltage between terminals C and D will be 20 volts, peak-to-peak, when 2 volts, peak-to-peak, is applied to the primary between terminals A and B. Terminal A swings positive with respect to the ground at terminal B during the first half cycle of the input signal. At the same time, terminal C is positive with respect to terminal D across the secondary. Resistors R1 and R2 are in the circuit as current-limiting components. When terminal C goes positive, diodes CR1 and CR3 and CR2 and CR4 are biased in a forward direction and present a very low impedance to the signal across the bridge. Assume that the diodes are conducting and that point E is connected to ground, as shown. Since point E and point F are essentially at the same potential in the bridge, point F must also be at ground potential. This means that during the first half cycle of the input signal, point F is essentially at ground.

Examine the circuit in figure 4-68 during the second half cycle of the input signal. Terminal A of the transformer is swinging on the negative side of the reference, and terminal C of the secondary is negative with respect to terminal D. During this time, the diodes of the bridge are reverse-biased and present a high impedance to the signal across the bridge. The bridge looks like an open circuit, or a very high impedance, at point F, even though point E is connected to ground. For a complete cycle of the input wave, the output impedance at point F will alternately be a very low impedance to ground and a very high impedance to ground. As a result, the bridge performs the same switching function as switch S1 in example A.

In the actual circuit application, the strobe input to the transformer is a 400-cps waveform of varying phase that varies between a positive voltage and ground for awhile and then between a negative voltage and ground. The fox-trot generator determines the rate of change of oscillation from positive voltage to ground to negative voltage to ground. The average voltage will be zero over a period of time, which means the output is not capable of being used later in the receiver circuit without additional rectification. Therefore, it is necessary to make the square-wave output that is supplied to later receiver circuits all of the same polarity. This is accomplished by using two diode gates as illustrated in figure 4-71. The two bridge circuits are connected across the secondary so that they are complementary. When bridge I is a short circuit to the signal applied from the secondary of transformer T2, bridge I acts as an open circuit. It has been shown that these two bridge circuits perform the same function as S1 in figure 4-69. While the input of T1 is positive, the line polarity coder signal is applied through transformer T2 to the diode gates so as to open C and ground E. When the input is negative, the line polarity coder drives the gates so that C is grounded and E is open. The result is that the output is all of the same polarity with respect to ground.

The output is not a pure sine wave because of the effects of the flipping action of the switch.

In the actual bridge circuits, only one of the two diode quads attached to each output transformer is grounded directly. The other is put at zero potential (effectively ground) by a balancing bridge, to remove any d-c unbalance inherent with the components of the bridge. The schematic diagram of the complete unit is shown in figure 6-150.

(11) GUARD STROBE AMPLIFIER (A601).

(a) GENERAL. - The guard strobe amplifier consists of two identical subcircuits, one in the cycle guard loop and the other in the envelope guard loop. Each has an input applied to it from its respective guard strobe detector. This signal is supplied to a chopper input circuit, driven at the rate of the fox-trot generator (approximately 5 cps), which removes any d-c offset from the circuit. The signal is then modulated with a 400-cps signal and coupled to a high impedance network consisting of two transistors

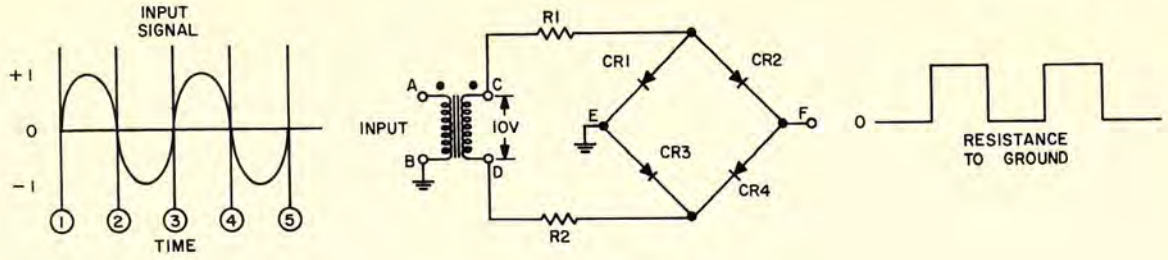


Figure 4-70. Detector Diode Switching

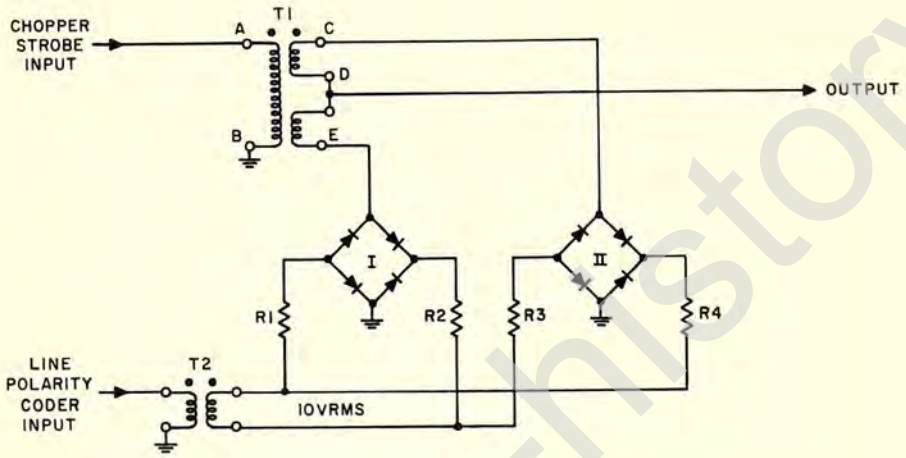


Figure 4-71. Strobe Amplifier, Diode Gate Switching Circuit

connected in complementary symmetry. This network is followed by a 3-stage amplifier that employs a-c coupling and partially bypassed emitter resistors throughout the circuit. The outputs from the cycle and the envelope subcircuits are 180° out-of-phase (this is the method of modulation used). The outputs from the two subcircuits are combined in an OR gate, which detects the most positive peak of the two at all times. The output from the circuit is applied to the skywave error threshold detector.

(b) DETAIL. - See figure 6-126 for the schematic diagram. The initial chopper input circuits are identical to the circuits used in the strobe amplifier module. A comprehensive discussion may be found by referring to paragraph 4-2*h*(10). Essentially, this input circuit passes the error intelligence signal that has been previously detected and removes any d-c offset that has built up. The original detector is driven by a reference driver at the fox-trot generator rate, causing some of the error intelligence detected to be positive and some to be negative. The chopper action in the guard strobe amplifier is also driven at the rate of the fox-trot generator. Because of the action of the input circuit, the output is an a-c signal composed only of the error intelligence information.

The 400-cps chopper modulates the output from the input circuit just described with a square wave. The 400-cps rate is much faster than the slow a-c rate determined by the fox-trot generator and allows a-c amplification. The 400-cps chopper operates by alternately sampling ground and then the signal line. This chopper drives both the envelope and the cycle subcircuits of this module at the same rate. The connectors are made so that the chopper is sampling ground in the envelope subcircuit while it is sampling signal in the cycle subcircuit. The net result is a modulation on one subcircuit which is 180° out-of-phase with the modulation on the other.

The 400-cps modulated signal is a-c coupled to a high impedance, complementary-symmetry circuit. This circuit leaves the signal undistorted and provides very effective isolation to prevent loading of the signal applied. A 3-stage amplifier then raises the output to the required level. Partially bypassed emitter resistors are used to maintain high gain and still keep the amplifiers relatively stable. The final stage has an adjustable control to allow a manual gain setting of the subcircuit to an exact level. Since both subcircuits operate identically, the levels of each subcircuit can be independently set at the required strength for proper operation of the OR circuit. This may be necessary because of unavoidable differences in component values or similar items that may affect the operational levels. The operation of the OR circuit is illustrated in figure 4-72.

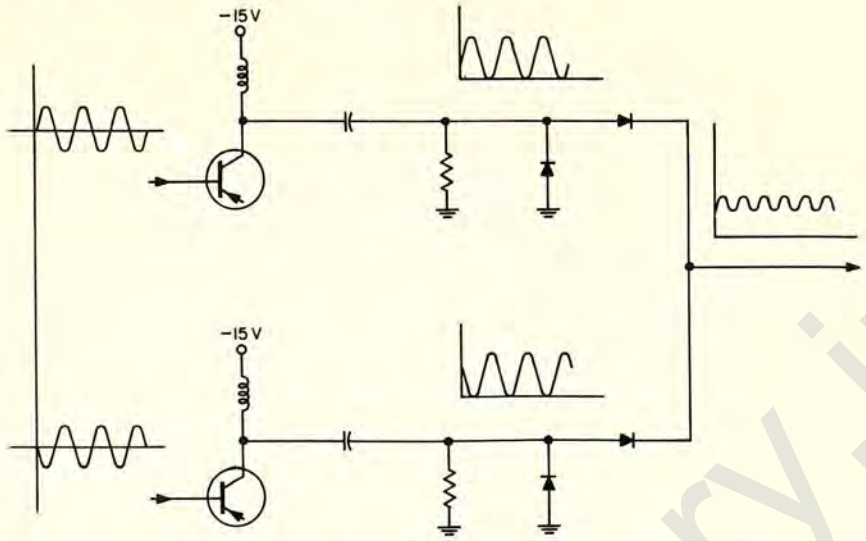


Figure 4-72. OR Gate in the Guard Strobe Amplifier

Both halves of the OR gate operate identically. The transistor dynamic response is enhanced by the load coil (swinging choke) in the collector circuit of the final transistor stage of each subcircuit. The signal is essentially a-c, 400-cps intelligence since a-c coupling is employed throughout the circuit. The capacitor and the diode connected to ground clamp the signal to ground, causing the entire waveform to be positive. The resistor connected to ground is an aid in preventing residual buildup on the capacitor. The output is taken from the final diode.

Since the two waves of each half of the OR circuit are 180° apart, one wave will be down while the other is up. The OR circuit selects the most positive of the two waveforms at all times to create a resultant d-c level output with a superimposed 400-cps fully rectified wave. This output reflects a detected error in either the cycle guard loop or the envelope guard loop. The circuit output is applied to the skywave error threshold detector.

i. AGC LOOPS. - The receiver must have an automatic gain control system which will compensate for the variations of the input levels involved since the received signals come from widely spaced transmitting sites and since the received intelligence is in the form of pulses. The gating system establishes a different agc level for each of the separate signals (M, X slave, and Y slave) so that the detection circuits of the receiver have equal signal levels applied from each of the transmitting stations. The agc gating system operates on a time-sharing basis which is related to the same time-sharing sequence of the remaining receiver circuits.

See figure 4-73 for the block diagram of the agc circuits. To simplify the discussion of these circuits, assume that the manual gain controls are all set to maximum gain. The agc loops are open, and the r-f amplifier is operating at full output. When the loops are open, the strobes are sampling a level that is in excess of the desired output level from the r-f amplifier; and the integrators build up a maximum level of agc voltage.

Next, assume that the receiver is switched to the agc position and the agc loops are closed. At this instant, the level applied to the agc bus drives the gain of the r-f amplifier to minimum, and the output of the r-f amplifier goes to a very low value. The envelope output from the detector is also at a minimum level, and the agc system begins to take control. The amplitude of the time-shared envelope output from the detector is sampled in the strobe circuits. These sampling actions are at the same rate that the incoming pulses are received. The master strobe samples the master envelope signal, the X strobe samples the X envelope signal, and the Y strobe samples the Y envelope signal. The action of the strobes is similar, therefore only the action of the master loop will be considered.

The amplitude of the master envelope signal is sampled in the strobe, amplified in the strobe amplifier, and the resulting d-c level is applied to the master integrator circuit. Large capacitors in the integrators store the average level of the integration output (which is a function of the agc level) to be applied to the r-f amplifier. Storage time is sufficient to maintain a fairly constant integrator output level over a period of several minutes. The master integrator output is applied to one of the inputs of the agc gate circuit. The agc circuit and the three associated toggles establish the gating sequence for passing the integrator outputs to the agc driver and eventually to the agc bus.

Next, the gating sequence of the master signal should be considered. The agc gate circuit allows the output of the master integrator to pass between the trailing edge of the YTS waveform and the trailing edge of the M AGC D waveform. The M AGC D waveform is a 160-microsecond pulse with its leading edge occurring 8960 microseconds after the MT

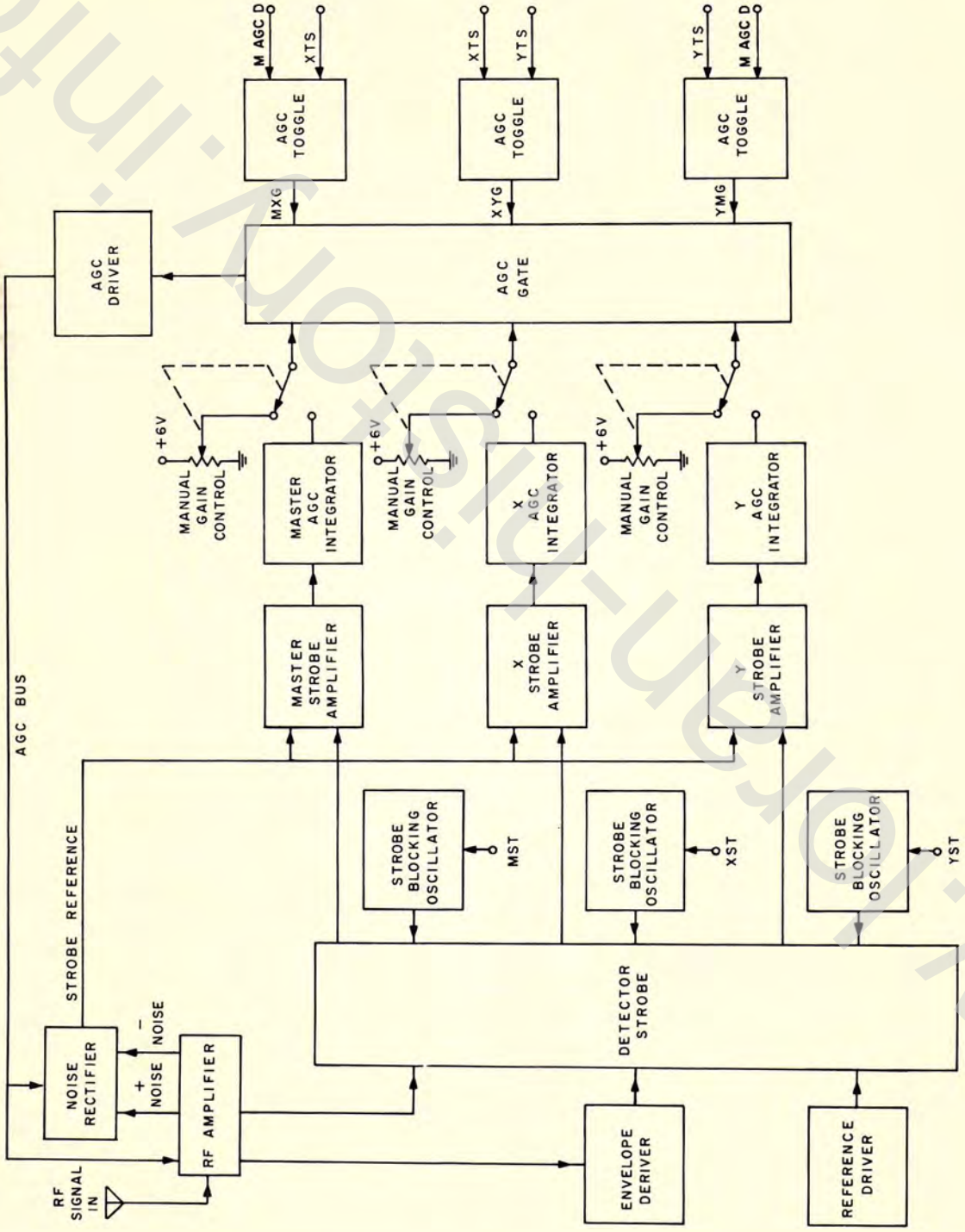


Figure 4-73. Gated AGC Control Loops, Block Diagram

signal and its trailing edge occurring 9120 microseconds after the MT signal. By this method of gating, the master agc level at the r-f amplifier is established well ahead of the master signal strength during the entire interval, which includes the ninth pulse. See figure 4-74 for the relative time sequence of the time-shared gates and the agc gates.

The time-shared output from the agc gate circuit is applied to the agc driver circuit to produce the actual agc levels to be applied to the r-f amplifier. The agc signal is also applied to the noise rectifier circuit and becomes one of the signals used to establish the strobe reference levels.

The noise rectifier circuit detects the levels of the average noise, average signal, and the average agc signals which are combined to establish the strobe reference levels. A reference is needed so that the r-f amplifier will operate at a gain condition which prevents it from becoming overloaded or saturated by the average noise level. The noise level sets the threshold of agc sensitivity so that low level signals will be amplified to the desired level even under high noise-to-signal conditions. The noise rectifier circuits form a separate control loop to prevent noise from overloading the r-f amplifier.

As the level of the incoming signals change, the agc circuits maintain a constant level of output from the r-f amplifier, thereby maintaining accuracy in the Loran-C receiver system. Even though the levels of the M, X-slave, and Y-slave signals at the receiver antenna may differ, the agc system of the receiver causes the r-f amplifier to deliver M, X-slave, and Y-slave outputs of equal level into the detector.

(1) STROBE AND STROBE BLOCKING OSCILLATOR. - For a discussion of the strobe portion of the detector-strobe and the strobe blocking oscillator, refer to paragraph 4-2*h*.

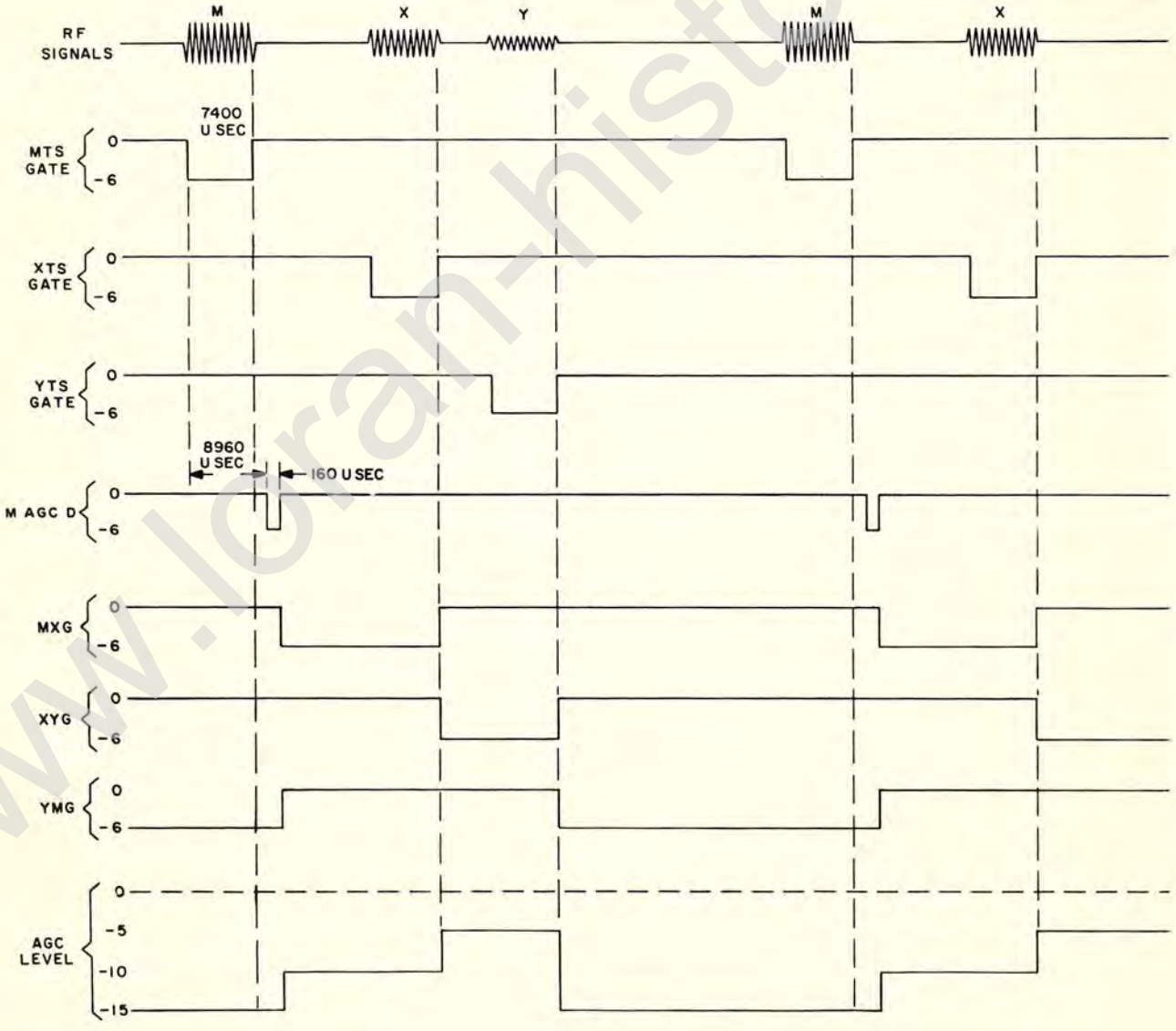


Figure 4-74. AGC Time Sequence Diagram

(2) AGC INTEGRATOR (A1507-A1509).

(a) GENERAL. - The agc integrator provides integration of the envelope strobe amplifier output. The time constant of the circuit is such that the output appears to be practically steady-state dc with respect to the normal switching and sampling times of the receiver. The output is 180° out-of-phase with the input as in ordinary amplifier design.

(b) DETAIL. - See figure 6-155 for the schematic diagram of the agc integrator circuit. The input applied to terminal 4 is coupled by R1 and R2 to the base of Q1. The signal input may vary ±5 volts when the receiver is not locked to a signal. The input level will be within the range of only a few millivolts of zero when the receiver is locked on. Capacitor C1 filters high frequency peaks of ac which may still be on the input.

NPN transistors Q1 and Q2 form a differential amplifier. Resistor R6, in the emitter circuit, biases the amplifier. Resistor R17 and the associated balance network provides a means for nulling the output when there is zero input. This compensates for the inherent tolerances in component values. Capacitors C5 and C6 provide high frequency stability. PNP silicon transistors are used in the second differential amplifier because of their high stability. Also, they couple quite readily to the NPN transistors used in the first stage.

Emitter follower output transistor isolates the successive circuits from loading the integrator. The degenerative feedback is coupled back through C3 and C4 to the base of Q1. When the input tends to go positive, the output goes negative, thereby suppressing the positive input.

As long as there is a positive voltage applied, the output will build up negatively to drive it back to the desired level. The converse is true for a negative input. Zener diodes CR2 and CR3 restrict the positive and negative voltage output to a range between +6 and -6 volts so that waiting time for proper lock-in condition is reduced. There are two outputs from this circuit. One is through diode CR2 to output terminal 10. Diode CR1 is part of the input gate to the signal overload indicator light. The second output from the circuit is directly from the emitter of Q5 to terminal 11. This output is used to supply feedback to the circuit as well as being applied directly to the agc gate and, from there, to the agc driver.

Feedback capacitors C3 and C4 are wired through connector terminals 3 and 11 for convenience of factory testing. This feedback path may be opened if an open loop test is required.

(3) AGC GATE (A1506).

(a) GENERAL. - The agc gate circuit combines three separate agc signals into a single time-shared output. The circuit consists of three identical emitter-follower stages, each preceded by a diode gating circuit. The outputs from the three emitter followers are connected to a common output line through isolation diodes. The circuit is contained on a single plug-in printed board and is located in the lower drawer of the receiver.

(b) DETAIL. - See figure 6-154 for the schematic diagram of the agc gate circuit. Since the circuit details of Q1, Q2, and Q3 are identical, only the input functions of Q1 are discussed here. Inputs applied to Q1 include the output from the master agc integrator, the YMG gate signal, and $\overline{\text{YMG}}$ gate signal from the master gate toggle. The YMG gate signal normally rests at 0 volt, but descends to -6 volts during the time from the trailing edge of the Y pulse group (YTS) to the time of the trailing edge of the M pulse group (MTS). The $\overline{\text{YMG}}$ signal rests at a level of -6 volts, but rises to 0 volt during the gate time. The input from the master integrator can vary from 0 volt to approximately -6 volts. Refer to the general discussion of the agc circuits in paragraph 4-2*i* and to figure 4-74 for the time relationships of the gate signals.

Assume that the input from the master integrator is at a level of -2 volts, the YMG level is 0 volt, and the $\overline{\text{YMG}}$ level is -6 volts. With a level of -2 volts applied at the junction of CR1 and CR2, CR1 conducts through R1 and presents a load of 10000 ohms to the master envelope integrator. However, CR2 is reverse-biased by the YMG signal and presents a high impedance to the integrator input. This causes the base of Q1 to remain at a level of 0 volt. Emitter follower Q1 conducts and causes the level at the emitter to be established at approximately 0 volt.

Next, assume that the levels of the YMG and the $\overline{\text{YMG}}$ inputs reverse. The level applied to R1 is now 0 volt and the level applied to R2 is now -6 volts. The signal of -2 volts from the master integrator is still applied. When this condition exists, CR1 is reverse-biased and CR2 conducts through R2, presenting a load of 10,000 ohms to the integrator. As CR2 conducts, the level at the input (TP1) is applied to the base of Q1. The level at the emitter of Q1 now becomes approximately -2 volts.

Observe the function of the circuits to the transistors. Signals of either zero or -6 volts are applied, alternating with their complements. The combination of R1, R2, CR1 and CR2 forms an impedance stabilizing circuit so that a constant load is presented to the integrator even though the signal from the integrator is not passed to the emitter follower.

The function of CR3, CR6, and CR9 should next be considered. The emitter levels of Q1, Q2, and Q3 will go positive, but the back bias on the diodes through resistors R3, R6, and R9 will prevent a positive voltage from reaching the output. Therefore, the desired signal level varies from 0 volt to -6 volts. At any one time, only one of the agc signals (integrator outputs) appears at the output because of the switching effect of the emitter diodes.

(4) AGC GATE TOGGLES (A1501-A1503).

(a) GENERAL. - The agc system requires a sequence of gates which will time share the master, X-slave, and Y-slave agc signals so that any one is independent of the other two. For example, should the master agc level change, it would not change the agc level applied during the receiving time of either the X or Y inputs. This time-sharing function is accomplished by the use of three toggle circuits. The

time relationships of the agc gates are shown in figure 4-74 along with the relative waveshapes involved. Refer to paragraph 4-2*d*(1) for the detailed description of the basic toggle circuits.

(b) DETAIL. - Refer to figure 4-75 for the block diagram of the gate toggles. Input functions can be thought of as starting gates (K1 inputs) and stopping gates (J1 inputs). The toggles in this application are bistable devices which require both a start and a stop function. Outputs Q and $\overline{Q}$ are complements; that is, when Q is at 0 volt, $\overline{Q}$ is at -6 volts. Also, when Q is at -6 volts, $\overline{Q}$ is at 0 volt.

The sequence of events in these circuits may be shown as follows:

1. YTS goes to zero - (stop) $\overline{XYG}$ goes to 0 volt, $\overline{XYG}$ goes to -6 volts.
   - (start) - YMG goes to -6 volts, $\overline{YMG}$ goes to 0 volt.
2. MTS goes to zero - (stop) - YMG goes to 0 volt, $\overline{YMG}$ goes to -6 volts.
   - (start) - MXG goes to -6 volts, $\overline{MXG}$ goes to 0 volts.
3. XTS goes to zero - (stop) - MXG goes to 0 volt, $\overline{MXG}$ goes to -6 volts.
   - (start) - XYG goes to -6 volts, $\overline{XYG}$ goes to 0 volt.
4. YTS goes to zero - the cycle is complete and the action in step 1 is repeated.

(5) AGC DRIVER (A1504).

(a) GENERAL. - The agc driver circuit amplifies the composite agc signals from the agc gate circuit and applies the amplified level to the agc bus and to the r-f amplifier module. The circuit consists of a differential amplifier input stage and an emitter-follower output stage. The circuit has a gain of approximately 2.5 so that the maximum input signal (-6 volts) is amplified to a level not to exceed -15 volts on the agc bus.

(b) DETAIL. - See figure 6-152 for the schematic diagram of the agc driver circuit. The input level applied at the base of Q1 is in the range from 0 volt to -6 volts. The input signal is developed across R1 and applied to the base of Q1. Transistor Q1 conducts, developing the signal in the emitter load, R3 and R4. Since Q1 and Q2 are emitter-coupled as a differential amplifier, the level at the junction of R3 and R4 is applied to the emitter of Q2 through R6. Transistor Q2 operates as a common base amplifier, the base being returned to ground. The signal applied to Q2 is amplified and appears at the collector across load resistor R5. This level is applied directly to the bases of Q3 and Q4, complementary emitter-follower, and is transferred through Q3 and Q4 to their emitters. The level at the emitters of Q3 and Q4 are coupled out of the circuit through R12.

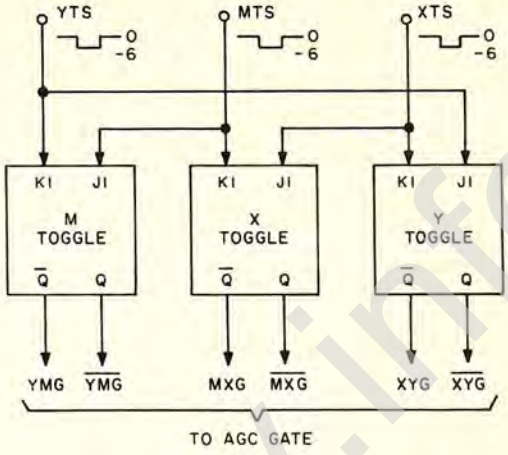


Figure 4-75. Gate Toggles, Block Diagram

(6) NOISE RECTIFIER (A1505).

(a) GENERAL. - The noise rectifier circuit produces a strobe amplifier reference level that in turn, acts on the strobe sampling output and the interference level to regulate the agc level applied to the r-f amplifier. This function is desirable so that the r-f amplifier will not become overloaded from noise peaks under high noise-to-signal conditions and the signals will be amplified to the proper level for application to the detector circuits. The total circuit involved in the noise rectifier operation is physically divided between the r-f amplifier module and the noise rectifier printed circuit board.

See figure 4-76 for the partial schematic diagram of the noise rectifier circuit showing the interconnections between the two modules. The rectifier portion of the r-f amplifier is not referenced directly to ground. The negative side of the rectifier is connected to the emitter of Q1 in the noise rectifier module and the positive side of the rectifier is connected as the input to the threshold-reference, differential amplifier, Q2-Q3.

The agc circuits operate without difficulty when the average levels of the received signals are above the average noise. However, when the average noise level exceeds the average signal level, a normal receiver tends to set the agc level with respect to the peak level (which is noise) rather than the signal level. The Loran-C receiver is required to operate with interference-to-signal conditions of approximately 100 to 1 and noise-to-signal conditions of approximately 10 to 1. The noise rectifier circuit provides a means of maintaining a good level of the amplified signal even when the noise level exceeds the signal. What is normally considered high noise levels do not saturate the receiver.

(b) DETAIL. - See figure 6-153 for the schematic diagram of the noise rectifier circuit. First, examine the function of Q1. The agc level is applied at the base of emitter follower Q1, and produces an

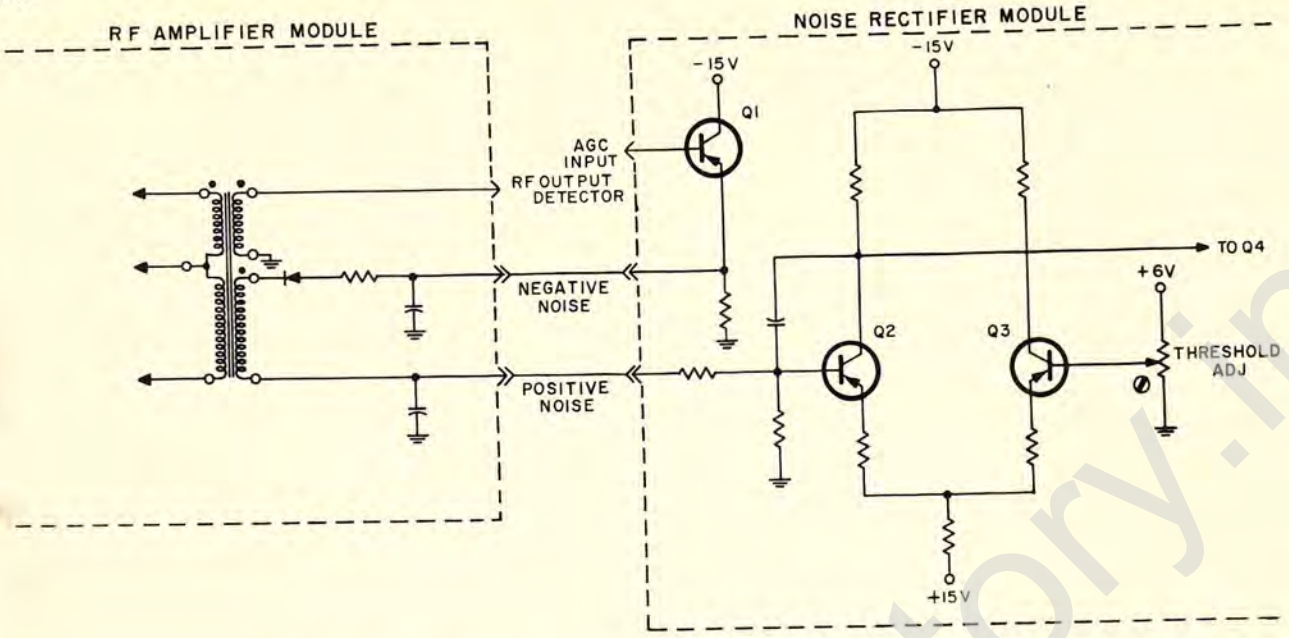


Figure 4-76. Noise Rectifier Circuit, Partial Schematic Diagram

emitter level which is approximately equal to the level applied at the base. The negative voltage at the emitter of Q1 is applied to the anode of the rectifier diode in the r-f amplifier as reverse bias. This keeps the rectifier diode cut off until the noise level exceeds the level of the signal. When this occurs, the rectifier diode in the r-f amplifier conducts and produces a small positive voltage at the base of Q2 which is applied through divider R2-R3.

Next, consider the functions of Q2 and Q3. The current through Q3 and R6 is set by threshold adjust control R9. The level at the emitter end of R6 establishes the bias applied to Q2. With no signal applied at the base of Q2, the transistor is in saturation; and the emitter, base, and collector voltages of the transistor are approximately equal. Load resistor R7 limits the current through Q2 and develops the differential signal level which is applied to Q4. When the noise level increases above the signal level, the rectified noise level exceeds the signal level; and a positive voltage is applied at the base of Q2. Capacitor C1 prevents the noise threshold level from following the levels of the peak noise and keeps the threshold level at a relatively smooth d-c value.

Emitter follower Q4 produces the strobe reference output level either through resistor R14 or resistor R13. A bus wire connection is made to R14 when the receiver is operating on 8-pulse reception. Resistor R13 is connected in when single-pulse operation is being used.

Assume a positive threshold voltage is applied at the base of Q3. When the noise level rises past the signal level, and the positive voltage at the base of Q2 exceeds the positive threshold voltage at the base of Q3, the voltage at the collector of Q2 and, hence, the base of Q4 is driven negative. The emitter of Q4 is then driven in a negative direction from its established reference output. The voltage divider formed by R10 and R11 determines the amount by which this reference can be reduced.

The output of the noise rectifier is approximately 150 millivolts when operating under 8-pulse condition. This is the approximate reference level with the output of the r-f amplifier set to 0.25 volt rms at the sample point of the signal pulse. The interference level at the output of the r-f amplifier must be at least 35 db before interference controls the operation of the agc loop.

The net result of the noise rectifier circuit may be summarized as follows. When the noise level exceeds the signal level, the agc level increases in a negative direction so that the noise will not saturate the r-f amplifier. Since the strobe circuit detects only the coincident signals from the detector, the strobe would not reflect a change in noise level. Without the noise rectifier circuit, the r-f amplifier could become saturated under high noise-to-signal conditions. Within an allowable range of noise, the noise rectifier circuits change the strobe reference level to prevent overloading the receiver from high noise conditions. The output of the r-f amplifier is limited so that it can never exceed 16 volts.

(7) AGC MONITOR (A1510).

(a) GENERAL. - The agc monitor circuit contains triggering circuitry for the Loran indicator (IP-532/SPN-30) to allow proper viewing of (1) the agc levels for the various signals and (2) the shape of the pulses during the entire pulse action, beginning at a time coinciding with the guard strobe triggers (approximately 45 microseconds ahead of the strobe triggers).

Two transistor stages are required to achieve the first purpose for all three chains of signals, M, X, and Y. This circuit modulates the agc voltage in the receiver with the output from the monostable multivibrator in the code group generator and applies the resulting output to the indicator for scope presentation. An example of a typical scope trace appears in figure 4-77. The size of each group of pulses will reflect the relative strength of the received signals. Also, the low frequency response of the indicator is avoided and the scope presentation will be a clean, internally generated signal free of the noise that is present on the signals received at the antenna.

The other six transistor stages are used to create IMT, IXT, and IYT triggers for the indicator, two stages being used for each trigger. The leading edge of the respective guard strobe trigger is used as a basis for the establishment of an indicator trigger. This means the scope triggers approximately 45 microseconds ahead of the strobe point, or approximately 15 microseconds ahead of the beginning of the trace when lock-on has been accomplished. This assures complete viewing of the pulse waveshape. In addition, the trailing edge of the applied trigger is used to obtain a view of the strobe action.

(b) DETAIL. - The circuit which allows viewing of agc consists of two emitter follower stages and a gating diode, as illustrated in figure 6-156. The agc gate signal applied to terminal 12 of the board is a time-shared signal varying between 0 and -6 volts. The output from the monostable multivibrator, which is applied to terminal 10, is a sequence of pulses between 0 and -6 volts. There is trigger for each of the pulses in the master code group, the X-slave code group, and the Y-slave code group. When the receiver is locked on, the group of pulses from the monostable multivibrator for each code group occurs at the same time the agc voltage varies to compensate for the relative strengths of the code groups received at the receiver antenna. For a very weak signal, the agc gate voltage will be near 0 volt; and for a large signal, the agc gate voltage will be very close to -6 volts.

The agc gate voltages for three code groups are assumed to be -2 volts, -0.5 volt, and -4 volts, respectively. At the start of the sequence, emitter follower Q1, an impedance-matching device, applies approximately a -2-volt level to the cathode of diode CR1. Before the first pulse from the monostable multivibrator arrives on terminal 10, the output of the monostable multivibrator is 0 volt. Hence, diode CR1 is conducting, establishing an output of 0 volt through Q2, also an emitter follower. When the first pulse for the master group does occur, the monostable multivibrator output drops to -6 volts and diode CR1 is cut off. This causes the -2-volt level from Q1 to be transferred to the output. After the pulses for the master group have finished, the agc voltage changes to accommodate itself to the -0.5-volt level for the X-slave code group. Now, when the pulsing action occurs, the pulse group will be between 0 and -0.5 volt. Similarly, the Y-slave code group pulses will be between 0 and -4 volts. The resulting output, as presented on the scope, is illustrated in figure 4-77.

The three circuits that create the indicator triggers each operate identically. These circuits are Q3 and Q4 for IMT, Q5 and Q6 for IXT, and Q7 and Q8 for IYT. Figure 4-78 is a simplified diagram of the master portion of the circuit described below. The MGST signal is a square-wave pulse varying between levels of 0 and -6 volts. The level is normally 0 volt and goes to -6 volts when a pulse occurs. The IMT output is a square-wave pulse that varies between -6 volts (while MGST is 0 volt) and +6 volts (while

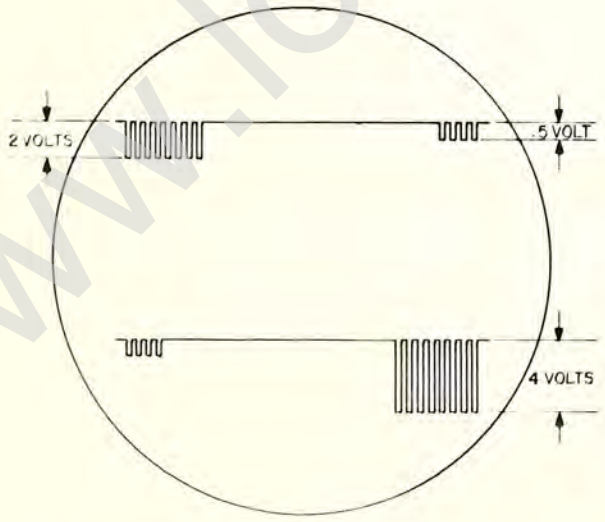


Figure 4-77. AGC Monitor Output, Sample Scope Display

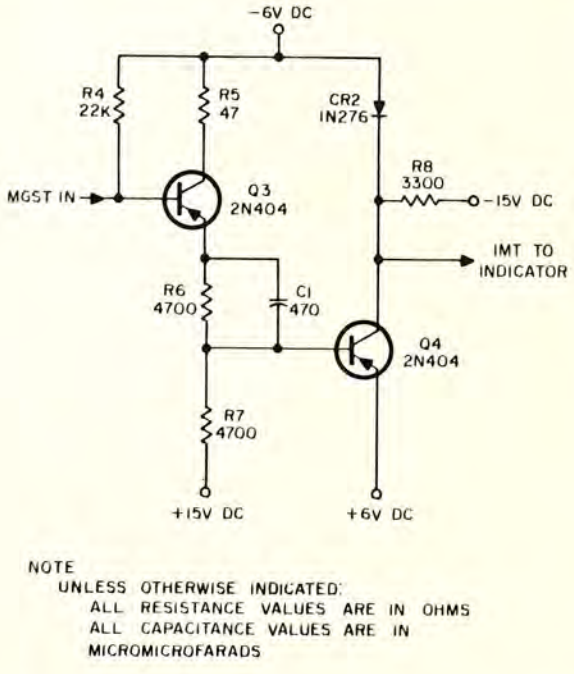


Figure 4-78. AGC Monitor IMT Circuit, Simplified Schematic Diagram

MGST is -6 volts). Transistors Q3 and Q4, voltage divider R6 and R7, capacitor C1, and diode clamp CR2-R8 are used to accomplish this action.

When MGST is 0 volt, transistor Q3 conducts and an approximate 0-volt level is applied to the emitter of Q3, the top of one end of a voltage divider, R6 and R7. These resistors are of equal value; therefore, a +7.5-volt level is applied to the base of PNP transistor Q4. Since the emitter of Q4 is established at +6 volts, the transistor will be cut off. Diode CR2 and biasing resistor R8 establish an output of -6 volts, which is applied to the circuit output at terminal 8.

When the guard strobe trigger goes to -6 volts, the emitter of Q3 also follows it to -6 volts. The voltage divider is now between -6 volts and +15 volts, establishing the midpoint at approximately +4.5 volts. The +6 volts on the emitter of Q4 is now sufficient to cause it to conduct, raising the collector to a +6-volt level. The circuit output now reverse biases diode CR2 and +6 volts is supplied to terminal 8.

Capacitor C1 is used to accelerate the switching action in order to steepen the sides of the square-wave output.

j. CYCLE SERVOLOOPS.

(1) GENERAL. - The Loran-C receiver must lock the phase of the locally generated 100-kc signals to the received signals to maintain the high degree of accuracy necessary. This is accomplished by coherently detecting the received signals with the locally generated signals. The output of the coherent detector is strobed, amplified, and applied to the servoloops to maintain a constant phase lock as long as the receiver is tracking one group of transmitting stations.

Refer to figure 4-79 for a block diagram of the master, X, and Y cycle servo-signal paths. First, the 100-kc local oscillator signal must be phase-locked with the received master signal to establish a reference for the X and Y 100-kc signals in the receiver. Phase lock using a coherent detector can best be accomplished when the reference signal and the received signal are 90° apart (when the output of the detector is zero). The local 2-phase, 100-kc oscillator signal is applied to the master cycle resolver to produce the master 100-kc signal. This master 100-kc signal is applied to the detector-strobe along with the received master signal. The detected master signal is then strobed and applied to the master cycle strobe amplifier where it is determined if phase lock exists. The output of the master cycle strobe amplifier is applied to the master integrator, which produces the error signal that is applied to the master cycle servoamplifier. The servoamplifier drives the master cycle servomotor, which, in turn, drives the master cycle resolver, shifting the master 100-kc signal until phase lock occurs between the received master signal and the locally generated 100 kc. When this phase lock occurs, the loop is balanced and there will be no error voltage generated. Ordinarily there will be a slight frequency difference between the locally generated 100-kc and the received 100-kc signals. Consequently, the master cycle servo must constantly make correction to maintain phase lock at the detector.

Consider next the X and Y cycle servoloops. Once the master 100-kc signal is phase-locked, it is used as a reference frequency for the X and Y loops. The output of the master cycle resolver is applied to a quadrature network in the 100-kc driver module to produce excitation voltages for the X and Y cycle resolvers. The 100-kc outputs of the X and Y cycle resolvers, properly coded, are applied to the detector-strobe at the same time as the received X and Y signals. Since the detector is a time-shared device, only one 100-kc signal is applied to the detector at one time. The detector cycle output of information is applied to all three of the cycle strobes, in the proper time sequence. The strobes sample the output of the detector to determine if phase lock exists between the received X and Y signals and the locally generated X and Y 100-kc references. If there is a phase error between the local and received signals, the strobe applies an output to the X and Y strobe amplifier. The strobe amplifiers amplify and demodulate the error signals and supply them in d-c form to the appropriate integrators and alarm circuitry. The error signals from the X and Y integrators are fed back to the X and Y servoamplifiers that drive the X and Y cycle servomotors. These servomotors rotate the X and Y resolvers, which shift the phase of the local X and Y 100-kc reference signals until phase lock is established and the loops are balanced. Because of the time-shared feature, the X and Y loops are entirely independent of one another.

Because the phase relationship of the received and local signals is so important to the accurate operation of the Loran-C system, a method of reducing possible mechanical error caused by friction and mechanical sticking is incorporated in the servoloops. The dither oscillator is employed to accomplish this. Each of the servoamplifier input amplitudes is related to the mechanical power applied to the corresponding cycle resolver. Consequently, as the servo error approaches zero, the torque applied to the resolvers also approaches zero. The motor sticks when the torque reaches a certain value. The dither signal is just of sufficient amplitude to overcome this sticking and friction (called "stiction") and enables the servomotor to turn the resolver until the error reaches zero. A dither frequency of 10 cps is used in sufficient amount to overcome the mechanical stiction without causing excessive fluctuation of the readout dials.

(2) UNIT DESCRIPTIONS. - The block diagram of the cycle servoloops illustrates many units that have been discussed in other paragraphs in the book. The following is a list of cross references of the units with the paragraph location where the detail descriptions are found.

unit	paragraph
Detector-Strobe	4-2*h*
Code Group Generator	4-2*g*
Servo Motor	4-2*p*
100-kc Driver	4-2*c*(3)
Resolver	4-2*c*(4)

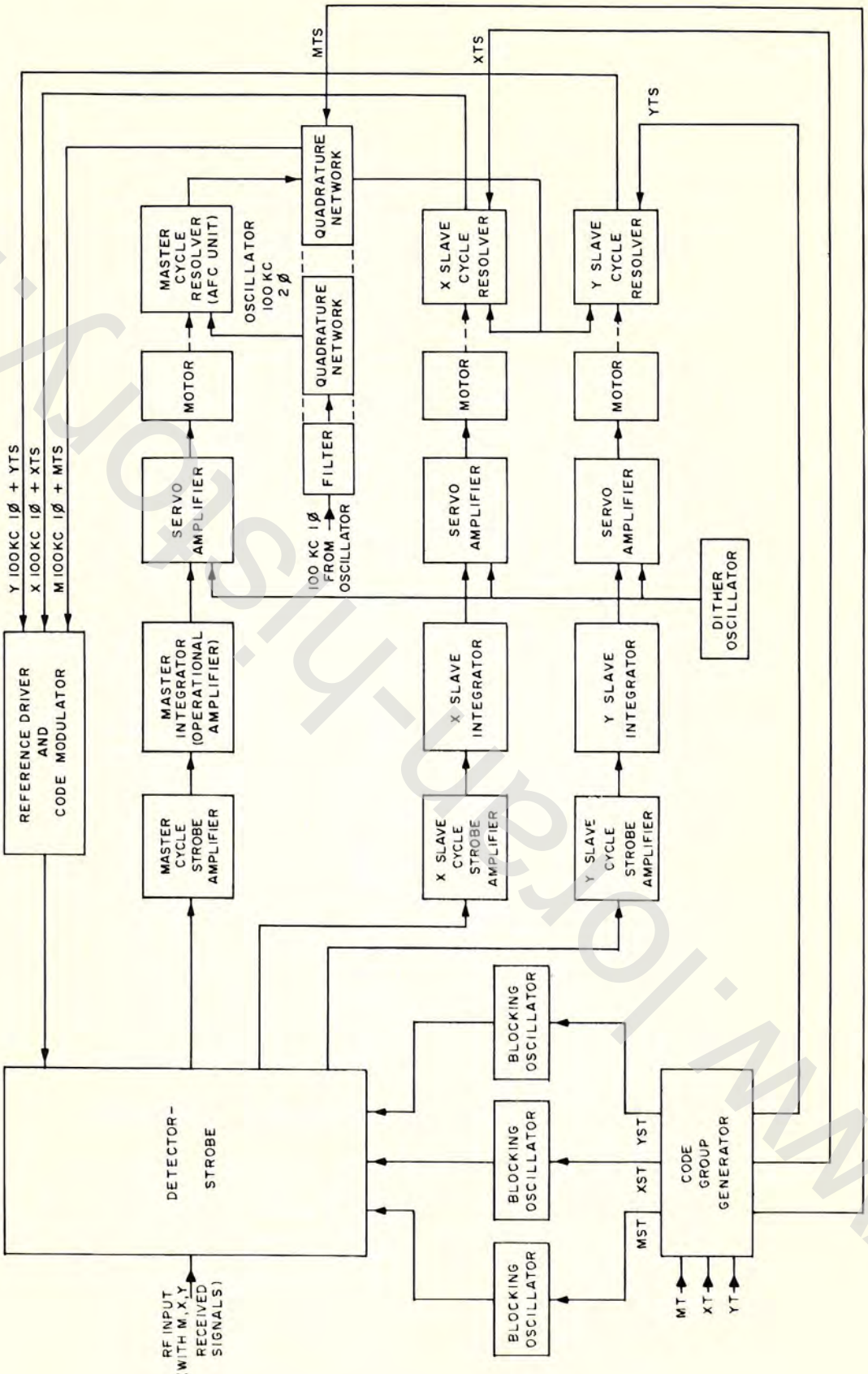


Figure 4-79. Cycle Servo Loop, Block Diagram

The strobe blocking oscillator and the strobe circuit discussions appear in paragraph 4-2*h*. In the cycle loop application, the cycle strobes sample an error voltage from the time-shared detector which will vary plus and minus from a level of 0 volt. Separate strobes are used to sample the master, X, and Y outputs from the detector. The inputs to the strobes will be 0 volt when phase lock is established in the system. The strobe outputs will vary from a zero level to produce error output levels in the order of a few millivolts. This small error signal must be amplified by the operational amplifiers (integrators) for ultimate application to the servo-amplifiers.

(3) OPERATIONAL AMPLIFIERS AND CYCLE TIME CONSTANT.

(a) GENERAL. - The operational amplifier module receives an input error signal from a cycle error amplifier, integrates the signal, and applies it to the master cycle or slave-delay servo. The three operational anplifiers are connected with the cycle time constant module, which provides a proper time constant for integration. See figure 4-80 for the diagram of this interconnection. This time constant is switched to a lower value when the error is a large value so that the servo-system may more rapidly reduce the error.

(b) OPERATIONAL AMPLIFIER (1451-A1453). - See the schematic diagram, figure 6-151. The input circuit of the operational amplifier consists of a resistive network. The input to terminal 1 is supplied from the cycle error amplifier for the respective loop and the other inputs are fed from the cycle time constant circuit. The inputs are all combined at chopper G1, which is driven at 400 cps. The chopper action creates a 400-cps signal modulated by the applied error signal. This combined signal is then amplified by the a-c amplifier.

The signal from the input resistive network is applied to the first stage of the amplifier. Capacitor C21 helps eliminate noise created by the chopping action. The first stage of amplification is provided by transistors Q1 and Q2, a modified Darlington pair. With respect to dc, this circuit has a fairly low input impedance and, therefore, is quite stable. But the circuit has a high a-c impedance because of the incorporation of a-c feedback through capacitor C3. The signal is then fed successively through four stages of amplification, Q3 through Q6. These stages employ decoupling resistors and capacitors in both their collector and emitter circuits. Degeneration is provided by the unbypassed emitter resistors. The last stage, Q6, is transformer coupled to the output. This increases the dynamic range capabilities of the circuit. The primary of T1 is tuned to 400 cps by capacitor C17 to minimize the possible effects of harmonics in the signal.

The output is synchronously demodulated with the input by use of the same 400-cps chopper. There are two outputs, one direct to terminal 11 of P1, and one filtered by R27 and C19 to terminal 22 of P1. The unfiltered output is used to supply feedback control to the cycle time constant circuit. The filtered output is applied to the master cycle servo or a slave-delay servo. The d-c gain capability is 60 db from terminal 1 to terminal 22.

(c) CYCLE TIME CONSTANT (A2501). - See the schematic diagram, figure 6-168. There are three separate circuits in the cycle time constant module, one of which works in conjunction with each operational amplifier. The servoloops in the receiver are driven by error signals that appear when the internally generated signals and the transmitted signals are not precisely coincident. Error will appear, for instance, when the conveyance in which the receiver is located accelerates or decelerates. Rapid changes of location, such as when a ship is turning, increase the danger of losing lock. This is because error is developed only under acceleration and not under a constant velocity in a type 2 servosystem. When error (discrepancy between the r-f and internal signals) exceeds 2-microseconds in cycle or 20-microseconds in envelope, a shorter time constant is inserted into the loop so as to speed up the servosystem to recapture the signal. A relay energizes in the cycle time constant module to connect this speed-up circuit.

The speed requirements of the master loop are less than those for the slave loop. This is because the master signal is its own reference and is not as greatly affected by changes in velocity as are the slaves. Therefore, no speed-up circuit is inserted in the master portion of the cycle time constant module by only a capacitance that is one half of the capacitance in the slave loops.

Since the slave loops are operationally identical, only the cycle time constant portion of the circuit that is in the X-slave loop is discussed. See figure 4-80. Ordinarily, when the error is changing at a rate slow enough for the X-slave delay servo to follow, the input from the X-slave cycle error amplifier is applied at terminal 1 of the operational amplifier unit. The feedback under this operating condition is passed through a capacitive network and returned to terminal 16 of the operational amplifier. When the error is sufficiently large enough to trigger the X-slave derived envelope-cycle error threshold detector, a relay internal to the cycle time constant circuit changes both the input resistance and the feedback resistance. The input is now through one set of relay contacts to terminal 15 of the operational amplifier (in addition to terminal 1). The feedback path is through the other contacts of the relay to terminal 13 of the operational amplifier (in addition to terminal 16). This action reduces the overall time constant of the servoloop.

(4) MAGNETIC AMPLIFIER.

(a) GENERAL. - In the cycle loop, the magnetic amplifier is placed between the operational amplifier and the servomotor. This amplifier is a sealed unit and generally cannot be repaired in the field. The amplifier requires a d-c input voltage and 400-cps primary power to produce the driving power for the servomotor. The servomotors are 2-phase, 115-volt a-c motors. Their direction of rotation is dependent on the relative output phase of the servoamplifiers. A negative d-c input to a servoamplifier will produce an output phase which will drive its motor in one direction while a positive d-c input will produce an output phase which drives the motor in the opposite direction. See the schematic diagrams

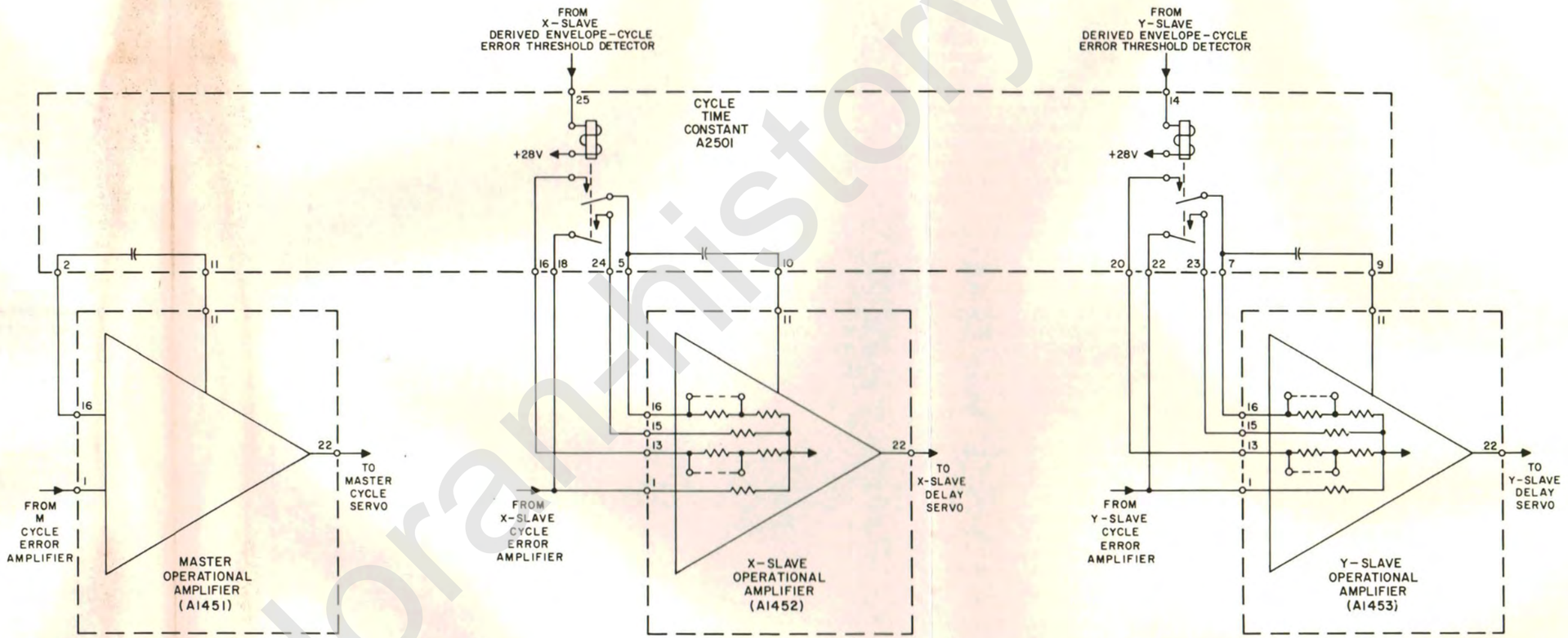


Figure 4-80. Operational Amplifiers-Cycle Time Constant, Simplified Functional Block Diagram

of figures 6-161 and 6-163 of the master and slave cycle magnetic amplifier connections.

(b) DETAIL. - The magnetic amplifier is illustrated in the simplified diagram of figure 6-174. Notice that there are two separate sections to the circuit, the d-c preamplifier and the servoamplifier.

The preamplifier portion has three inputs. Two of the inputs are to the two control windings. The other input is the 115-volt, 400-cps power directly from the power transformer. The two sets of inputs and the output are all isolated from one another. The d-c output voltage of the preamplifier is dependent only on the d-c current flowing in the control windings. Essentially, the preamplifier is a current-to-voltage device. That is, a 1-microampere current change in one control winding will cause a change of .05 volt at the output. In other words, the circuit exhibits a transresistance of 50000 ohms. The maximum output for the preamplifier is approximately 17 volts with a linear response up to approximately 7.5 volts. For the applied 400-cps supply voltage, the output will be made up of 800-cps spikes as shown in figure 4-81.

The two control windings for the preamplifier stage make it possible to employ negative feedback in its operation. In the slave cycle loop application, a portion of the output voltage is returned to one of the control windings through a large resistance to oppose the input signal from the strobe-amplifiers.

The output from the preamplifier is applied to the servoamplifier stage through a resistance in one of the control windings. Since the servoamplifier frequency response is limited to approximately 10 cps, the servoamplifier reacts to only the d-c components of the preamplifier output. The other control winding supplies dither excitation at 10 cps so that even when the first input is very minute, there will still be an input to the motor.

As shown by the waveforms in figure 4-82, the two phase outputs from the servoamplifier are not smooth sine waves. The two output signals will be approximately equal with respect to ground when the input to the servoamplifier is very small. There will be a small a-c null voltage across the two terminals. When the servoamplifier is operating near one-half of its output, the waveforms are as shown in example B. The output voltage between terminals 13 and 14 is more than 150 volts when the servoamplifier is operating at full output. The resistor-capacitor combination across the output adjusts the 2-phase output applied to the servomotor to obtain maximum motor speed.

Terminals 15, 16, and 17 are provided for adjusting the d-c offset of the preamplifier output. In the envelope loops, a potentiometer between terminals 15 and 16, with the wiper arm connected to terminal 17, is used in the envelope loops to adjust motor speed to zero when the preamplifier input is grounded. No adjustments are provided for the magnetic amplifier in the cycle loop application.

In the three derived envelope loop applications, operational amplifiers are not present and a capacitor is inserted in the negative feedback arrangement so that the circuits respond as low-pass amplifiers. See figures 6-162 and 6-163 for the connection of the magnetic amplifiers in these loops.

(5) DITHER OSCILLATOR (A2002, A2003).

(a) GENERAL. - The dither oscillator supplies dither excitation to the servoamplifier input to overcome the stiction of the servo gear trains. Figure 4-83 shows the relationship of error amplitude (motor input) to torque applied to the resolver rotor. As the error voltage approaches zero, the torque of the servomotor also approaches zero. There is a point at which the stiction of the gear train overcomes the effect of a small error voltage applied to the servomotor, and the motor will stall.

(b) DETAIL. - See figure 6-164 for the schematic diagram of the dither oscillator. To understand the phase relationships around the oscillator circuit, remember that at low frequencies, a common base amplifier has no phase shift between emitter and collector and an emitter follower has no phase shift between base and emitter.

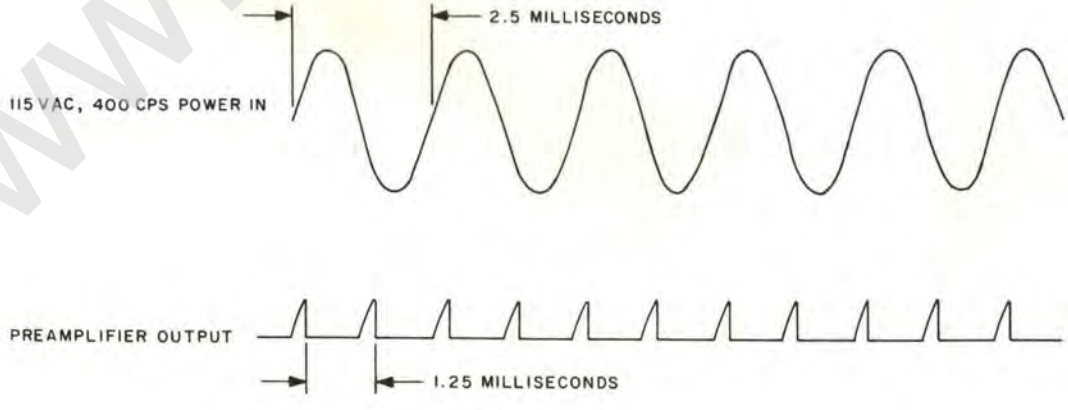


Figure 4-81. Preamplifier Output, Waveshapes

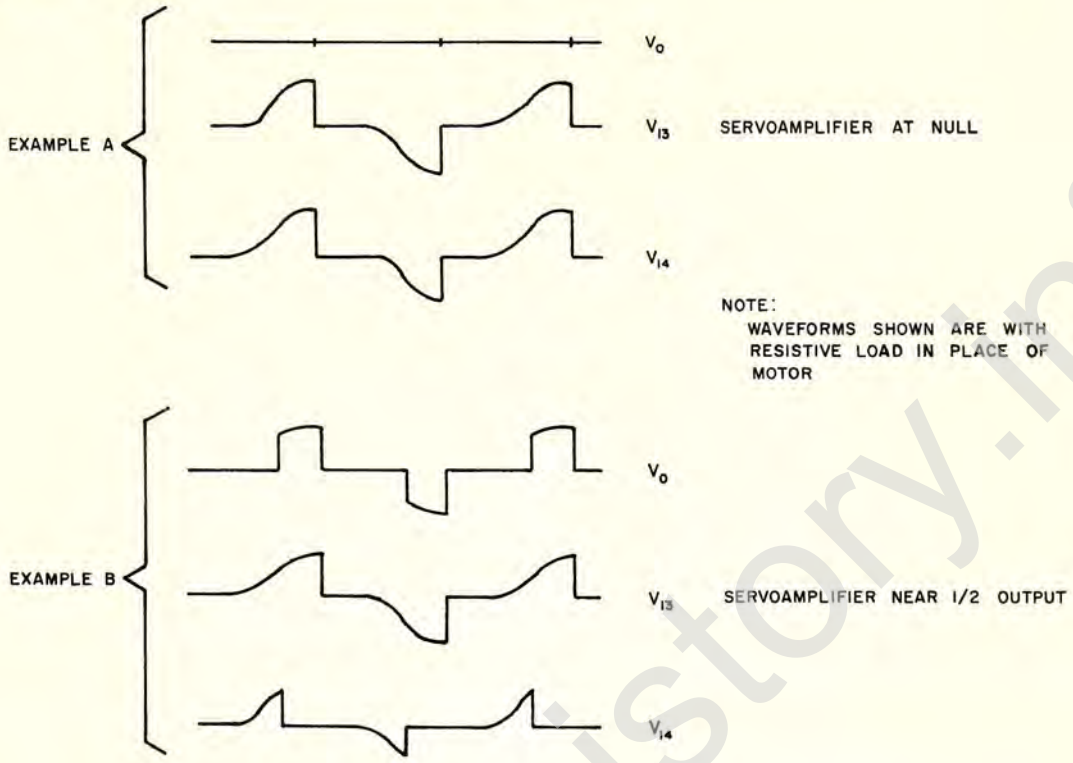


Figure 4-82. Servoamplifier Output, Waveshapes

The dither oscillator circuit consists of two basic units, the oscillator (Q1 and Q2) and the output amplifier (Q3). First, examine the functions of Q1 and Q2, the loop for the originating signal. The signal is developed at the collector of Q1, applied to the base of Q2, and then developed with no phase shift in the emitter load of Q2. The signal is then applied to the emitter of Q1. Finally, the signal is amplified in Q1 and developed at the collector with no phase shift. The signal completes the loop as regenerative feedback, thereby sustaining oscillation. The frequency of oscillation is determined by the resistor-capacitor combinations in the collector of Q1 and the feedback path between Q2 and Q1. A leading phase shift of +45° results when the impedances of R2 and R3 are equal to the impedance of C2. A lagging phase shift of -45° results when the impedance of R1 is equal to the impedance of C1. The frequency at which these phase shift characteristics occur determines the oscillation frequency. Over a complete cycle, the leading phase shift and the lagging phase shift cancel with a resultant net phase shift of zero.

Stabilizing adjustment R2 is a manual control used to compensate for aging of the capacitors or for variations in transistor characteristics. The amplitude of oscillation may also be varied by adjusting R2. The circuit will not oscillate when set at one extreme. When set at the other extreme, the oscillations will be of such amplitude that clipping and distortion will occur.

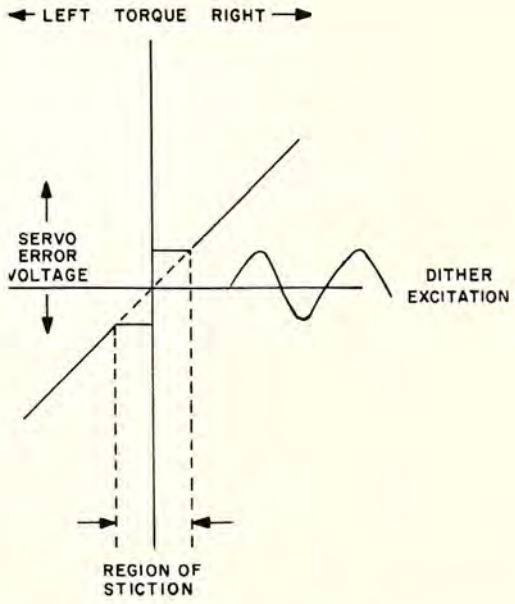


Figure 4-83. Dither Oscillator Torque versus Error Voltage

The output stage, Q3, is a simple amplifier and is used for isolation and impedance matching. The output of the circuit is coupled to the inputs of the servoamplifiers through C3, C4, and C5, respectively.

k. MASTER, X, and Y DERIVED ENVELOPE LOOPS. - See Figure 4-84 for the operational block diagram of the master, X, and Y envelope loops. The phase of the master 100-kc reference signal is established by the master cycle servoloop and is used as a phase reference in the three envelope servoloops. The single-phase output of the master cycle resolver is applied to a quadrature network that produces 2-phase excitation for the master envelope resolver and the X and Y cycle resolver. The single-phase output of the master envelope resolver is applied to the pulse rate generator section of the receiver that produces a 10-kc sine wave by counting down the 100-kc. This sine wave is applied to the 10-kc resolver driver module that produces a single-phase master 10-kc signal and a 2-phase output to drive the X and Y envelope resolvers. The master 10-kc output and the single-phase X and Y 10-kc resolver outputs are applied, through squaring amplifiers, to the code group generator section of the receiver.

The code group generator produces gates related in time to the received signals from the master, X-slave, and Y-slave transmitters. The phase code output from the code-group generator is applied to the reference driver and keys the local 100-kc signals so that the received pulse envelope can be detected in the proper phase in the cycle and envelope detectors. The r-f output is also applied to the envelope deriver. In the envelope deriver, the r-f input is delayed 5 microseconds, amplified, and added to the original signal to create the derived envelope waveshape, which is applied to the derived envelope detector. As with the envelope and cycle detectors, the reference driver also keys the derived envelope detector in the proper time sequence.

The derived envelope strobes sample the derived envelope waveshape to establish the delay error between the received pulse envelope and the generated strobe triggers. This error in envelope delay is applied to magnetic amplifiers, which, in turn, excite the servoamplifiers. If envelope error exists, the master, X, and Y servos reposition their respective resolvers to reduce the detected envelope error to zero.

The descriptions for the various units within the derived envelope loops and their paragraph references are listed below.

Name	Paragraph
Detector-Strobe	4-2*h*
Code Group Generator	4-2*g*
Strobe Blocking Oscillator	4-2*h* (3)
Strobe Amplifier	4-2*h* (10)
Magnetic Amplifier	4-2*j* (4)
Dither Oscillator	4 2*j* (5)
Servoamplifier	4-2*j* (4)
Servomotor	4-2*c*
Resolvers	4-2*c* (2)
Squaring Amplifier	4-2*p* (5)
Pulse Rate Generator	4-2*e*
100-kc Filter	4-2*d* (5)
10-kc Resolver Driver	4-2*d* (6)

l. GUARD SIGNAL PATH. - The purpose of the guard circuits is to detect the presence of skywave contamination at the receiver and cause an alarm light to be actuated. Because of the difference in transit time of ground waves and skywaves from transmitter to receiver, it is possible for the receiver to produce an error in the delay readout if the receiver locks in on a skywave signal. The receiver must sample only the ground waves from the shore transmitters to maintain the accuracy of the system.

See figure 4-85 for the time relationships of ground waves to skywaves and the guard strobe and signal strobe timing. In the example, it is assumed that there is no skywave from the master transmitting station or from the Y-slave station. However, the illustration shows that a skywave is present from the X-slave transmitter. The waveform on line A shows the proper time relationship between the ground wave signals from the three shore stations. Line B shows the presence of the X skywave with relation to the other two signals. Line C shows the combined time relationship of the detected envelope signals and the strobe sampling triggers.

Notice that the guard strobe trigger (for example, MGST) occurs before the signal strobe trigger (for example, MST). In the case of the master and Y-slave signals, there is no envelope signal present to the left of the ground wave envelope signal. However, if the receiver locks in on the X skywave, the X guard strobe trigger (XGST) occurs during the time that the X envelope signal is present. Consequently, the guard circuits in this example would detect the presence of skywave contamination.

See figure 4-86 for the block diagram of the guard signal path. The detected cycle signal and the detected envelope signal from the detector portions of the detector-strobe unit are applied to the cycle guard strobe and the envelope guard strobe. The signal from the guard strobe oscillator is used to gate the passive strobe circuits to allow any detected signal to pass through to the guard strobe amplifier. The guard strobe blocking oscillator receives its input from the station selector switch. The signals from the cycle loop and from the envelope loop are amplified separately in the guard strobe amplifier and applied to an OR circuit. The resulting signal is then applied through the station selector switch to the skywave threshold detector, which lights the SKYWAVE light when a signal of sufficient strength is applied.

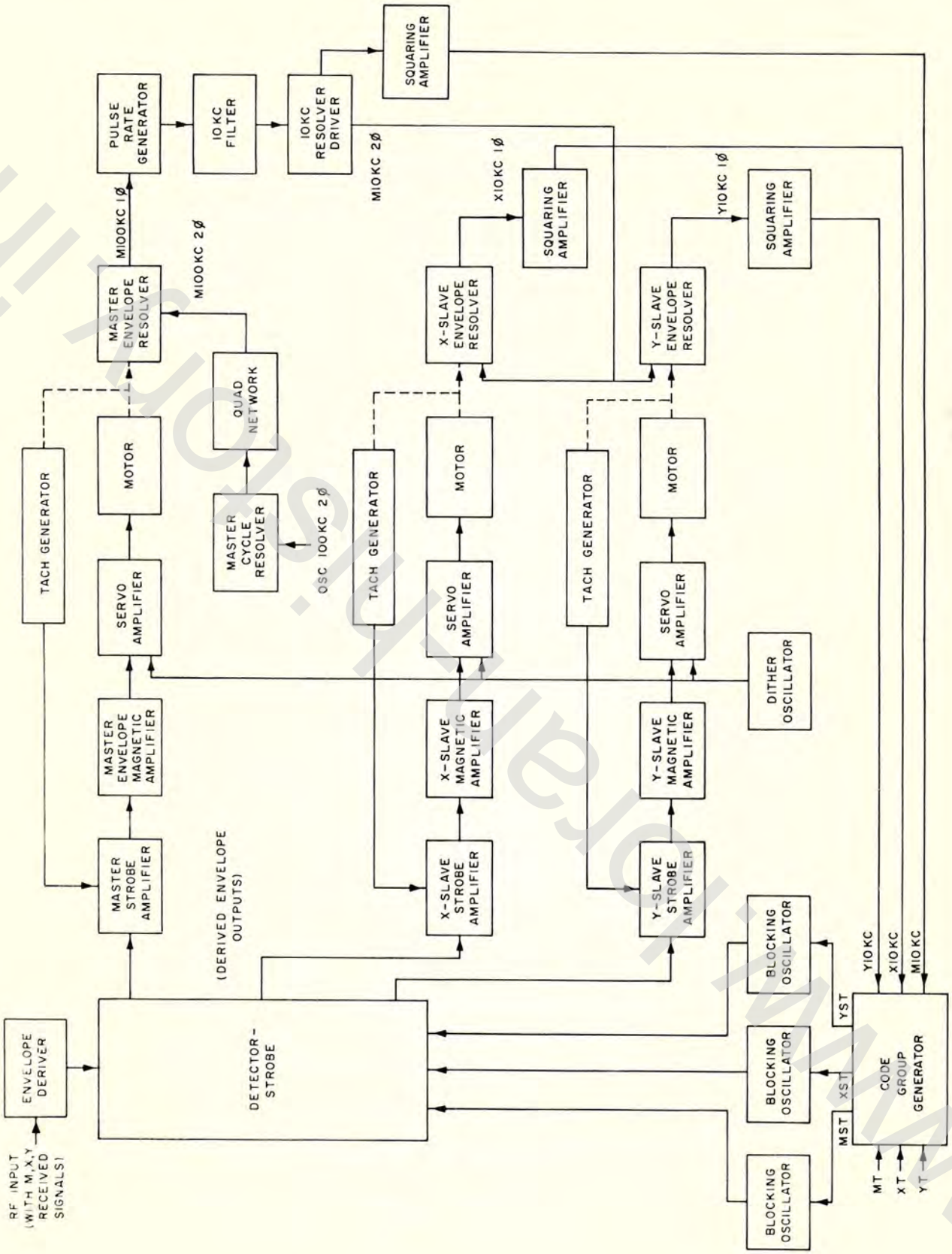


Figure 4-84. Envelope Loops, Block Diagram

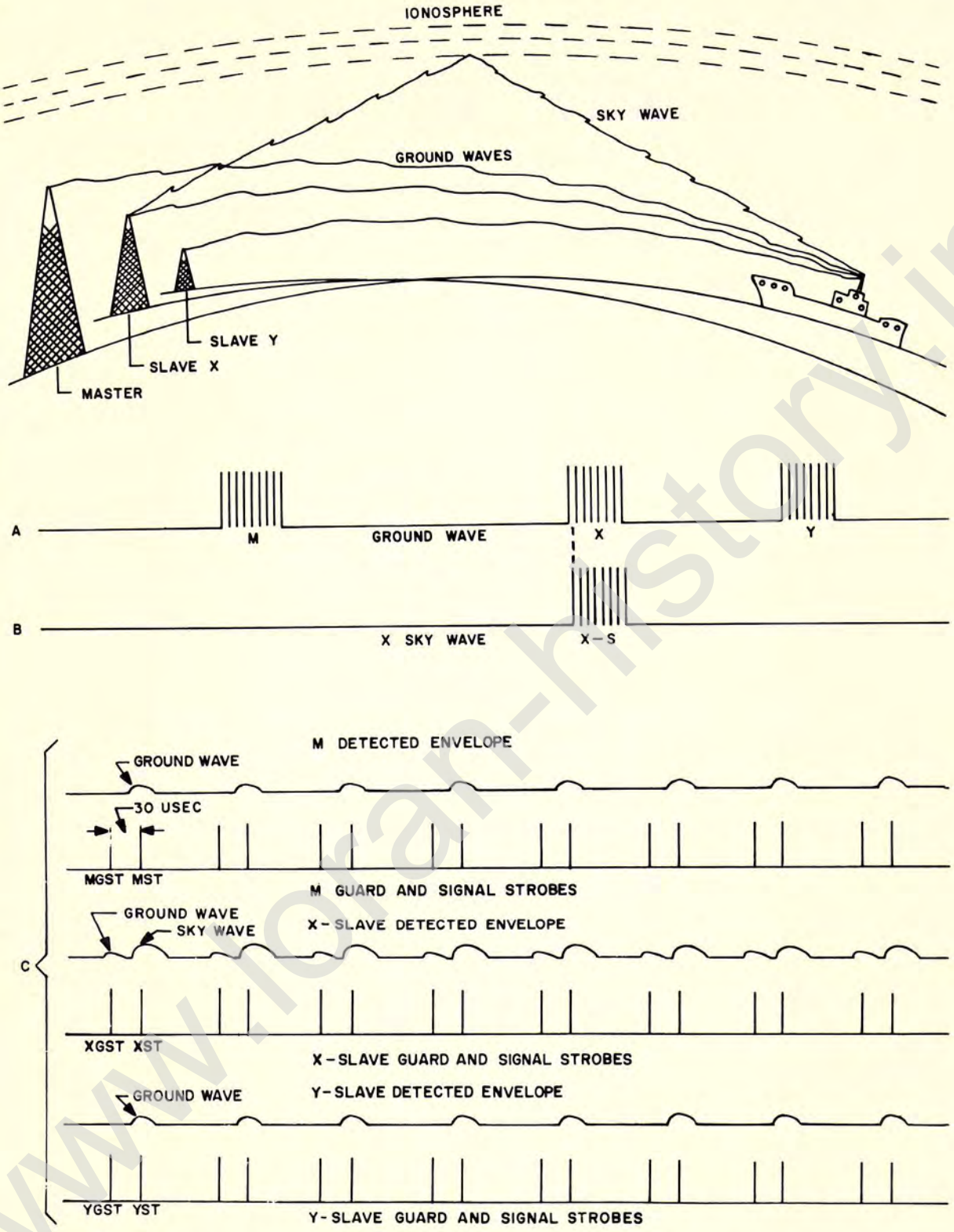


Figure 4-85. Skywaves, Ground Waves, and Strobe Time Realtionships

During normal operation, the guard strobe triggers are applied to the guard circuit in a time-shared sequence. That is, the MGST signal is applied 16 times, the XGST signal is applied 16 times, and the YGST signal is applied 16 times for a complete cycle of the sequence. When using this mode of operation, each of the signals are sampled, in sequence, and the operator has no way of knowing which signal is contaminated when the SKYWAVE indicator lamp lights. The operator must then switch the strobe trigger input to one of the single sources (M, X, or Y) that continuously strobes only one signal. By switching the strobe trigger mode, the operator can determine which one of the signals is contaminated by the presence of a skywave.

(1) GUARD AMPLIFIER, GUARD STROBES, AND BLOCKING OSCILLATORS. - As indicated by figure 4-86, guard signal path block diagram, the input applied to the guard strobe amplifier is derived from both halves of the guard strobe circuit. A discussion of the guard strobe amplifier appears in paragraph 4-2*h*(11).

The guard strobe circuits in the detector-strobe module are identical with the other strobe circuits except for the time that they are triggered from the strobe blocking oscillator. Triggers for this blocking oscillator are supplied from the station selector switch. The actual guard strobe triggers are generated in the code group generator section of the receiver. The guard strobe sampling process takes place approximately 45 microseconds before the other strobes.

Refer to paragraph 4-2*h* for a detailed discussion of the detector-strobe section.

(2) ERROR THRESHOLD DETECTOR (A1601-A1610).

(a) GENERAL. - The error threshold detector senses the output level of one or more of the error amplifiers or other amplifiers and compares the input to an established reference level within the error threshold detector circuit. A relay is de-energized when the applied peak input level becomes more positive than the reference level, causing an alarm light on the front panel of the receiver to light. The major circuits in the error threshold detector are a peak-detecting emitter follower (Q1), a Schmitt trigger (Q2-Q4), and a relay driver stage (Q5). There is also a constant current device (Q3) which operates with the Schmitt trigger.

The circuit changes state only when the input voltage exceeds the reference threshold level. Otherwise, the circuit remains unaffected even though the voltage applied to the input varies up to any amount less positive than the reference voltage. After the circuit has changed state because of a sufficiently large input, a decrease in input to a new reference level, considerably lower than the old threshold voltage, will be required to change the state of the circuit back to its original condition.

(b) DETAIL. - See the schematic diagram of the error threshold detector which appears in figure 6-157. In normal operation, a jumper is connected between terminals 11 and 12. The first stage of the circuit, Q1, is both a peak detector and an emitter follower. It acts as a peak detector by allowing a charge equal in magnitude to the applied voltage to build up on capacitor C1. With a small input, the applied input voltage will be a square wave clamped to ground and less than the reference threshold. Transistor Q1 allows the charge to build up on capacitor to some small degree and cause slight ripple during the cycles of zero applied voltage, but the voltage applied to the base of Q2 remains a nearly constant voltage of a magnitude equal to the applied voltage.

The constant-current characteristic of the circuit is provided by transistor Q3. The NPN transistor, Q3, will always be conducting independently of the action of the rest of the circuit. This is because the base is at ground potential and a negative voltage is applied through resistor R4 to the emitter. Transistor Q3 will continue to conduct with a current of about 1.5 milliamperes as long as the voltage on the emitter remains more negative than ground potential. The voltage level on the collector of Q3 will be changed by action of the circuit, but will never drop to a zero value. The transistor will remain on with a constant current.

Next, consider the function of the Schmitt trigger, Q2 and Q4. The reference voltage for this circuit is established by a voltage divider consisting of R3, R5, R7, R10, and CR4. Zener diode, CR4, maintains a constant voltage drop of 10 volts which is applied across R10. Since the diode represents a very low-impedance to ground, the voltage at the movable arm of R10 is a variable control that may be set between 0 and 10 volts. Ordinarily the setting is close to +3 volts. Assume that Q2 is cut off and the desired reference voltage for the Schmitt trigger is +3 volts. This level is established by adjusting R10 so that the voltage at the base of Q4 (TP1) is +3 volts. There is very little current flow through R7, R5, and R3 with most of the voltage being dropped across R5. Since the emitter of Q4 conducts through a constant source, the level applied at the base of Q4 also appears at its emitter. Consequently, the reference level is effectively applied to the emitter of Q2. When the peak output from Q1 is less positive than the reference voltage, Q2 is cut off because of the reverse bias to emitter. This establishes the level at the collector of Q2 at approximately +15 volts.

The Schmitt detector, Q2 and Q4, also provides the means for switching the alarm relay of the circuit. The switching action from conduction of Q4 to conduction of Q2 and the return switching is made as instantaneously as possible so that relay coil K1 will reflect either alarm or no alarm. Without a feedback resistor between transistors Q4 and Q2, a change of input to the circuit would cause the switching action to occur unsatisfactorily. When the threshold voltage is just barely in the threshold region, Q2 would not turn on completely. This invites sluggish operation. To make any small threshold voltage sufficient to activate relay K1, a resistive voltage divider network reduces the value of the voltage on the collector so that Q2 will completely turn on. As a result, the switching action is positive and definite.

Assume that Q4 is conducting and Q2 is not conducting. A level near ground potential is applied to the low side of resistor network R3, R5, R7, and R10. The high side is connected to +15 volts. Since current is flowing at the junction between R5 and R7 (TP1), the true voltage divider is upset, and a potential of approximately 14 volts is established at the junction of R3 and R5 (the collector of Q2). When Q2 begins to conduct, flow at the R5 and R7 junction decreases and the flow at the R3 and R5 junction (collector of Q2) begins. This changes the balance in the voltage-divider network so that the R3 and R5 junction is at a less positive potential than before. Transistor Q2 now conducts harder. This speed-up action continues until Q4 is no longer conducting and Q2 is completely turned on. The acceleration of the switching action is so great that, essentially, the switching has occurred instantaneously.

Not only has the R3 and R5 junction changed potential, but so has the junction of R5 and R7. Therefore, the input voltage will have to decrease below the new threshold level of the voltage on the base of Q4 before Q2 will turn off. Of course, when the action does start turning off Q2 and turning on Q4, the acceleration is similar to the action described above and the switching is nearly instantaneous again. The value the input voltage must be to cause the circuit to switch in one direction compared with what it must be to cause it to switch back in the opposite direction is the inherent hysteresis of the circuit.

Hysteresis is not actually necessary for the successful operation of the circuit. All that is necessary is a positive switching action in both directions. Hysteresis achieves this result without being detrimental to the circuit operation. The effects of hysterisis are minimized by utilizing a Zener diode for establishing a low-impedance source. The circuit adjustment is highly sensitive so that even a voltage extremely close to the threshold value will change the state of Q2 and Q4. Because of hysteresis, when the value reduces slightly below the value that originally caused the circuit to change state, the circuit will not switch back. A new reference threshold level, lower than the first, will be required to switch the circuit back to the original state. The undesirable effect of relay chatter is also eliminated by hysteresis.

When transistor Q4 is conducting, with a current flow of approximately 1.5 milliamperes, the voltage established by R6 at the collector of Q4 (base of Q5) will be approximately 3 volts below the +28-volt bias (approximately +25 volts). Diodes CR1 and CR2 are forward-biased so that the voltage on the emitter of Q5 is approximately +27 volts, which is more positive than the collector of Q4. Resistor R8 is a bleeder resistor that maintains current flow through the diodes. Since this transistor is a PNP transistor, it is properly biased to conduct. When the transistor conducts, the emitter voltage energizes relay K1. The result is that the relay coil remains energized even though the applied threshold voltage may have returned to a value slightly less than the value originally needed for the relay to become initially energized. Diode CR3 is shunted across K1 to prevent inductive back-emf from applying unnecessary negative spikes to transistor Q5 when the relay is deenergized.

(c) OTHER APPLICATIONS. - The error threshold detector is used in several of the other error detection circuits. In general, a jumper is

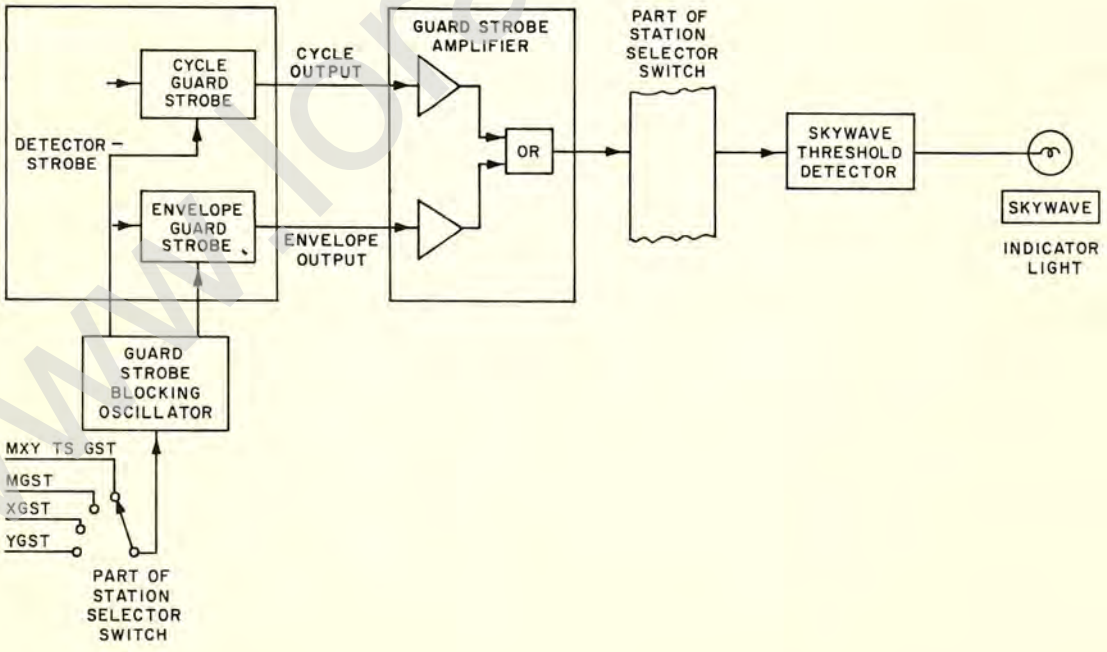


Figure 4-86. Guard Signal Path, Block Diagram

placed between terminals 11 and 12, which makes Q1 a peak detector. However, the jumper is removed for low frequency application, which removes C1 from the circuit. An example of this application is with the blink light amplifier. In this case, the applied signal is of such low frequency that the charge on capacitor C1 would follow the frequency variations if it were still in the circuit. Since the frequency is slow with respect to the switching action of the Schmitt trigger (Q2 and Q4), the capacitor is not required. Transistor Q1 now functions only as a straight emitter-follower d-c amplifier.

m. RECEIVER SEQUENCE CONTROL.

(1) GENERAL. - The station selector switch (S1003) is the heart of the sequence control of the receiver. The interconnection of this switch is illustrated in figure 5-12. A few fundamental concepts will be helpful in understanding the operation of the sequence control.

(a) When there is no input being received by the circuit shown on the diagram (complete absence of signal or signal is locked on), there is a zero input from the strobe amplifiers.

(b) When there is an error, the strobe amplifier output may indicate either a positive or a negative error. However, the threshold circuits only operate with a positive input. Therefore, the output from the error amplifier is always positive.

(c) As a result of *(a)* and *(b)*, when there is no signal, the thresholds from the derived envelope and cycle strobes are energized and the relay contacts are in the closed positions.

(d) When there is an input from the strobes (before lockon), there will be an amplified error to the threshold circuits which will deenergize the related relay.

(e) The agc (envelope) strobes, integrators, and threshold circuits differ slightly from the derived envelope and cycle circuits. There is a reference level applied to the agc strobe amplifier circuit of sufficient value for the signal at the output of the r-f amplifier to be 0.25 volt at the 30-microsecond strobe point. Only the reference is reflected in the strobe-amplifier output when there is no signal applied to the strobe. The integrator will provide a positive output to the threshold circuit for the no-signal condition. The integrator output will be negative when a signal to the receiver is present. The threshold circuit relay will be energized when the integrator output is negative.

(2) LOCKING IN ON THE MASTER STATION USING THE M SWITCH POSITION. - Initially, the station selector switch is set to the M position and no signal is locked on. Slew action has not been started.

(a) The LOST SIGNAL light will not be on. Since search is usually performed with the manual GAIN CONTROL knobs away from the AGC position, there will never be an input to A1608, the master lost signal threshold, from the master gate. The only path for the LOST SIGNAL light is through the contacts of K1010. Relay K1010 can only receive a ground energizing signal through wafer D Rear of S1003 and terminals 7 and 4 of A1608.

(b) Either the LEFT or the RIGHT button is depressed to initiate master slew action. Assume that the RIGHT button is chosen.

1. Ground is supplied through S1005 to K1001, which energizes and latches its associated contacts.

2. Ground is also applied to K1002 and K1003 through diode CR1022 when K1001 energizes. A holding ground is provided for K1002 through its own contacts 8 and 3, contacts 8 and 1 of STOP button S1006, contacts 12 and 8 of S1003B Rear, and terminals 6 and 4 of MSS error threshold detector A1602.

3. Similarly, K1003 is held energized through the same contacts of K1002.

4. Ground is also supplied to the RIGHT indicator light through contacts 6 and 2 of K1001.

(c) The subtraction or addition of pulses to the master loop is made through terminal 6 of SPEED switch S1007A, through contacts 3 and 8 of K1003, and contacts 7 and 6 of S1003E Front to monostable multivibrator A940-7.

(d) The counter in the pulse-rate generator will add or subtract according to the information supplied through the direction relay. If K1001 is in the right position, the slew gate relay is activated and the pulses added. There is a subtraction of pulses if no input is supplied to the slew gate (relay K1001 is in the slew left position).

(e) The following sequence occurs when the receiver comes across a detectable signal.

1. There will be a detectable error in the derived envelope and/or cycle strobe. Assume that there is a detectable error in the derived envelope strobe.

2. The error will be amplified by the M derived envelope error amplifier, A1617.

3. Output from terminal 14 is applied through contacts 2 and 6 of S1003C Rear to terminal 10 of the envelope error threshold detector A1605, which lights the ENVELOPE ERROR light.

4. Output from terminal 13 is applied to MSS (derived envelope-cycle) threshold A1602. When the signal is sufficiently large, the normally energized relay in A1602 will deenergize, opening its contacts. The slew path described in 4-2*m*(2)*(b)* 2 is broken at terminals 6 and 4 of A1602.

5. Output from terminal 12 is open at wafer S1003C Rear.

6. A similar sequence would occur if there was a detectable error in A1618, lighting the CYCLE ERROR light and triggering the MSS threshold (A1602).

NOTE

The envelope error and cycle threshold detectors A1605 and A1606 are more sensitive than A1602. This means that the error lights can flash without the slew action being stopped.

(f) Eventually, slewing will stop when the master signal begins to lock on.

1. The direction light will go out. The ground path for the light is through contacts 6 and 4 of A1602, contacts 8 and 12 of S1003B Rear, contacts 1 and 8 of STOP button S1006, and terminals 3 and 8 of K1002. Contacts 6 and 4 will open when the threshold is triggered.

2. This same path is the holding path for relays K1002 and K1003 at contacts 2 and 8 of K1002. When K1002 deenergizes, this prevents the direction light from lighting again when the error signal to A1602 is reduced.

(g) After there is a small detectable error signal in the loop K1003 deenergizes, the path from the PRR counter to the monostable multivibrator through S1007, contacts 3 and 8 of K1003, and contacts 6 and 7 of S1003E Front will be broken. The error remaining will be cranked out by the servo-loop due to the signal that is applied to the cycle error amplifier from the strobe amplifier, and also to the operational amplifier. This is the signal present at terminals 4 and 5 of A1618.

(h) When the error is completely removed from the cycle and envelope loops, the error signals applied to A1605 and A1606 will be reduced sufficiently for the ENVELOPE ERROR and CYCLE ERROR lights to go out.

(i) After the master loop is locked on, the M GAIN CONTROL may be placed to the AGC position. The developed agc voltage will be supplied to A1608. As long as the received signal is locked on, there will be sufficient signal to trigger the circuit and light the LOST SIGNAL light. If the signal is lost, the light becomes lighted through the contacts 8 and 3 of K1010 when K1010 is energized through contacts 8 and 12 of S1003D Rear and terminals 4 and 7 of A1608.

(j) The SKYWAVE light would have come on when the signal was first detected if the detected signal had been a skywave. This is because the guard strobes (strobing approximately 45 microseconds ahead of the skywave) would also have detected a signal and applied an input to A1607. After complete lockon, it is possible to jump off the skywave by manually depressing the slew LEFT button until the light goes out.

(k) When the signal being received by the r-f amplifier becomes large enough to endanger saturation of the amplifier, a signal is supplied through the contacts on S1003D (Rear) to the receiver overload detector, A1620. When this detector is triggered, there is an output applied to the SIGNAL OVERLOAD indicator light.

(3) LOCKING IN ON THE SLAVE STATIONS USING THE X(Y) AND Y(Z) POSITIONS. - Assume that the master station has been locked on, but the slaves have not. The station selector switch is placed in the X(Y) position.

(a) The LOST SIGNAL light will not be on since the manual GAIN CONTROL knobs are being used and not AGC.

(b) Either the LEFT or the RIGHT slew button is depressed to initiate slew action. It is assumed that the RIGHT button is chosen.

1. Ground is supplied to K1001, which, in turn, energizes K1002 and K1003. After the slew button is released, K1002 and K1003 remain energized through the contacts of K1002. The remainder of the path is the same as described in paragraph 4-2m(2)(b).

(c) The slew action for the slaves is determined by the speed of the servos and not by adding or subtracting pulses to or from a counter. The path for this is through S1007A Rear (SPEED switch), contacts 7 and 4 of K1003, terminals 5 and 3 of S1003A (Rear), to the X-slave delay servo package.

(d) There will be a detectable error in either the derived envelope error amplifier (A1615) or the cycle error amplifier (A1616), or both, when the receiver starts to lock on. It is assumed that there is an error detected in the X derived envelope strobe.

(e) The X derived envelope error amplifier, A1615, will be triggered, activating A1603. When A1603 is triggered, the ground path in the slew path is broken, similar to the action for the master. The direction light will go out.

(f) The CYCLE ERROR and the ENVELOPE ERROR lights go out only when the error is reduced to the very small operating value. Either light may go out before the other since the envelope and cycle loops operate independently.

(g) As with the master, the manual GAIN CONTROL knobs may be placed in the AGC position when lockon has been accomplished. Now, should X be lost (if S1003 is in the X(Y) or OPR position), there would be a signal detected by A1609, the X lost signal threshold detector. This would activate the LOST SIGNAL light through the same path as that of the master. Refer to paragraph 4-2m(2).

(h) A similar action for the Y-slave will happen when the Y position of the station selector switch is used.

(4) OPR (OPERATE) POSITION. - All of the lights should remain off when the station selector switch is set to the OPR position after lockon is achieved.

(a) The lost signal light is off because none of the signals from the agc gates are sufficiently strong to trigger a lost signal threshold circuit, A1608, A1609, or A1610.

(b) There are no errors being sensed by either the derived envelope strobes or by the cycle strobes sufficiently large enough to trigger A1602, A1603, or A1604 or to light an error light.

(c) When an error amplifier circuit receives an error signal, this information is supplied to the CYCLE ERROR or ENVELOPE ERROR lights through switch S1003C (Rear). Diodes are used in the outputs of the error amplifiers so that ground will not be reflected into the other two circuits should only one station signal be lost.

(5) M MULT (MASTER MULTIPLE) POSITION.

The master multiple circuit consists of the items shown in figure 4-87. Basically, the M MULT position of the SEARCH SELECTOR CONTROL allows for a much speedier method of locking in on the master signal. Each of the error threshold detectors (master derived envelope-cycle, X derived envelope-cycle, and Y derived envelope-cycle) will sense signal when a master M1 signal is received. Noise may cause an error threshold detector to trigger in a few infrequent instances, but provisions are made to allow the operator to determine whether or not noise causes the triggering. Neither a slave signal or an M2 code group will be sensed by the threshold detectors.

There are two portions of the master multiple circuit. The first portion consists of the threshold detectors and relays K1011, K1012, and K1013. The second portion includes the resistors, Shockley diodes, and the XTH and YTH toggles. The relays in this circuit are numbered in the 1000 series (indicating that they are part of the chassis wiring). However, they are silk-screened on the board with only the last two digits.

It is assumed that the normal condition of master M1 signal is being sensed by the master threshold detector. During search, ground was provided to slew relay K1002 through contacts 8 and 11 of STOP switch S1006, through wafer BR of S1003, through the energized relays in A1604 and A1603, through deenergized contacts 4 and 6 of relay K1011, through the energized relay in A1602, to ground. Notice that the relays internal to error threshold detectors A1602, A1603, and A1604 are in the energized condition when there is no error signal being detected. When a master M1 signal is received and sensed by the master derived envelope-cycle threshold detector, the relays in this unit (A1602) deenergize. This opens the ground path of slew relay K1002 and provides a ground path to relay K1011. When K1011 latches, the possibility of providing a ground to either slew relay K1012 or K1013 is removed at pins 6 and 4 of K1011. When K1011 latches, it removes the possibility of providing a ground to either K1012 or K1013, even when the relays within A1603 and A1604 deenergize. When K1011 energizes, contacts 8 and 3 of K1011 close and provide a path to ground through contacts 6 and 4 of deenergized relay K1002. This path remains after the relays in A1602 energize.

It is assumed now that, instead of a master M1 signal being sensed by A1602, a master M1 signal is sensed by A1604. The relays in this unit deenergize, removing ground from slew relay K1002 and furnishing a ground to K1012, which causes it to energize. When K1012 energizes, it obtains a ground path through contacts 3 and 8 of K1012 and deenergized contacts 4 and 6 of slew relay K1002. When K1012 energizes, contacts 4 and 7 of K1012 close and provide a path for the 28 volts to terminal 2 of the STOP switch, S1006. A signal sensed by A1604 would ordinarily energize K1013. It will not be able to after K1012 energizes. Relay K1011 will energize if a later signal is sensed by A1602, but this has no effect on the remainder of the circuit.

If a master M1 signal triggers A1604, the Y derived envelope-cycle error threshold detector, a similar sequence of relay energizing and path blocking will enable 28 volts eventually to be applied to the YTH toggle and will prevent 28 volts from being applied to the XTH toggle.

It is assumed now that noise sufficient to light the ERROR lights and stop slew action is being sensed by A1602, A1603, or A1604, instead of master M1 signal. The operator needs only to watch for intermittent flashing of the CYCLE ERROR and ENVELOPE ERROR lights to determine whether signal or noise triggered a detector. When the lights remain on, SEARCH SELECTOR CONTROL S1003 should be switched from the M MULT position to the M position. This effectively erases all memory from whichever relay coil is energized (K1011, K1012, or K1013) by removing the ground and 28-volt d-c paths. The operator can observe that the CYCLE ERROR and ENVELOPE ERROR lights will remain lighted if the receiver is close to locking onto the M1 signal (in the M1 gate). The lights will not come on if the M2 signal or any one of the slave signals are in the M1 gate because of an absence of error signal in the loops being detected. The operator then should turn switch S1003 back to M MULT. The receiver is detecting a valid signal if the indicator lamps light now, but it is in a gate other than M1. If the lights do not come on, then the threshold detector that stopped the slew action was triggered by noise. If the received signal is in any of the gates, the relay energized originally will energize again. After the operator determines that the receiver has been triggered by noise instead of signal, he can initiate slew action for a valid signal by depressing one of the slew buttons, thereby energizing relay K1002.

When a valid signal is known to be detected, depending on which threshold detector senses the signal, the situation is now ready to transfer the code counting within the receiver to correspond with the received signal. There is no need to change the timing if the master M1 signal has been detected by A1602. The 28-volt bias is prevented from being applied to the second portion of the master multiple circuit. If A1603 has sensed the received signals, 28 volts is ready to be applied to the second portion of the circuit at pin 2 of switch S1006. If A1604 has sensed the received signal, 28 volts is in position to be applied at pin 3 of S1006.

It is assumed that 28 volts is applied to pin 2 of S1006. A circuit is established as shown in figure 4-88 when the STOP switch is depressed.

When 28 volts is applied, there is a voltage divider established that applies approximately +14 volts at the anode of the Shockley diode. The toggle will trigger, but the Shockley diode will also conduct, establishing its anode at a negative value, which is just slightly more positive than the -15-volt bias applied to its cathode. The value is considerably more negative than the voltage applied to the OR gate diode in the toggle circuit and clamps the toggle input to ground. There is a path to ground and sufficient current to keep the Shockley diode conducting even when +28 volts is removed from the top of the voltage divider. Therefore, the toggle input remains at ground when +28 volts is reapplied to the voltage divider. The +28 volts will not affect the toggle action.

The YTH toggle is triggered in a similar manner by depressing STOP switch S1006 when A1604 has

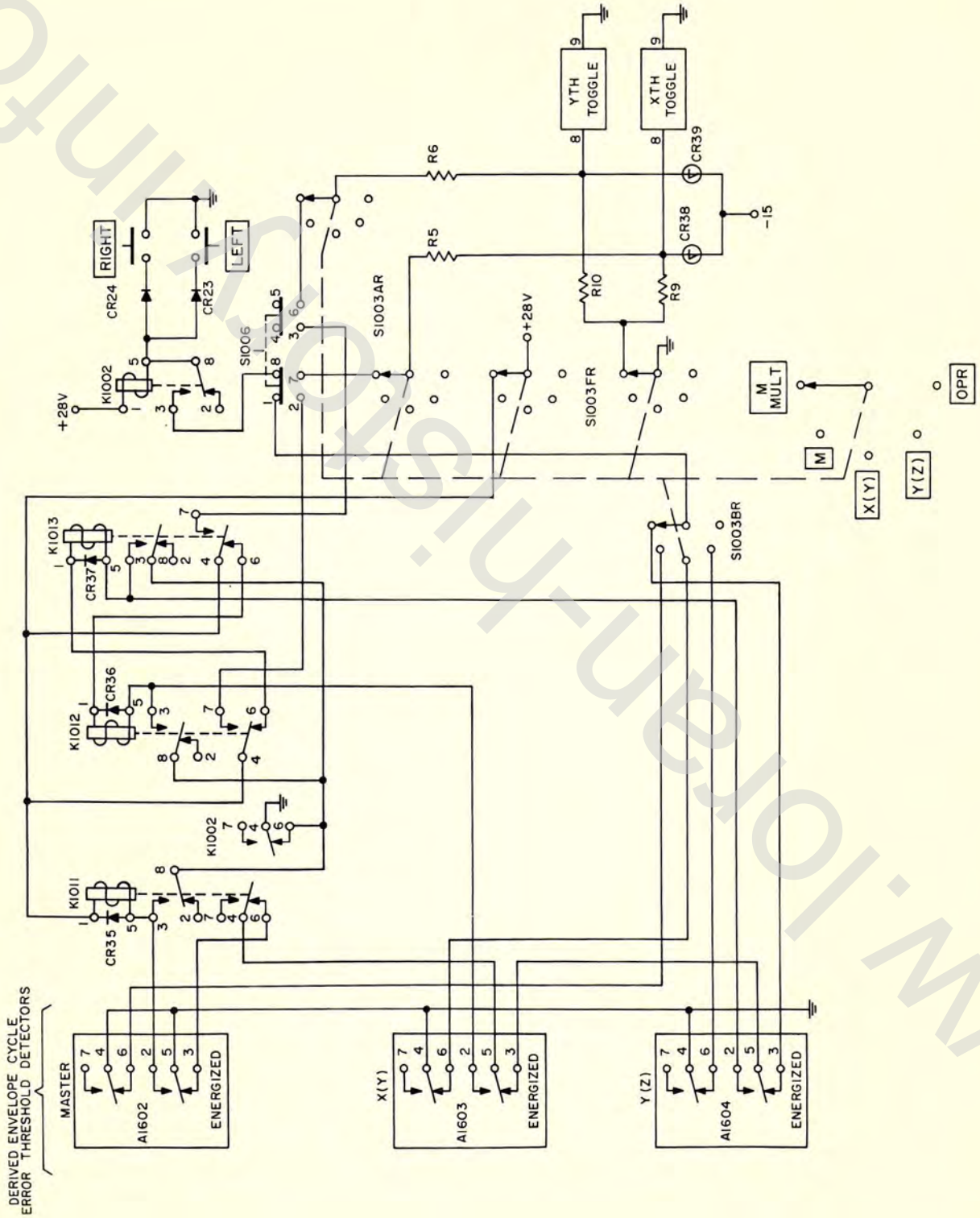


Figure 4-87. Master Multiple, Simplified Schematic Diagram

energized K1013. There is only one way to reset the triggering circuit once either XTH toggle A927 or YTH toggle A928 is triggered and Shockley diode CR1038 or CR1039 conducts. The ground path is broken and the Shockley diode is cut off when the SEARCH SELECTOR CONTROL is set to any position other than M MULT.

(6) SPECIAL CONDITIONS AND PROVISIONS. - There are several special conditions and provisions that may be encountered during lockon or after lockon has been accomplished.

(a) BLINKING SLAVE. - The blink light circuit consists of a blink light amplifier, a blink light error amplifier, and a threshold detector circuit. When a slave station signal is blinking, it does so at a rate of 0.667 cps. When the SEARCH SELECTOR CONTROL is in the OPR position, contact 12 is connected to both contact 10 and 11 of S1003E Rear. These connections are, in turn, connected through 47,000-ohm resistors to the envelope strobe outputs for slaves X and Y. These resistors are large with respect to the output impedance looking back into the strobe circuits, so the feedback from one strobe to the other is very small. However, by being tied together in wafer S1003E Rear, the blink light circuit samples both strobe outputs. If either one begins to blink, the light will so indicate. To determine whether X or Y is blinking, the station selector switch is placed first in the X and then in the Y position. Notice that in each of these positions, only one signal is applied to the blink light circuit.

(b) GROUP ALTERNATE. - The GROUP ALTERNATE switch may be used to switch the coding in the receiver one complete period to assist quick slewing, particularly when used in conjunction with the indicator. This adjustment instantaneously transfers the code groups so that M1 is now in the former position of M2 and M2 is in the former position of M1.

(c) EXCESS DELAY. - An important special feature is provided by the EXCESS DELAY light. In time sequence, the pulses arrive at the receiver in an M-X-Y order. After the master signal has been locked on, the range for the X and Y signals are limited. That is, the leading edge of the X-slave signal cannot occur any sooner than the trailing edge of the master signal and the trailing edge of the X-slave signal cannot occur any later than it is possible for the leading edge of the Y-slave signal to occur. A similar limitation is placed on the slew action of the Y-slave. That is, the leading edge of the Y-slave cannot occur before the latest possible trailing edge of the X-slave. Neither can the trailing edge of the Y-slave occur after the leading edge of the master signal. This means that the EXCESS DELAY light will light if a slewed slave signal encroaches on an adjacent pulse rate period in either direction. Also, the corresponding slew coil of K1001 will energize through switch S1003E Front. Now, whereas the slewing for a station may have been right, it is now reversed and will be left.

When the overlap of signals occur, a path is also closed for activating MSL, XSL, or YSL coils until the slew action reverses. This causes one of the signals to disappear by action of the slew limit circuitry in the receiver.

n. ERROR INDICATORS.

(1) LIGHTS. - The indicator lights on the front of the receiver chassis are the following:

1. HEATER on
2. RCVR on
3. BAND PASS
4. SKYWAVE
5. BLINK
6. LOST SIG
7. EXCESS DELAY
8. ENVL ERROR
9. CYCLE ERROR
10. SIGNAL OVERLOAD
11. AMBIGUITY (4)
12. LEFT slew
13. RIGHT slew

The function of the lights have been explained in section 3, Operator's Section. Generally, they indicate an operating condition (e.g. RCVR on, slew LEFT, etc.) or a presence of a detected, unwanted signal (e.g. BLINK, ENVL ERROR, etc.). The lights glow red when lighted, except for the HEATER and the RCVR lights, which glow green. Only the two green lights should be lighted before a reliable reading can be taken. Depress the frame of the lights so they give a glow indication to determine if they are in good working order.

(2) RECEIVER OVERLOAD CIRCUIT (A1620).

(a) GENERAL. - The receiver overload circuit detects conditions of receiver overload and actuates an alarm relay. When the receiver overload circuit input (agc integrator output) goes more negative than -6 volts, the r-f section of the receiver begins to saturate. An alarm light is used to warn the operator of overload conditions.

(b) DETAIL. - See figure 6-159 for the schematic diagram of the receiver overload circuit. First, consider the circuit condition when the input is less negative than -6 volts. This is the condition when the applied voltage is within normal operating limits. Assume a level at the base of Q1 (a PNP transistor) that is less negative than the emitter voltage of -6 volts. Transistor Q1 is cut off, there is no voltage drop across R4, and the collector of Q1 rests at a level of -10 volts. This is the potential established by the constant voltage drop through Zener diode CR3. The NPN transistor, Q2, is cut off when the base voltage is less positive than the emitter voltage. The level of -10 volts applied to the base of Q2 is less positive than the emitter since there is a constant voltage drop of approximately 0.5 volt through diodes CR1 and CR2. This keeps Q2 cut off. When Q2 is cut off, there is no current flow through K1, and the relay is deenergized.

Next, the circuit conditions should be considered when the input is more negative than -6 volts, the conditions of fault. The level applied through R2 to the base of Q1 is more negative than the level applied at the emitter of Q1 and the transistor conducts. The current through Q1 causes a voltage drop across R4 and produces a level of approximately -6 volts at the

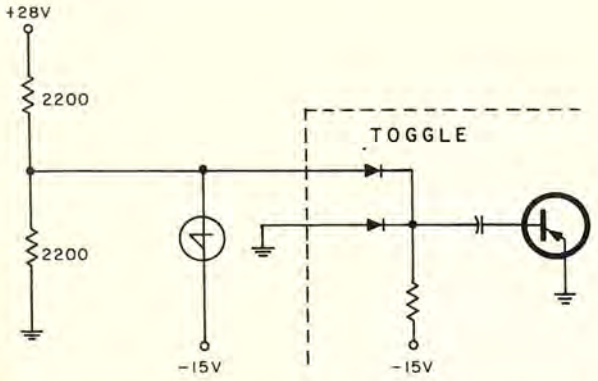


Figure 4-88. Trigger Circuit for XTH or YTH Toggle

base of Q2. Transistor Q2 conducts when the base voltage (-6 volts) is more positive than the emitter voltage (-9.5 volts). There is now current flow through K1, and the relay is energized. Also, observe the action of divider R3, R2, and R1. The current flow through K1 and R7 causes the voltage at the collector to go in a negative direction. This negative-going voltage is applied back to the base of Q1 and aids the externally applied negative signal. This amounts to regenerative feedback and causes Q1 to conduct harder than it would if it were dependent on the applied signal alone. This, in turn, causes Q2 to conduct harder than it would if it were dependent on the applied signal alone. The circuit rapidly reaches saturation to close the relay and hold it in the energized position. As a result of this feedback, almost instantaneous switching occurs when the circuit input goes more negative than -6 volts.

Since it is desirable that the activating voltage for relay K1 does not exceed +28 volts, diode CR4 is utilized. Regardless of how far below -6 volts the voltage on the low side of relay K1 becomes, it will never become more negative than ground potential. Current through R7 limits the voltage and diode CR4 prevents spikes. Since a +28-volt bias is applied directly to the high side, a +28-volt potential difference is the maximum voltage that can be applied to the coil.

When the input voltage to the circuit again reaches a value more positive than -6 volts, the emitter of PNP transistor Q1 will again be more negative than the base of Q1, cutting off Q1. When Q1 cuts off, the collector of Q1 becomes -10 volts again and Q2 cuts off. Resistor R5 maintains a slight drop across diodes CR1 and CR2 so that the emitter of Q2 will remain slightly less negative than the -10 volts on the base. After Q2 cuts off, there will be no current flow in the collector circuit, so that all of the points around the collector will be at a +28-volt potential. Relay K1 will deenergize and open the alarm circuit since there will be no potential across its coil.

Resistor R7 is a protective dropping resistor for Q2, lowering the collector potential of Q2 to -6 volts. Diode CR4 protects Q2 from surge voltages when relay coil K is deenergized.

(3) ERROR AMPLIFIER (A1611-A1619).

(a) GENERAL. - The error amplifier senses the level of the strobe amplifier output, converts this d-c input to a 400-cps square wave, and amplifies the result for application to an error threshold detector circuit. The circuit is composed of two major units, a chopper (Q1-Q2), and a 2-stage amplifier (Q3-Q4). Provisions are made in the output circuit to combine two or more of the error amplifier outputs through an OR circuit.

(b) DETAIL. - See figure 6-158 for the schematic diagram of the error amplifier circuit. The input RC network, consisting of capacitor C1 and resistors R1 and R2, prevents chopped signals from appearing on the strobe output wave. It also supplies transistor Q1 with a certain d-c level which follows the applied strobe level. Transistors Q1 and Q2 and transformer T1 act as a chopper device to produce the desired waveshape applied to the amplifier portion of the circuit. A 20-volt rms, 400-cps voltage is applied to the primary of transformer T1. The secondary voltage on this transformer is 8 volts rms with a center-tapped connection. One half of the secondary value, which is 4 volts rms or 5.6 volts peak, is much larger than any voltage that will ever appear on the emitter of Q1. The chopper circuit alternately selects the emitter voltage on Q1 and the emitter voltage on Q2. When the 400-cps voltage is going through its positive cycle, the base voltage on Q1 will be larger than the voltage on the emitter, and the transistor will be cut off. During the negative half cycle, the transistor will be biased so that the transistor will turn on and the emitter voltage will be reflected in the collector circuit. The positive half cycle for Q1 is the negative half cycle for Q2, since the base of Q2 is tied to the other side of the transformer. Thus, while the emitter of Q1 is being sampled, Q2 will be cut off. Conversely, Q2 will be turned on while Q1 is cut off, and the emitter voltage of Q2 will be sampled. This is ground potential. The output from the chopper is, therefore, a 400-cps square wave, with one side grounded and at a magnitude equal to the strobe input.

Next, consider the operation of the amplifier circuit. The chopper output is applied to the base of Q3 through C1. Emitter follower Q3 is biased by divider R5-R6 and is always conducting. The square wave applied from the chopper is passed through Q3 and applied through C3 to the base of amplifier Q4. The gain of Q4 is adjusted by varying the degree of negative feedback in the emitter of the amplifier. Capacitor C4 is a bypass path that determines the amount of negative feedback that appears at the emitter of Q4. The output of Q4 is developed across the inductive load, L1, and is coupled to the output components through C5. The output level is clamped to ground potential by CR1 so that a negative voltage will not appear at the output. Consequently, the output will swing from a zero level to some positive level.

Three outputs are provided. Output 1 (terminal 2) is direct and output 2 (terminal 3) passes through CR2 that makes up part of a positive OR circuit when connected with the number 2 output of another error amplifier circuit.

(4) BLINK LIGHT AMPLIFIER (A1621).

(a) GENERAL. - The blink light amplifier circuit is basically a bandpass amplifier employing carefully controlled positive feedback. The input to the circuit is a nonsymmetrical triangular wave at 0.667 cps, which is amplified and applied to an indicator light. The blinking signal shows that a slave station is not properly phased with the master station. The Q control, which is the bandwidth control, can be accurately adjusted to respond to a frequency of 0.667 cps. A Q in the order of 15 or 20 is sufficient to reject any undersirable frequencies that might otherwise activate the circuit.

(b) DETAIL. - See the schematic diagram of the blink light amplifier, figure 6-160. The value of Q in the circuit is controlled by two groups of parameters: those in the collector circuit of Q1, and those in the emitter circuit. The circuit is very closely dependent on the exact relative adjustment of these circuit parameters, and the fact that the values are not precisely the same from unit to unit makes it necessary to provide manual adjustment facilities. It is desirable to make two types of adjustments: the bandwidth (or Q) adjustment, and the center frequency (CF) adjustment. By adjusting the Q-response of the circuit, frequencies not in the range of the center frequency, 0.667 cps, may be filtered out so that they will not be amplified and applied to the blink light indicator. To minimize the number of adjustments, a resistor in the collector circuit of Q1 and a resistor in the emitter circuit are ganged together. These linear potentiometers are R4A and R4B. As the resistance value of one circuit is increased, the resistance of the other circuit is decreased. This effectively changes the positive feedback of the circuit, and thus the Q, without changing the center frequency value for which the circuit is tuned. In making this adjustment, the time constant of the collector circuit changes in one direction while the time constant of the emitter changes in the opposite direction.

The second adjustment that may be made is the adjustment of the center frequency. This is accomplished by changing the resistive values of both circuits in the same direction. That is, when the resistance of the collector circuit is increased, the resistance of the emitter circuit is also increased. This is accomplished by ganging CF resistors R5A and R5B. By adjusting both of these resistors simultaneously, the Q-adjustment is not appreciably affected.

A Zener diode is inserted in the emitter circuit to drop the -6-volt d-c output level to approximately -1.4 volts. The diode does not limit the a-c signal level applied to the error amplifier circuit.

o. POWER SUPPLIES. - There are three power supplies for the receiver circuits: the low voltage power supply (+6, -6, +15, and -15 volts regulated), the high voltage power supply (+130 and +150 volts regulated and +200 volts unregulated), and the 28-volt power supply (+28 volts regulated and +28 volts unregulated).

(1) LOW VOLTAGE POER SUPPLY (A2201).

(a) GENERAL. - The low voltage power supply module supplies regulated d-c outputs of +15 volts, -15 volts, +6 volts, and -6 volts to the receiver circuits. The module contains a transformer, four rectifiers, four filters, four control amplifiers, and four regulators. The four regulator circuits are very similar; therefore, only the +15-volt circuit is discussed in detail.

(b) DETAIL. - See figure 6-165 for the schematic diagram of the low voltage power supply. The output from the transformer secondary (pins 5, 6, and 7) is applied to rectifiers CR2201 and CR2202, filtered by C2201, and applied through 3/4-ampere fuse F2201 to the +15-volt regulator circuit. The functions of the various components in the regulator are as follows:

1. Constant voltage reference -- CR2204 and R2203
2. Variable voltage reference -- R2205, R2206, and R2207
3. Control amplifier ---------- Q2203
4. Regulator driver ---------- Q2202
5. Series regulator ---------- Q2201
6. Bias reference ---------- CR2203
7. Output adjustment (ADJ) ----- R2206

Regulation is maintained in the following manner. A constant voltage reference (approximately 10 volts) is established at the emitter of Q2203 by the drop across CR2204 and R2203. A portion of the total output voltage is appled from divider R2205, R2206, and R2207 to the base of Q2203 through R2204. The difference between the voltages on the base and emitter of Q2203 will cause Q2203 to conduct. This develops a voltage level across the collector load, R2201, that is applied to the base of Q2202. Transistor Q2202 will then conduct through R2202. The voltage across R2202 establishes the voltage applied to the base of Q2201. Emitter bias for Q2201 is established by the constant drop across CR2203, which is biased in a forward direction. The difference between the emitter and base voltages on Q2201 establishes the conduction and its effective impedance in the circuit. The desired +15 volts is derived from the collector ofQ2201. Capacitors C2202 and C2203 are placed in the output of the regulator circuit to provide filtering and to eliminate the possibility of the regulator loop from oscillating.

Next, it is assumed that the +15-volt level rises to +16 volts. Since the emitter level of Q2203 is fixed, the rise in output level is divided and applied to the base of Q2203. This causes Q2203 to conduct more heavily, lowering the voltage at the base of Q2202. The PNP transistor, Q2202, conducts more heavily and drives the base of Q2201 more positive as the base voltage on Q2202 moves toward the collector voltage. The PNP transistor, Q2201, conducts less as the base voltage moves to a value closer to the emitter voltage. The drop across Q2201 increases (emitter to collector), and the output level returns to its normal level of +15 volts.

The circuit of the -15-volt regulator is similar to the +15-volt regulator. However, the -15-volt load current is approximately two times that required of the +15-volt supply. Consequently, transistors Q2204 and Q2213 are connected in parallel to carry the load. Resistors R2227 and R2228 are small resistors used in the emitter circuits to equalize the current and to balance the load through the two transistors.

The circuit functions of the two 6-volt regulators are similar to the +15-volt regulator. However, the constant voltage Zener diodes, CR2212 and CR2216, operate in the region of 2.5 volts. Thermistors RT2201 and RT2202 are added to these regulators for temperature stabilization.

(2) HIGH VOLTAGE POWER SUPPLY (A2301).

(a) GENERAL. - The high voltage power supply module supplies regulated outputs at +130 volts, +150 volts, and unregulated +200 volts dc for the receiver circuits. The power supply contains a transformer, a rectifier, a control amplifier, and a regulator output stage. Reference voltages are maintained by the use of Zener diodes.

(b) DETAIL. - See figure 6-166 for the schematic diagram of the high voltage power supply. Primary a-c input power is applied to transformer T2301; taps are provided for input levels of 105 volts, 115 volts, and 125 volts. The 105-volt and 125-volt taps may be used if the source voltage is at some level other than the normal 115 volts. The output from the transformer secondary is applied to bridge rectifier CR2301, CR2302, CR2303, and CR2304, which is referenced to ground. The positive rectifier output is filtered by L2301-C2301 and applied to the regulator circuits through a 3/8-ampere fuse, F2301.

The actual voltage regulation is accomplished by Zener diodes. The primary reference level of 150 volts is set by two 75-volt Zener diodes, CR2306 and CR2307. A constant current through these diodes is maintained by Q2301. Transistor Q2302 functions as the output-current source since the output-current requirements of the module exceed the ratings of the reference diodes. The external load for the emitter of Q2302 is comprised of R2306 and R2309. Since the base of Q2302 is established at a constant reference level, the emitter also maintains the same constant level, 150 volts. The current drain at the 130-volt level is relatively small (only approximately 10 milliamperes) and does not tend to cause excessive voltage drop in the two resistors.

Assume that the output voltage from the rectifier rises. The voltage at the base of Q2301 rises a similar amount because of the constant voltage drop across CR2305, a 10-volt Zener diode. Since the emitter and base voltages at Q2301 change together, the current through CR2306 and CR2307 is held constant and the regulator output at the emitter of Q2302 also remains constant.

Assume the external load current is doubled. The drop across R2301 increases because of the added current through Q2302. This change in voltage is also reflected at the base of Q2301 as a negative-going voltage, since the drop across CR2305 follows the drop across R2301. The negative-going voltage at the base of Q2301 tends to make it conduct harder. However, the emitter of Q2302 follows the base voltage and stabilizes the current through CR2306 and CR2307. The current through the reference diodes holds the voltage at the base of Q2302 at a constant level. Therefore, the output level will also remain constant.

A simplified circuit of the unregulated power supply is shown in figure 4-89. Capacitors C1021 and C1022 and inductor L1004 are mounted on the chassis because of their large physical size. These components filter the unregulated output. Diode CR2308 isolates the unregulated supply from the regulated supply.

To summarize, transistors Q2301 and Q2302 are basically current sources, Zener diodes CR2306 and CR2307 actually are voltage regulators for the +150-volt and +130-volt outputs, and diode CR2308 is the isolation diode for the unregulated +200-volt output.

(3) 28-VOLT POWER SUPPLY (A2401).

(a) GENERAL. - The 28-volt power supply module supplies both regulated and unregulated +28-volt power for the receiver. The circuit consists of two basic portions: a rectifier, a filter, and a regulator for the transistor power output and a rectifier; a filter, and a blocking diode for the heater supply to the 100-kc reference oscillator. Notice that the regulated +28-volt output line is connected externally to the RCVR (receiver) ON-OFF switch so that the transistor output supply can be turned off without disturbing the 100-kc reference oscillator heater supply. Regulation of this unit will withstand input variation up to plus or minus 10 percent.

(b) DETAIL. - See figure 6-167 for the schematic diagram of the +28-volt power supply. Consider first the circuit of the regulated portion of the power supply. The a-c input is applied to a full-wave rectifier, CR2403 and CR2404, through one secondary of transformer T2401. Capacitors C2409 and C2410 across diodes CR2403 and CR2404 function as a filter for the noise generated by the silicon diode rectifier by suppressing the noise peaks. Notice that the center tap of this secondary is not returned to ground. Since this is the case, the whole portion may be considered as floating. Actually, this circuit may be considered to be a controlled voltage-dropping device. A change in the impedance of the series regulator circuit will change the voltage drop across the load. Series regulator Q2401-Q2403 is placed in the negative side of the circuit because of the characteristics of the transistors used in this circuit. The

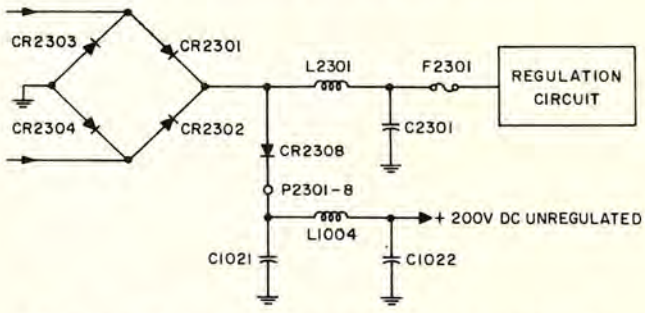


Figure 4-89. Unregulated Power Supply, Simplified Schematic Diagram

center tap at terminal 9 of T2401 is negative with respect to ground potential. Notice that the collectors of Q2401 and Q2403 are at a negative potential since their emitters are returned to ground through limiting resistors R2409 and R2408. Zener diode CR2405 maintains a constant drop of 18 volts because there is conduction through R2401. This stable reference of 18 volts is applied to the emitter of control amplifier Q2402.

Assume that the output voltage rises from +28 volts to +30 volts with respect to ground. This 2-volt rise is reflected on the emitter of Q2402 because there is a constant drop across CR2405. However, the voltage change at the base of Q2402 will be only approximately 1 volt because of the voltage division across R2402, R2405, and R2406. Consequently, the change on the emitter is greater than the change on the base. The net result of this change increases the forward bias from base to emitter of Q2402, and the transistor conducts more heavily. The increased conduction through Q2402-R2407-R2402 causes the drop across R2402-R2407 to become more positive with respect to the collectors of Q2401 and Q2403. As the base voltage on Q2401 and Q2403 moves away from the collector voltage, the transistors begin to cut off and their effective impedance in the circuit starts to increase. This increase in impedance between ground and the center tap of the transformer will drive the center tap (return path) more negative with respect to ground. When the center tap of the transformer goes in a negative direction, the output from the rectifier also goes in a negative direction a corresponding amount. Consequently, the output level is lowered from the high condition of +30 volts to the desired level of +28 volts.

The output level of the regulated portion of the power supply is determined by the adjustment of R2405. Filtering is accomplished by the combination of C2404, C2405, C2406, C2407, and C2408, which are connected in parallel across the rectifier output. Capacitor C2411, between the base and collector of transistor Q2402, provides degenerative feedback to the noise frequencies generated by the silicon diode rectifiers. The regulated output is fused at 1.5 amperes by F2402. Notice that if the fuse is blown, there is no return path for the rectifier; positive voltage is not present on the output line; and voltage is not applied to the regulator portion of the circuit.

The unregulated output is rectified by CR2401 and CR2402, filtered by L2401, C2401, C2402, and C2403, and fused by 1-ampere fuse F2401. While the power supply is energized, diode CR2406 serves as a blocking diode to prevent the output from being applied to the external input line. While the power supply is deenergized, 28 volts from an external source may be supplied through CR2406 to the circuits in the receiver.

p. SERVOMECHANISMS.

(1) MASTER CYCLE AND MASTER ENVELOPE SERVO PACKAGES (A1801, A1901).

(a) GENERAL. – The master servo packages provide mechanical power to turn the master cycle and master envelope 100-kc resolvers. Error signals generated in the detection process are applied to the input of the appropriate master servo package. Physically, the modules each consist of a sealed magnetic amplifier unit, a servomotor, a reduction gearhead, a resolver, and a printed board for mounting the external components. The master envelope servo also has a tach-generator attached to its motor for velocity feedback. The ultimate function of the master servos is to shift the phase of the 100-kc reference signals in response to a d-c input voltage.

(b) DETAIL. - Refer to figure 6-161 or 6-162 for a simplified block diagram of the master servo packages. The magnetic amplifier is actually two amplifiers in a single case as discussed in paragraph 4-2*j*(4). The d-c amplifier portion amplifies the input to drive the servoamplifier portion. The servoamplifier applies 2-phase, 400-cps power to excite the servomotor which rotates the 100-kc resolver through a 1200:1 gear reduction. The servomotor contained in the master envelope servo differs from that contained in the master cycle servo in that it includes a tach-generator. The tach-generator is excited by 10 volts rms at 400 cps from the line polarity coder and provides a 400-cps output voltage that is proportional to the servomotor speed.

Two master servo packages are used in the receiver. In response to a d-c input from the master operational amplifier, the master cycle servo operates in the master 100-kc cycle loop to modify the signal from the receiver local oscillator to produce a signal that is coherent with the received master signal. That is, the 100-kc output from the cycle resolver is phase-locked with the received master signal. In response to a d-c input from the master strobe amplifier, the master envelope servo operates in the master 100-kc envelope loop to produce a signal that is coincident with the received 100-kc master signal. That is, once the master 100-kc signals are in phase lock, the master envelope servo modifies this signal in a time relationship to produce the master timing trigger (MT), which is coincident in time with the leading edge of the received master signal. The output of the tach-generator is fed back to the master strobe amplifier so as to reduce the output of the strobe amplifier. This velocity feedback reduces the speed of response of the master envelope loop and thus provides the filtering necessary for high noise-to-signal inputs.

Notice that a dither excitation is also applied to the servoamplifier. This dither signal has an amplitude that is just enough to overcome the effects of friction and sticking (stiction) in the gearing system. Dither excitation is more fully explained in paragraph 4-2*j*.

(2) SLAVE DELAY SERVO PACKAGE (A2001, A2101).

(a) GENERAL. - Basically, the slave delay servo package produces timing information for the remaining circuits of the receiver. The ultimate product of the slave delay servo is the slave-trigger timing. The slave triggers are directly related to the master trigger since the master trigger is the primary basis for all other timing signals in the receiver. Once the master trigger is established and is coincident with the received master trigger, the timing functions of

the slave-delay servos become significant. The slave-delay readout itself is not significant until the slave triggers become coincident with the received slave triggers. At this time, the receiver is locked in, and the slave-delay readout dials represent the true delay between the received master signal and the slave signals. The slave-delay servo will be discussed in terms of time since the product of the receiver is read out in microseconds of delay. The Loran-C receiver contains two identical slave-delay servo units, one for the X-delay and the other for the Y-delay

See figure 6-163 for the schematic diagram of the slave delay servo package. The inputs to the unit include:

1) Slave integrated cycle error from the operational amplifier.
2) Master 100-kc, 2-phase from the 100-kc driver.
3) Slave derived envelope error from the strobe-amplifier.
4) Master 10-kc, 2-phase from the 10-kc driver.
5) Dither excitation to the cycle and envelope servo amplifiers.
6) Output of the encoder driver.
7) Clutch excitation, +28 volts dc.

Outputs from the slave delay servo include:

1) Binary output to the timing (coincidence detector) circuits.
2) Slave 100-kc to the reference driver.
3) Slave 10-kc to the pulse group timing circuit.
4) Dial readout calibrated in microseconds.
5) Potentiometer readouts from the cycle and envelope for the pen recorder.
6) Tach-generator output.
7) Ambiguity switching.

(b) DETAIL. - See the schematic diagram of the slave-delay servo shown in figure 6-163. The function of the slave-delay servo is to supply timing information to the detector-strobe circuits and code group generator, to read out the slave delay on a mechanical counter calibrated in microseconds, and to provide electrical outputs for an external recorder. The total circuit does not exist as a single module, but it becomes convenient to speak of these associated circuits as a unit. The slave-delay servo module is composed of the rotating components, gearing, and the associated servoamplifiers. The servoamplifiers are magnetic amplifiers which produce the driving voltage for the drive motors from a d-c error input voltage.

The X-slave and Y-slave delay servos are identical, and each is capable of operating throughout the pulse repetition interval. Each slave-delay servo consists of envelope and phase comparison loops that are each closed independently, but are cross-connected mechanically through a summing differential. This cross connection permits the cycle loop, which has a shorter time constant and a 10-microsecond resolving period, to provide a phase lead to the envelope loop during transient conditions.

First, the relationships encountered in the cycle portion of the delay servo should be considered. The cycle drive motor drives the 100-kc resolver and the tenths and units drums of the readout counter. Since the period of the 100-kc signal is equal to 10 microseconds (and one turn of the tenths counter drum is equal to 1 microsecond), these units must be geared in such a way that a time difference of 1 microsecond at the resolver will equal one revolution of the tenths counter drum. It should be noticed that the above relationship holds true from the output of the gearhead which follows the cycle drive motor. For shipboard operation, the gearhead driven by motor B1 is approximately 900/1. This gearhead should be replaced by one that is approximately 90:1 when the receiver is used in an aircraft installation. The extra gearhead is normally stored on the chassis under the selectivity unit. Also, each slave delay servo should have a wire soldered across R3 and R33 in its operational amplifier when the receiver is used in an aircraft installation.

The period of the 10-kc signal is 100 microseconds. Therefore, one thousand revolutions of the 10-kc resolver represent the 100,000-microseconds maximum pulse repetition rate interval. The angular position of the 10-kc resolver is read in microseconds by the mechanical counter and is recorded electrically by the analog-to-digital converter (ADC). Each count in the ADC represents 20 microseconds of delay from the master trigger. Consequently, the 10-kc resolver makes one complete revolution for every five counts of the ADC. This means that as the ADC and 10-kc resolver rotate, the basic slave delay time is established. The output of the ADC (20-microsecond increments) is compared with the master timing information in the pulse rate generator. When these counts coincide, a slave delay trigger is generated.

Next, consider the relationships encountered in the derived envelope portion of the delay servo. The envelope drive motor turns the 10-kc resolver; the tens, hundreds, throusands, and ten-thousands drums of the readout counter; and the ADC. The resolution of the drive system is now based on one revolution of the tens readout drum being equal to 100 microseconds of delay. The ADC unit stores time delay information in the form of binary numbers (time increments of 20 microseconds). The period 10 kc is equal to 100 microseconds. Consequently, the resolution of the envelope portion of the drive system is one-tenth of the resolution of the cycle drive system. Since the envelope loop cannot maintain a fixed speed without phase error, the cycle and envelope drive systems must be connected in such a way that the cycle motor drives the envelope gear train when the time delay is steadily changing. This connection is accomplished in the cycle/envelope differential and allows the envelope motor to operate at zero speed during vehicle motion.

Follow the drive systems from the ambiguity differential. The simplified block diagram shows that one turn of the shaft is equal to 1 microsecond of time delay. The inputs to the differential both equal one revolution for 10 microseconds of delay (1:10). The cycle/envelope differential is driven by the 100:1 gearhead while there is envelope error. The envelope motor comes to rest after envelope error ceases to exist. Its duties are taken up by the cycle portion of

the slave-delay servo through the proper gearhead and through the cycle/envelope differential. This prevents a large envelope error from suddenly appearing and causing loss of lockon in the loop. The display of the exact time delay between the master trigger and the slave trigger will be shown on the dial readout. The timing of the slave trigger depends on the position of the ADC and the position of the 10-kc resolver.

Observe the function of the discrepancy alarm. The speed ratio of the cycle shaft (at the readout counter) to the envelope shaft (at the readout counter) is 1:100. This ratio is reduced to one by the reduction gears that drive the discrepancy differential. If both the cycle shaft and the envelope shaft turn at the proper rate, the output of the discrepancy differential is zero and the discrepancy alarm cam does not turn. However, if there is a discrepancy in the rotation of the cycle and envelope shafts, the discrepancy differential produces an output which turns the discrepancy cam. When a difference of more than 5 microseconds is present, the discrepancy alarm is actuated.

A provision is made for changing the drive speed during the slewing operation. The track clutch is normally closed and the slew clutch is normally open. However, during slewing operation, the slew clutch is closed so that the 10-kc resolver and the ADC will turn at a rate much faster than possible during the tracking process. When the slewing process stops, the track clutch is again closed.

The application of the dither excitation is fully explained in paragraph 4-2*j*(1). The dither oscillator is discussed in paragraph 4-2*j*(5).

q. NOISE GENERATOR (A2601).

(1) GENERAL. - The noise generator is essentially an item of test equipment included with the receiver. Random noise is generated in the board and supplied to the selectivity unit with the antenna signal so that the noise characteristics of the set may be tested.

(2) DETAIL. - Refer to the schematic diagram, figure 6-169. There are four stages to the noise generator: (1) the noise source, (2) an emitter follower, (3) an amplifier, and (4) an output emitter follower. The noise source is a Zener diode which has been selected for its noise characteristics. It is biased at the knee of the breakdown curve. Since each diode is slightly different, variable resistor R2 is provided to perform this function. The noise is coupled to transistor Q1 through capacitor C1. The amplitude is set by resistor R3.

Transistor Q1 is an emitter-follower stage that isolates the noise source from the rest of the circuit. The output from this stage is applied to amplifier stage Q2. The upper cutoff frequency, approximately 350 kc, is determined by the characteristics of Q2. The lower frequency cutoff point, approximately 50 kc, is established by emitter-bypass capacitor C2. Therefore, the operating frequency from 50 to 350 kc is established and amplified for application to final stage Q3.

Transistor Q3 is an emitter follower for isolating the output from the first two stages. Also, the emitter resistor, R10, and resistor R11 establish the output impedance for the circuit at approximately 600 ohms. This is purposely set to be a mismatch with the antenna.

The impedance for the antenna is approximately 50 ohms. Since this circuit does not match the antenna, there is no loading of the antenna signal into the rest of the circuit. Capacitor C3 couples the output to the antenna coupler.

In normal operation, this circuit is not used. For test purposes, a BNC cable and a TEE connector are used so that the antenna and the noise generator may both be connected to the selectivity unit.

4-3. INDICATOR.

a. GENERAL. - The indicator works with the receiver. See figure 4-90 for the block diagram of the indicator. Except for the possibility of application of an external signal at the probe position on the indicator, all signals for the indicator are derived from the receiver. Possible inputs for the vertical circuit of the indicator are: (1) the Loran-C signals generated in the receiver, (2) the signal from the in-phase detector circuit in the receiver, (3) the signal from the agc circuit of the receiver, and (4) any external signal. The horizontal circuit has four possible inputs: (1) the master trigger from the code group generator in the receiver, (2) the X-slave trigger from the code group generator in the receiver, (3) the Y-slave trigger from the code group generator in the receiver, and (4) any external signal applied at the front panel position.

The indicator has the capability of viewing (1) the whole transmitted chain (master and both slaves), (2) the master group and X-slave group, (3) the master group and Y-slave group, (4) a master pulse and X-slave pulse (the modulation within the envelope), and (5) a master pulse and a Y-slave pulse. The sweep generator speeds may be selected to choose any one of the various repetition rates of Loran-C station groups. To operate on the fast speed, the top trace on the scope triggers on the leading edge of a master guard pulse, and the bottom trace triggers on the leading edge of the selected slave guard pulse. When operating on the medium speed, the top trace of the scope triggers on the first guard pulse of the master station group, and the bottom trace of the scope triggers on the first guard pulse of the selected slave station group. The slow traces trigger only on the master station signal. The circuit of the sweep generator corrects for the various sweep speeds that must be selected in order to view the various Loran-C repetition rates.

The sweep signal from the sweep generator is applied to the horizontal deflection amplifiers. There are facilities in this circuit for both horizontal gain and horizontal positioning of the signal. The sweep generator also provides the necessary trace separation signal for the vertical deflection amplifier.

The blank-unblank circuit cuts off the electron beams in the cathode ray tube during the periods of retrace so that these extraneous electrons will not interfere with the normal scope presentations.

The vertical circuit consists of three alternate paths for an applied signal. One is through a selective amplifier and two notch filters. The selective

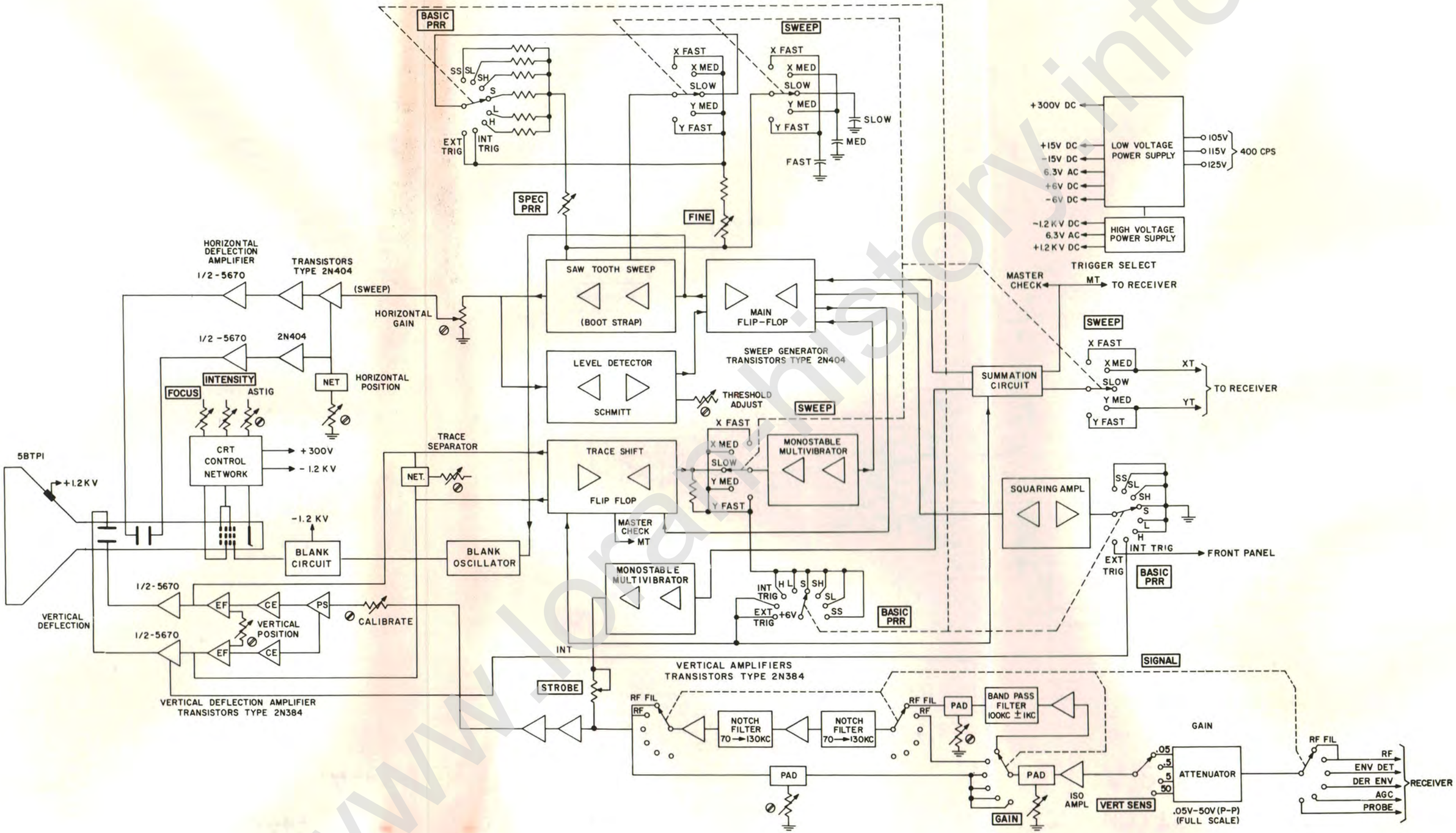


Figure 4-90. Loran Indicator IP-532/SPN-30, Block Diagram

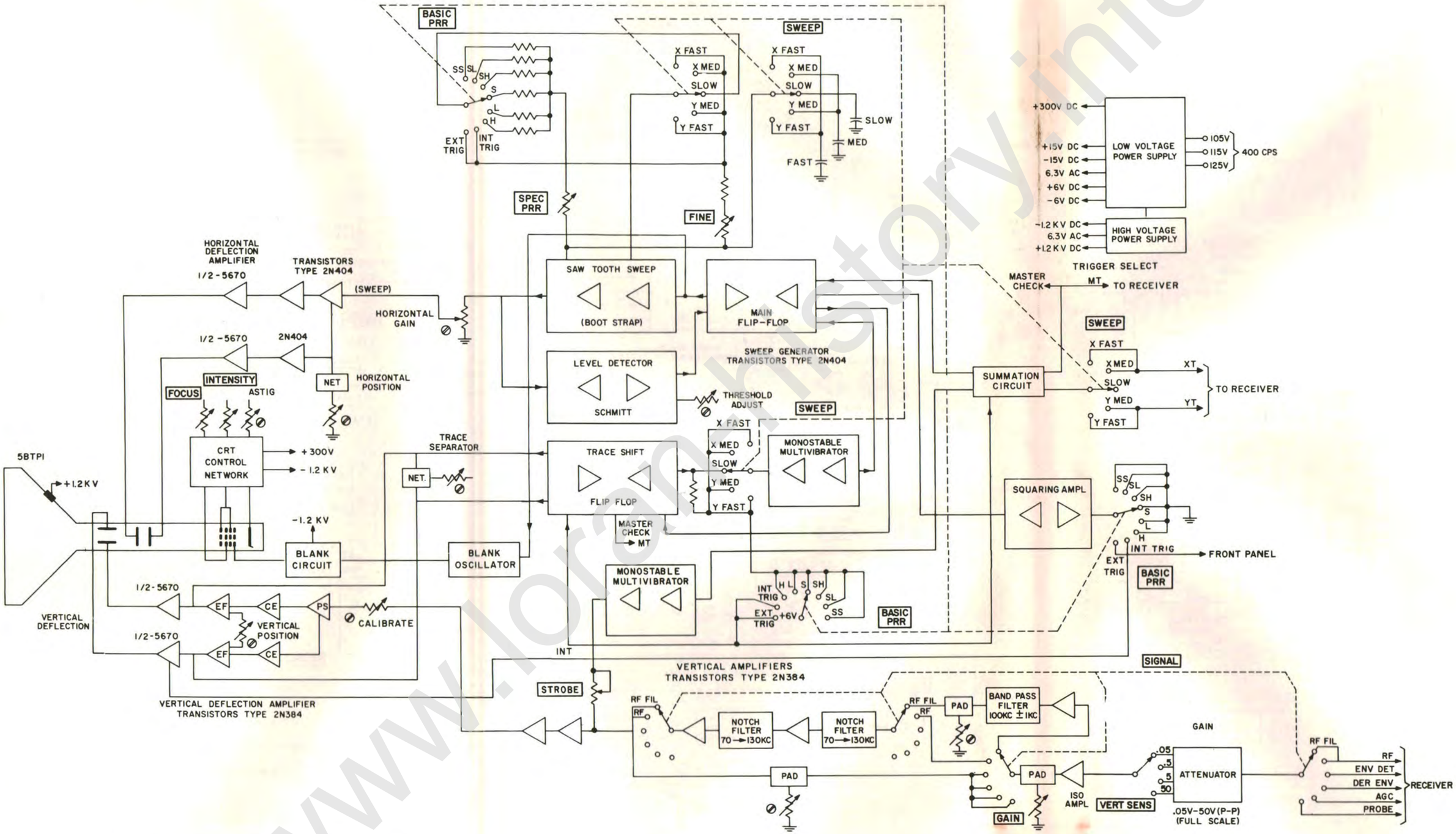


Figure 4-90. Loran Indicator IP-532/SPN-30, Block Diagram

amplifier greatly narrows the bandpass characteristics of the circuit, and the notch filters effectively provide means for attenuating an undesired signal that may be in the area close to the Loran-C signals. Another path bypasses the selective amplifier but includes the two notch filters. The third alternate path applies the input signal around both the selective amplifier (bandpass filter) and the notch filters directly to the vertical amplifier circuit. All three paths include an attenuator path to provide a means of selecting the sensitivity of the scope according to the strength of the applied signal.

Notice that there are means of connecting the indicator so that it may be used for a general purpose oscilloscope by selecting the external connection to both the horizontal and the vertical circuits. But this use is limited to the range of sweep speeds that are available. In addition, the input impedance is only moderately high, approximately 47,000 ohms.

(1) SWITCHES. - There are four multiposition wafer switches on the indicator. These are the SWEEP switch, the BASIC PRR switch, the SIGNAL switch, and the VERT SENS (V/CM) switch. The first two help select the different modes of operation for the horizontal sweep circuit. The SIGNAL switch chooses the input to the vertical circuit, and the VERT SENS (V/CM) switch selects the magnitude of the presented signal on the scope.

(a) SWEEP SWITCH. - The SWEEP switch chooses whether the indicator will operate on a slow, medium, or fast sweep rate. There are five optional positions to which the switch may be set: SLOW, M + X(Y) MED, M + X(Y) FAST, M + Y(Z) MED, and M + Y(Z) FAST. See figure 4-91. When the SLOW position of the switch is chosen, the indicator trace is triggered by the first master trigger pulse from the code group generator in the receiver. The two traces on the scope will be long enough to contain all of the pulse information for a complete group of master, X-slave, Y-slave, and Z-slave pulses (if present). To facilitate this type of operation, one wafer prevents triggers from either of the slave code group outputs from affecting the sweep circuits, only the master trigger being desirable. In any of the other four positions of the switch, the sweep circuit is triggered alternately by a master trigger and by a slave trigger. When one of these modes of operation is chosen, the operator is no longer viewing the whole chain of pulses. The operator is now viewing only the master and one slave group (in a MED position) or the superimposed envelopes of the master and the superimposed envelope of a slave (in a FAST position). If the receiver is operating from the received signals from the X- and Y-slave stations, the M+X(Y) position is used to view the master and the X-slave information. The M + Y(Z) position is used to view the master and the Y-slave information. If the receiver is operating from the received Y-slave and Z-slave stations, then the M + X(Y) position is used to view the master and the Y-slave information; the M + Y(Z) position is used to view the master and the Z-slave information. In each case, all extraneous signals are omitted and hence do not appear on the scope.

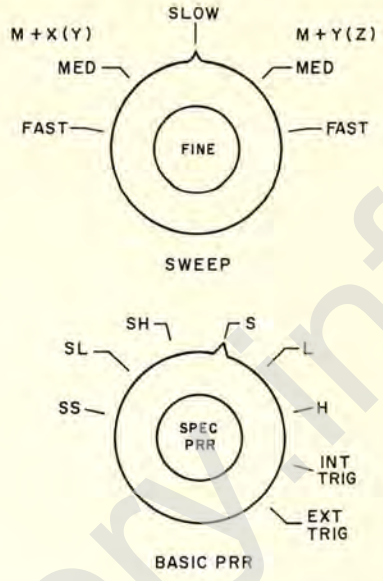


Figure 4-91. Indicator Sweep Controls

For the bootstrap circuit (saw-tooth sweep) to operate properly, there must be a resistor-capacitor combination in the circuit of sufficient time duration to be compatible with the desired sweep rate. See figure 4-89. Two wafers of the SWEEP switch select the proper components. One wafer selects a capacitor (or capacitor combination) for the desired operation, and the other selects the resistor value that determines the charging cycle for the bootstrap. When the SLOW position is chosen, the appropriate capacitor for slow operation is selected by the switch. The other wafer selects a path which includes the selected resistor (by the BASIC PRR switch) and the SPEC PRR control. The maximum utilization of the scope face may be realized by changing the resistor selecting elements.

A variable control is necessary to allow for the difference in the specific pulse-repetition rates within a basic rate. After the adjustments have been set for a particular rate, the SPEC PRR control is not disturbed when the operator switches the SWEEP switch to a MED or a FAST position. The FINE control is inserted in the bootstrap circuit when a MED or a FAST position is chosen by the SWEEP switch. This control is used to vary the sweep length for the trace selected so as not to interfere with the SPEC PRR control. This feature provides a convenience to the operator. If the operator chooses to switch back to the SLOW sweep position after being in another position, the operator may do so without having to readjust a fine adjustment control.

There is a fourth wafer on the SWEEP switch that is used to choose the output from the trace-shift flip-flop to the monostable multivibrator. When the indicator is operating in the SLOW sweep position, the monostable multivibrator is triggered by a pulse from the trace-shift flip-flop in order for it to start the initiating action for the second scope trace. The switch allows the trigger pulse to enter the monostable multivibrator directly. When a MED or FAST

position is selected, a +6-volt bias blocks the output from the trace-shift flip-flop and prevents the monostable multivibrator from triggering, allowing the slave trigger from the receiver to start the second scope trace.

(b) BASIC PRR SWITCH. - The BASIC PRR switch primarily chooses the length of the trace for operation with one of the pulse repetition rates. This switch is also illustrated in figure 4-92. Also, facilities are included for adjusting the sweep length when an internal or external signal is selected. The external signal may be any signal the operator chooses. The internal signal is derived from the vertical deflection amplifier and represents the signal that is applied to the input of the vertical circuit. There are three wafers to the BASIC PRR switch.

The first wafer grounds the input to the squaring amplifier when one of the regular pulse-repetition-rate positions is selected. The input to the sweep circuit may be either master or slave triggers wired directly from the code group generator in the receiver. Therefore, the squaring amplifier input path is disabled by this method. However, if the INT TRIG or EXT TRIG position of the switch is selected, the signal must be shaped so that it will trigger the sweep circuit. The selected input is then allowed to pass through the squaring amplifier to the sweep generator.

The second wafer is part of the sweep-length determining network. When one of the basic pulse repetition rates is selected, the resistor of the proper time-constant value and the SPEC PRR control are inserted in the circuit. The FINE control is selected when the INT TRIG or EXT TRIG position is chosen.

The third wafer ganged on the BASIC PRR switch controls the operation of the trace-shift flip-flop. The center contact of the switch is connected to signal ground, +6 volts d-c. When one of the pulse repetition rates is selected, this +6 volts is applied to the input of the monostable multivibrator to block the output trigger from the trace-shift flip-flop, except when the SWEEP switch is in the SLOW position. The circuit is left unaffected when the SWEEP switch is in the SLOW position. When the BASIC PRR switch is placed in the INT TRIG or EXT TRIG position, +6 volts is applied at two places. One of these is to a diode gate in the trace-shift flip-flop. The bias applied here prevents the master check (master trigger) normally applied to the trace-shift flip-flop from triggering this circuit. The +6 volts is also applied to the summation circuit to prevent the master and slave triggers from affecting the operation of the horizontal sweep circuit.

(c) SIGNAL SWITCH. - The multiple-wafer switch in the vertical circuit selects the input which is to be used for viewing on the cathode ray tube. See figure 4-93 for a diagram of this switch. The optional inputs are the r-f input from r-f amplifier in the receiver, the in-phase (envelope) detector output in the receiver, the derived envelope from the

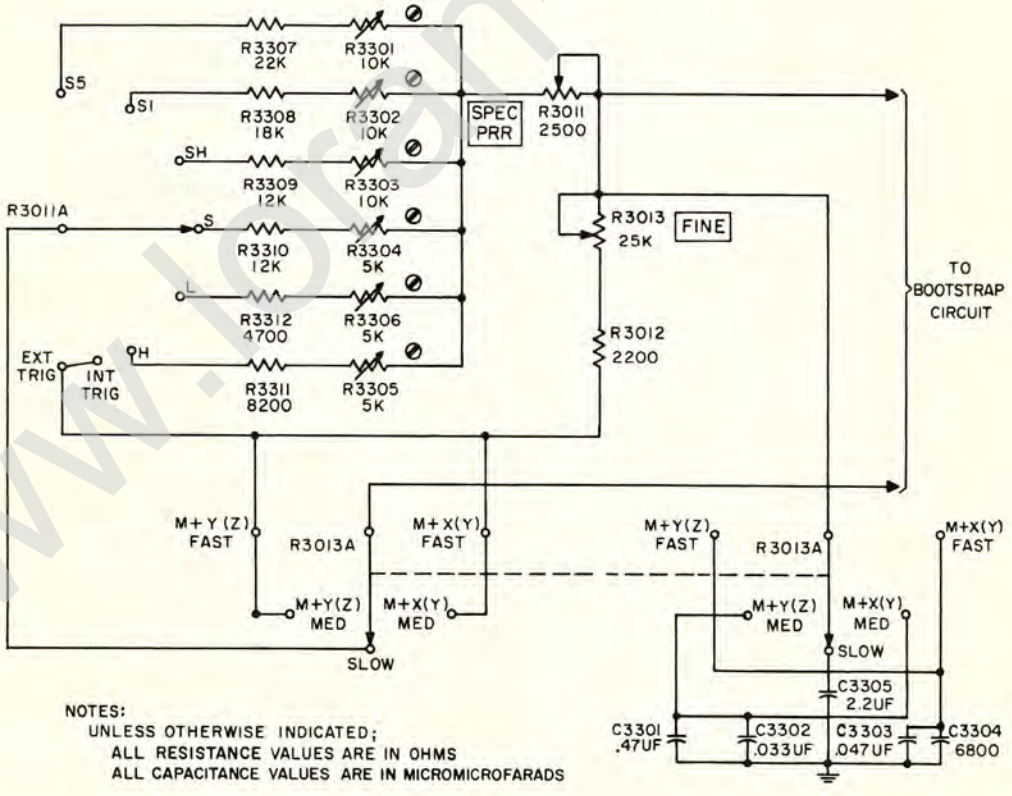


Figure 4-92. Resistance and Capacitance Selecting Network, Bootstrap Circuit

envelope deriver, the agc signal in the receiver, and any signal the operator selects to be applied to the PROBE position.

One wafer selects the input. The second chooses a path which bypasses the filtering system when any internally generated receiver signal is selected. The second and third wafers choose the input and the output of the bandpass filter when the RF FIL position is chosen. The bandpass filter is bypassed when the RF position is selected. The fourth wafer applies the output signal from the notch filters to the vertical amplifiers when either the RF or the RF FIL position is chosen. If one of the other positions is selected, the signal bypasses the filters and is applied straight through from the isolation amplifier. The overall gain control and the individual path gain controls can be used to equalize the various paths so that the operator will not have to readjust when moving from one type of input to another. Both notch filters operate over a frequency range from 70 to 130 kc and may be adjusted independently by the control knobs to eliminate strong, unwanted signals close to the Loran-C operating frequency. See figure 4-94.

The STROBE control, which is concentric with the SIGNAL control, allows the operator to observe the strobe point on the waveforms. The magnitude of the strobe point is variable from being hardly discernible to being quite large so that it may be set to any convenient level by the operator.

(d) VERT SENS (V/CM) SWITCH. - The VERT SENS (V/CM) control selects the correct amplification of the applied signal for proper viewing of the various scope presentations. As shown in figure 4-95, the scale is marked in volts per centimeter. If the operator chooses, he may vary the amplification to a greater degree between the detent positions on the large knob by turning the small concentric

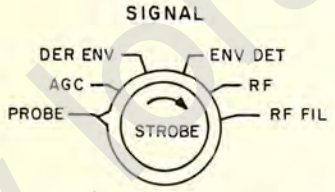


Figure 4-93. Input Signal Switch

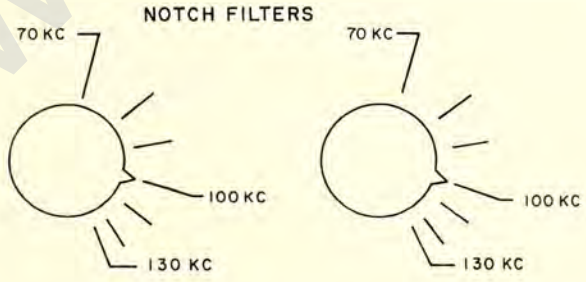


Figure 4-94. Notch Filter Control Knobs

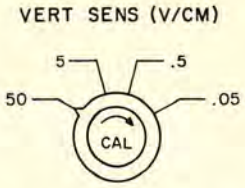


Figure 4-95. Vertical Sensitivity Switch

CAL knob. However, the calibrations on the VERT SENS (V/CM) dial will be correct only when the CAL knob is turned fully clockwise.

b. HORIZONTAL CIRCUIT. - The horizontal circuit is composed of an input summation network, the sweep generator, and the horizontal deflection amplifier. The summation network selects the signal to be applied to the horizontal portion of the indicator circuit. The sweep circuit determines the duration and magnitude of the horizontal signal. The horizontal deflection amplifier prepares the signal to be applied to the horizontal deflection plates of the cathode ray tube.

The signal applied through the summation circuit to the sweep generator is normally a master pulse from the code group generator in the receiver alternating with a slave pulse from the code group generator. When the master signal is applied to the main flip-flop, it changes state and initiates the sweep in the bootstrap. The time length for the sweep is selectable by an internal potentiometer. The output of the bootstrap is fed back to the Schmitt level detector, which triggers when a predetermined level is reached. The level detector output is returned to the main flip-flop. The flip-flop changes state again and cuts off the signal applied to the bootstrap. The outgoing signal from the bootstrap is applied to the horizontal deflection amplifier and from there to the horizontal deflection plates of the cathode ray tube.

(1) SUMMATION CIRCUIT. - The summation circuit, figure 4-96, is comprised of a group of diodes connected as a gate that blocks signals or allows signals to pass to the sweep generator. The signals applied to the summation network are the indicator master trigger (INT), an indicator slave trigger (either IXT or IYT, as selected by the sweep selector switch), and a +6-volt bias (in the INT TRIG or EXT TRIG position of the basic switch). The gate operation is controlled by the proper biasing of the diodes. When the cathode of a diode is more positive than its anode, the diode will be cut off and a signal will not be relayed to the remainder of the network. A -6-volt bias is constantly applied to the common cathode side of the network through a high value resistor. Both the master trigger and the selected slave trigger are -6- to 0-volt pulses. Between pulses, the normal levels at the inputs to the summation circuit are -6 volts. If the diodes were perfect, -6 volts at all diode anodes would establish the common cathode point at a level of -6 volts. Therefore, any selected positive-going trigger (0 volt) will pass when the cathode is at -6 volts. Also, when a trigger

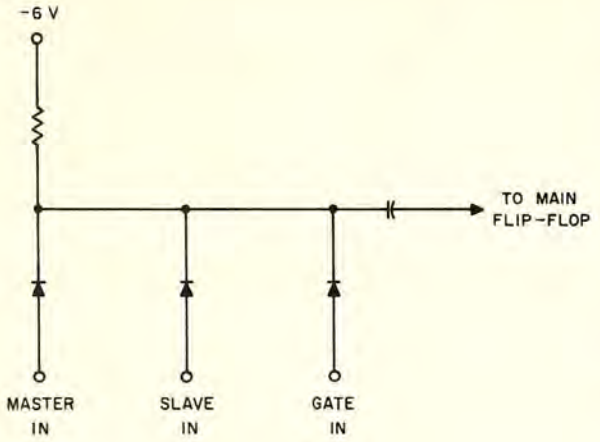


Figure 4-96. Summation Circuit, Simplified Schematic Diagram

is passed, the common cathode connection becomes 0 volt. This is more positive than the applied signal to any other anode and prevents feedback into the receiver along another path. An example of this is the prevention of a master pulse from re-entering the receiver along a slave trigger route.

If either the INT TRIG or EXT TRIG position of the basic switch is selected, +6 volts will be applied to the common cathode connection through a diode (GATE IN on the diagram). This is a more positive voltage than 0 volt, the most positive trigger signal to the anode of any diode. Therefore, all trigger signals are prevented from affecting the sweep circuit.

(2) SWEEP GENERATOR. - The sweep generator circuit consists of the following network: the main flip-flop, the bootstrap sweep circuit, the Schmitt level detector, the trace-shift flip-flop, and the monostable multivibrator. See the block diagram of figure 4-90, and the schematic diagram of figure 4-97. Under normal operation, when the BASIC PRR switch is set to the SS, SH, SL, S, H, or L position, the signal applied to the sweep generator consists of a master pulse from the code group generator in the receiver alternating with a slave pulse from the code group generator. When the master signal is applied to the main flip-flop, it changes state and initiates the sweep in the bootstrap. The time length for the sweep is selectable by an internal potentiometer. The output of the bootstrap is applied to the horizontal deflection plates of the cathode ray tube. It is also applied back to the Schmitt level detector, which triggers when a predetermined level is reached. The level detector output is returned to the main flip-flop. The flip-flop changes state again and cuts off the signal applied to the bootstrap.

The main flip-flop, in addition to triggering the bootstrap, also triggers the trace-shift flip-flop. The start of the trace from the circuit is established on the top line of the trace on the cathode ray tube by a master pulse applied directly from the code group generator in the receiver. When the signal is applied from the main flip-flop, the trace-shift flip-flop changes state and causes the top trace to begin. When the main flip-flop again changes state, the lower trace is initiated.

The monostable multivibrator is used for any of the slow speeds. It derives its triggering signal from the trace-shift flip-flop. When operating on any of the slow speeds, the sweep circuit triggers only on the main station pulses from the receiver. Therefore, it is necessary to begin the lower trace at a given delay time after the completion of the top trace. The monostable multivibrator is triggered by the pulse from the trace-shift flip-flop. After the desired time delay, the monostable multivibrator returns to its original state and triggers the main flip-flop.

The squaring amplifier is independent of the sweep-generator circuit in the normal operation. However, it does function when either an external or internal signal is used to trigger the sweep circuit. The squaring amplifier produces sharply spiked trigger signals suitable for initiating sweep action from an irregular input waveform, when it becomes greater than a certain magnitude.

(a) MAIN FLIP-FLOP.

1. GENERAL. - The main flip-flop functions essentially as a 2-position toggle switch which is stable in either position. The primary function of the main flip-flop is to initiate a starting trigger for the saw-tooth sweep circuit at the proper time. One state of the flip-flop starts this sweep and prevents any outside signals from disturbing the sweep until it is complete. The other state cuts off the saw-tooth sweep input and is a reset position in preparation for initiating the sweep again. Because it can operate in this manner, the circuit is referred to as either being ON or OFF. When the circuit is turned ON, it initiates (1) the pulse to start the bootstrap circuit, (2) the pulse for triggering the trace-shift flip-flop, and (3) the bias necessary to cut off input signals applied to the diode switch. In turn, the main flip-flop may be turned on by a trigger (1) from the summation circuit, (2) from the monostable multivibrator that starts another sweep trace in lieu of a trigger from the summation circuit when a SLOW position is chosen by the SWEEP switch, and (3) from the squaring amplifier through the diode switch to start the sweep action when an external or internal signal is used. The only means that is used to cut off the main flip-flop is a trigger from the Schmitt level detector. During the bootstrap sweep time no other signal can be applied. When the trace is completed, the level detector will reset or turn the main flip-flop off so that another trigger will be able to initiate, or turn on, the main flip-flop and start a new trace.

See figure 4-98 for the schematic diagram of the flip-flop circuit. The flip-flop circuits in the Loran-C indicator are essentially the same as the toggle circuits in the receiver. A detailed circuit analysis appears in paragraph 4-2*d*(1). As a quick guide to the operation of the circuit, it should be remembered that the outputs of the circuit are mainly determined by two design features: pulse steering and pulse shaping.

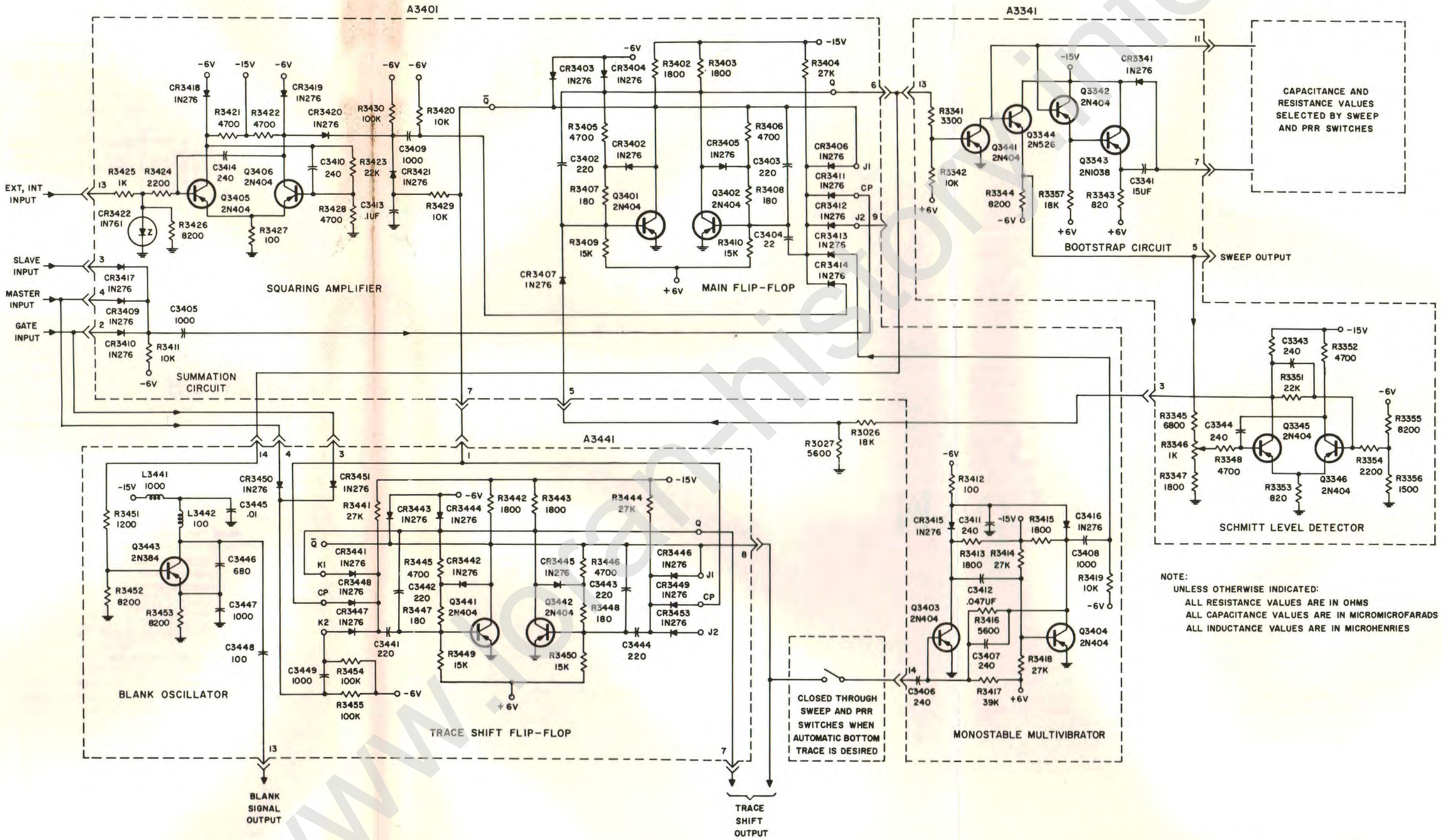


Figure 4-97. Sweep Generator, Functional Schematic Diagram

2. PULSE STEERING. - Pulse steering is used to assure bistable operation of the flip-flop. Connections are made between the Q output and the K1 input and between the $\overline{Q}$ output and the J1 input. When positive-going inputs are applied to both CP's at the same time, the following series of events takes place.

Q1 is conducting; $\overline{Q}$ output is 0 volt.
Q2 is cut off; Q output is -6 volts.
Inputs are applied and both transistors switch.
Positive-going Q output adds to the positive-going input at terminal 3.
Negative-going $\overline{Q}$ output inhibits the positive-going input at terminal 9.
Only Q1 feels a change at its base as a result.

3. PULSE SHAPING. - Capacitors C2 and C3 are incorporated in the base circuits of Q1 and Q2. The function of C2 and C3 is to accelerate the switching time of the circuit and to effectively steepen the rise time of the square-wave outputs at Q and $\overline{Q}$.

4. APPLICATION. - The flip-flop circuit in figure 4-98 is representative of both the main flip-flop and the trace-shift flip-flop, which function almost identically. A cross reference of the numbers used in the general flip-flop circuit of the figure and the main and trace-shift flip-flop appear in table 4-7.

TABLE 4-7. COMPONENT FLIP-FLOP CROSS REFERENCE

GENERAL	MAIN	TRACE-SHIFT
C1	*	C3141
C2	C3402	C3142
C3	C3403	C3143
C4	C3404	C3144
CR1	*	CR3441
CR2	CR3402	CR3442
CR3	CR3403	CR3443
CR4	CR3404	CR3444
CR5	CR3405	CR3445
CR6	CR3406	CR3446
CR7	CR3407	CR3452
CR8	*	CR3448
CR9	CR3411	CR3449
CR10	CR3413	CR3453
Q1	Q3401	Q3441
Q2	Q3402	Q3442
R1	*	R3441
R2	R3402	R3442
R3	R3403	R3443
R4	R3404	R3444
R5	R3405	R3445
R6	R3506	R3446
R7	R3507	R3447
R8	R3508	R3448
R9	R3509	R3449
R10	R3510	R3450

*Not used in Main Flip-Flop

In operation the main flip-flop is triggered from a number of sources discussed in detail in paragraph 4-3*b*(3) and shown in simplified schematic diagram form by figure 4-107. The trigger input to transistor Q3401 comes from the Schmitt level detector output through CR3407 and is directly coupled to the base of Q3401. Trigger inputs to transistor Q3402 are capacitively coupled to the base.

The Q output from the main flip-flop gates the blanking oscillator and the bootstrap sweep circuit; the $\overline{Q}$ output is the clock pulse for the trace shift flip-flop.

The Q output (from the collector of transistor Q2) is used to trigger the bootstrap circuit and the blank-unblank circuit. The $\overline{Q}$ output (from the collector of transistor Q1) establishes the clock pulse of the trace-shift flip-flop.

(b) BOOTSTRAP CIRCUIT. - The input to the bootstrap is a square wave with alternate voltages of 0 and -6 volts. See the simplified diagram of figure 4-99. The 1800-ohm resistor R1 and the 10,000-ohm resistor R2 form a voltage divider network. A total of 6 volts will be applied across the entire combination when a zero voltage is applied to the circuit. The voltage across R1 will be some small positive fraction of this total voltage. This small positive voltage is applied to transistor Q1. The total drop will be 12 volts across the entire combination when -6 volts is applied to the circuit. Some small negative voltage will be applied to Q1 since R1 is near the negative end. A negative voltage applied to the base of PNP transistor Q1 will bias it in the forward direction.

Transistor Q1 will switch on. The resistance of the transistor is quite small during the conducting cycle and any charge built up on the panel capacitance selected by the SWEEP switch will discharge. The output of the bootstrap circuit will also return to 0 volt since it is connected at this point.

Transistor Q1 switches off when a level of 0 volt is applied to the voltage divider and the charging cycle of this circuit occurs. The negative voltage applied to the selected resistance will begin to build a negative charge on the selected capacitor. The negative charge will be passed to transistor Q3 of the diagram. There is no phase reversal in this transistor since it is connected as an emitter follower. The transistor has been conducting because of the positive bias applied to its emitter, but now the conduction increases. The gain through the transistor is roughly unity. Negative voltage is applied to C2. The voltage across C2 is approximately constant, so that the output also becomes more negative. This negative voltage cuts off diode CR1 by making its anode more negative than its cathode. A more negative voltage applied to

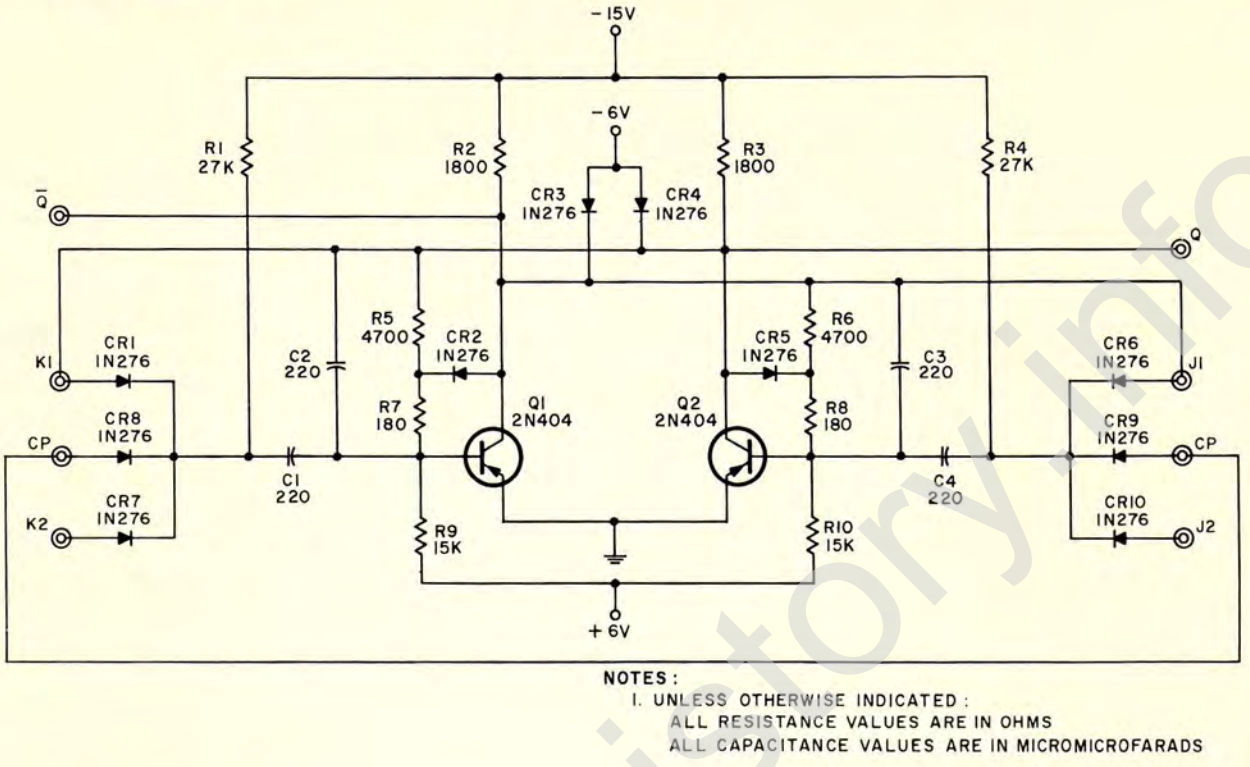


Figure 4-98. Standard Flip-Flop, Schematic Diagram

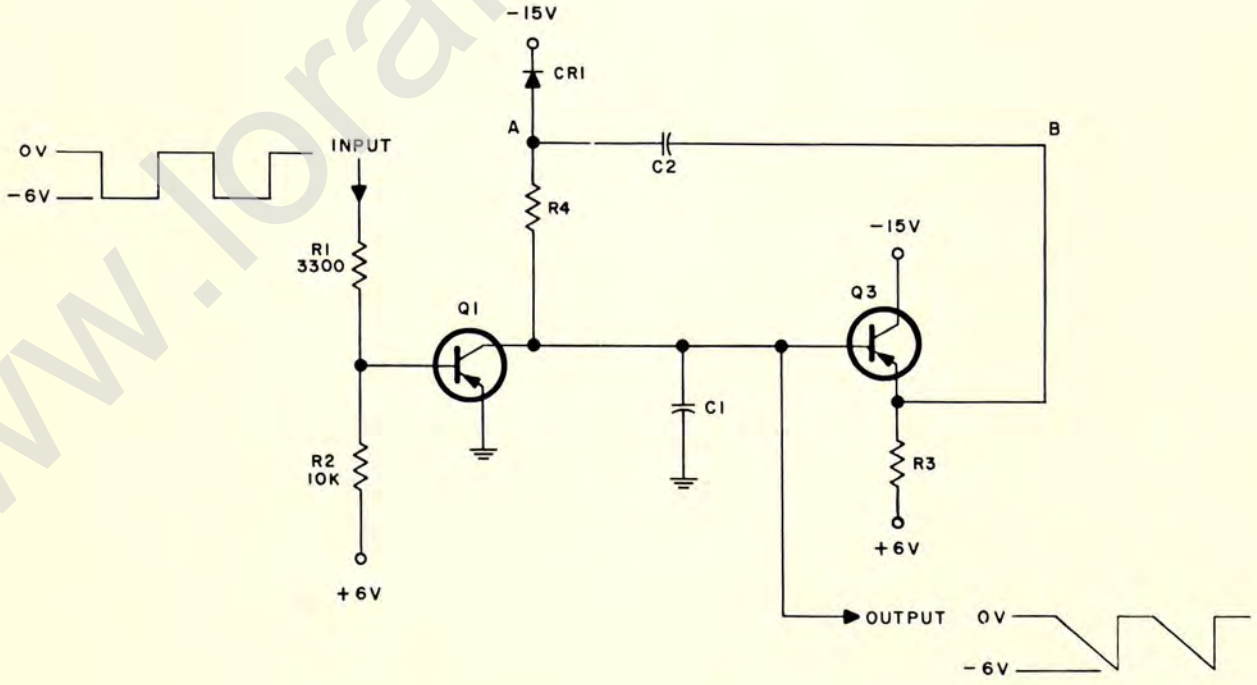


Figure 4-99. Bootstrap Circuit, Simplified Schematic Diagram

the selected resistance will increase the negative charge on the selected capacitance, the voltage across the selected resistance remaining constant. The charge on the selected capacitance will start the cycle over again.

The limiting factors in the simplified drawing are the maintenance of the charge on C1 and the shape of the charging curve of the selected capacitance. The size of resistor R3 determines how quickly the charge on C1 builds up. This is important because of the following reasons. Capacitor C2 quickly discharges when Q1 switches on due to its input. In fact, Q1 conducts so rapidly that for a short time the base of Q3 is positive with respect to the emitter, cutting off the transistor. Now, C1 attempts to discharge. The base of Q3 will become negative again (because of the applied negative voltage to the input) and again build up a charge on C1. This short lapse of time is the limiting factor for the time between traces. The charging time of C1 depends on the size of R3. However, resistor R3 cannot be made too small because it is across the selected capacitance while it is charging. If it were small, the charge on the selected capacitance would quickly roll off (exponentially) and the resulting trace would not resemble a straight line and it would not reach a very high value. A Darlington pair has therefore been inserted in the circuit at Q3342 (figure 4-100). It does not change the size of the resistance appearing to C1 (C3441 in the actual circuit), maintaining it at a small value. However, it does effectively increase the impedance to the capacitance selected by the SWEEP switch by a multiplying factor of the beta of Q3343.

The output of the circuit could be taken from the emitter of Q3343, point B in the simplified circuit. This is disadvantageous because the slight tendency for C1 (C3341 in the actual circuit) to discharge is reflected at this point. To avoid this, another transistor-resistor combination is inserted at the base of Q3 (Q3342 in the actual circuit). The 8200-ohm resistor, R3344, provides a high output impedance for the circuit. The impedance presented to the selected capacitance is equal to β Q3342 β Q3343 R3343. Therefore, the transistor acts as a very good isolator, leaving the original bootstrap circuit relatively unaffected. The output wave from the circuit is a very smooth saw-tooth shape output.

The length of the trace is determined by the size of the selected resistance and capacitance. One wafer of the SWEEP switch effectively selects the appropriate resistance path for the FAST, MED, and SLOW positions; and another wafer of this same switch selects the appropriate capacitance value. Variable resistors are included in the path so that an increment of a resistance value may be selected.

Figure 4-89 shows the resistance and capacitance selecting network which determines the sweep-charging time for the bootstrap circuit. There are two wafers of the SWEEP switch and one wafer of the BASIC PRR switch involved in the proper component selection.

The capacitance selection is relatively simple. The SWEEP switch is used to select one of the three possible capacitor combinations and applies the selected value directly between terminal 11 of printed circuit

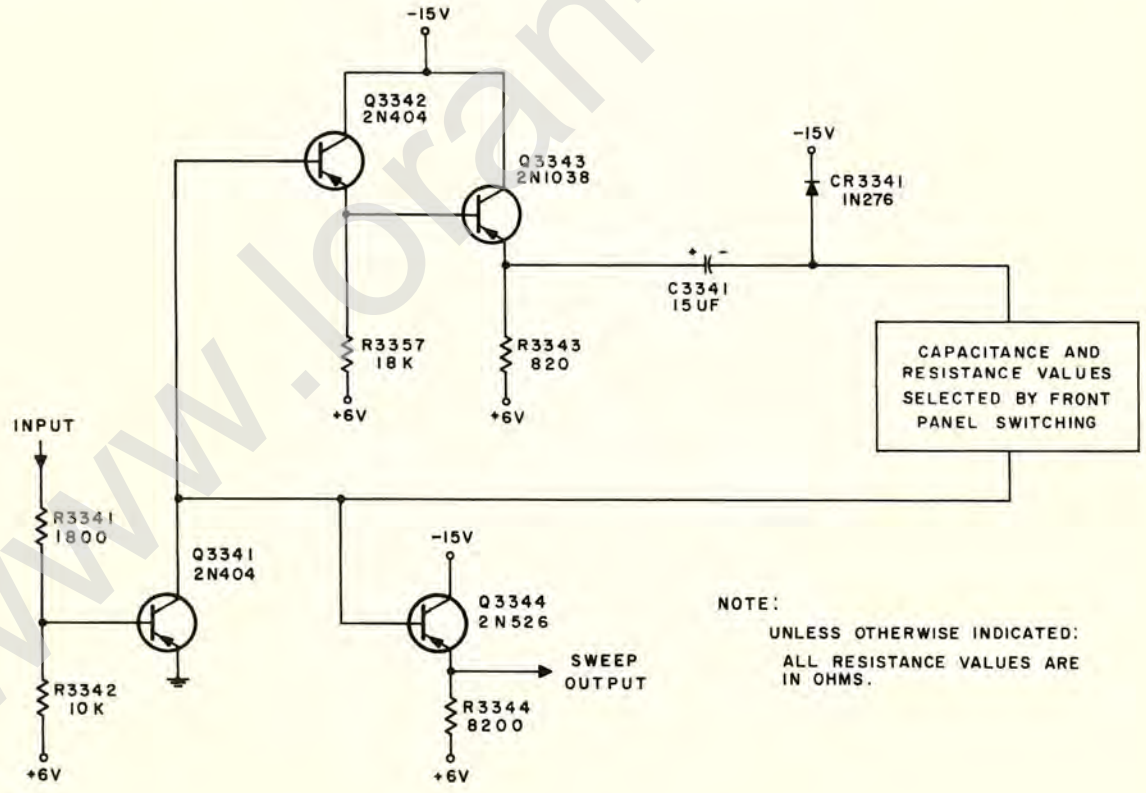


Figure 4-100. Bootstrap Circuit, Schematic Diagram

board A3341 and ground, independent of the BASIC PRR switch position. See the printed circuit connections shown in figure 4-101.

The resistance selection is a little more complicated. There are two types of positions that may be selected by the SWEEP switch. These are (1) any of the individual pulse-repetition-gate positions (SS, SL, SH, S, L, or H) and (2) one of the trigger positions (INT TRIG or EXT TRIG). When one of the first positions is chosen, the time for the sweep at the chosen pulse repetition rate is dependent on the duration of the pulses for a transmitted Loran-C station group. The time length for such a chain is known, so preselected resistors may be selected for each of these six switch positions. Actually, each of the six possible positions will choose a fixed resistor-variable resistor combination. The variable resistor is a trimmer adjustment for setting the combination to be compatible with the capacitors used. Such a device is needed to allow for the difference of resistance and capacitance component values within tolerances.

The complete resistance path for the circuit is between terminal 7 and terminal 11 of board A3341 at all times. See sheet 2 of the indicator overall schematic, figure 6-183. The path always includes terminal 9 of one wafer on the SWEEP switch. The path will also pass through terminal 6 when operating in the SLOW position. From there, the path goes through terminal 12 of the wafer used on the BASIC PRR switch and the selected resistor for the basic pulse repetition rate chosen. The path also includes SPEC PRR control potentiometer R3011. This control is used to adjust for variations of resistance values needed to make the proper length trace for the various specific pulse repetition rates within a basic group.

If a FAST or MED position of the SWEEP control is chosen, the path is through terminals 7, 8, 10, or 11 (which are all tied together) on the SWEEP control, resistor R3012, and FINE potentiometer R3013. The FINE adjustment can be used to vary the sweep to any desired amount without interfering with the SPEC PRR control. After the SPEC PRR control has been set, the operator can move the SWEEP switch from the SLOW position to some other position without having to worry about readjusting the SPEC PRR control.

The FINE control and fixed resistor R3012 are inserted in the circuit again if the INT TRIG or EXT TRIG positions of the BASIC PRR switch are selected. There will always be a closing path to terminal 7 of board A3341 regardless of the position of the SWEEP switch, which is now ineffective.

(c) LEVEL DETECTOR. - The basic circuit for the Schmitt trigger level detector appears in figure 4-102. The circuit accepts a sweep signal from the bootstrap circuit which is a linear, negative-sloping pulse. When this signal reaches a predetermined magnitude, a pulse will be generated and applied to the main flip-flop. Before sweep is initiated, the condition of the circuit is as follows. Transistor Q2 is conducting because it has a slight negative bias applied to its base at R1. Resistor R7 establishes the return path to ground. The input to Q1 is 0 volt, hence, the voltage applied to the base of Q1 is also 0 volt. Transistor Q1 will not conduct without a negative bias.

As the voltage at R5 starts becoming negative with the applied voltage, current passing through R7 is drawn away from Q2 and now passes through Q1. When the conduction through Q1 reaches a stage where it is greater than the conduction through Q2, because of the negative voltage increase at the input, all of the current through R7 will tend to take the easiest path and pass through Q1. This action eventually causes transistor Q2 to stop conducting. The voltage at the emitter has become too negative with respect to the base to sustain conduction.

This changing of conduction from Q2 to Q1, as described above, takes an appreciable amount of time. A voltage divider consisting of R1 and R2 accelerates this action. As Q1 starts to conduct, the collector voltage will change from its initial value of -15 volts (when Q1 was cut off) to a more positive value. This is reflected by R2 at the base of Q2. Hence, not only is the emitter of Q2 becoming more negative, but the base is becoming more positive. This cuts Q2 off almost instantaneously. A positive pulse is obtained at the collector whenever this occurs.

In the actual circuit as shown in figure 4-103, a capacitor is paralleled with resistor R3351 (R2 in the simplified circuit). This capacitor operates on the fast rise time of the leading edge of the pulse from the collector of Q3345 and accelerates cutoff even more. Another component that aids this cutoff time is the capacitor between the collector of Q3346 and the base of Q3345. This capacitor provides a return path to the base of Q3345 for the leading edge of the negative-going pulse on the collector of Q3346. The resulting effect is that Q3345 is biased more heavily than if it depended on the input bias alone. Therefore, Q3345 conducts more rapidly and decreases the time for switchover from one transistor to the other. The output of the circuit is derived from the fast rising current through Q3345 when it conducts on each cycle.

Transistor Q3346 is biased so that it conducts again when the input to the circuit returns to 0 volt. Transistor Q3345 is returned to cutoff to await another sweep pulse from the bootstrap circuit.

The exact operating level of this circuit (the point where conduction of Q3345 cuts off Q3346) is adjustable by potentiometer R3346 in the input. This resistor merely changes the voltage divider ratio and causes the circuit to operate on a higher or lower input bias current.

Output from the collector circuit of transistor Q3345 is connected across a voltage divider (R3026/R3027) the opposite end of which is connected to +6 volts. In this way approximately one fourth of the algebraic difference between the voltage at the collector of Q3345 and +6 volts is applied to the reset input of the main flip-flop (the base of Q3401). Actually, as the collector voltage of Q3345 changes from about -15 volts to about 0 volt, the input to the main flip-flop changes from about +1 volt to +4.5 volts.

(d) TRACE-SHIFT FLIP-FLOP. - The trace shift flip-flop operates primarily to change the voltage on the vertical deflection plates so that the cathode ray tube trace will be on two separated lines. That is, no two consecutive traces will be at the same vertical deflection potential. By sweeping two complete and separate traces on the face of the cathode

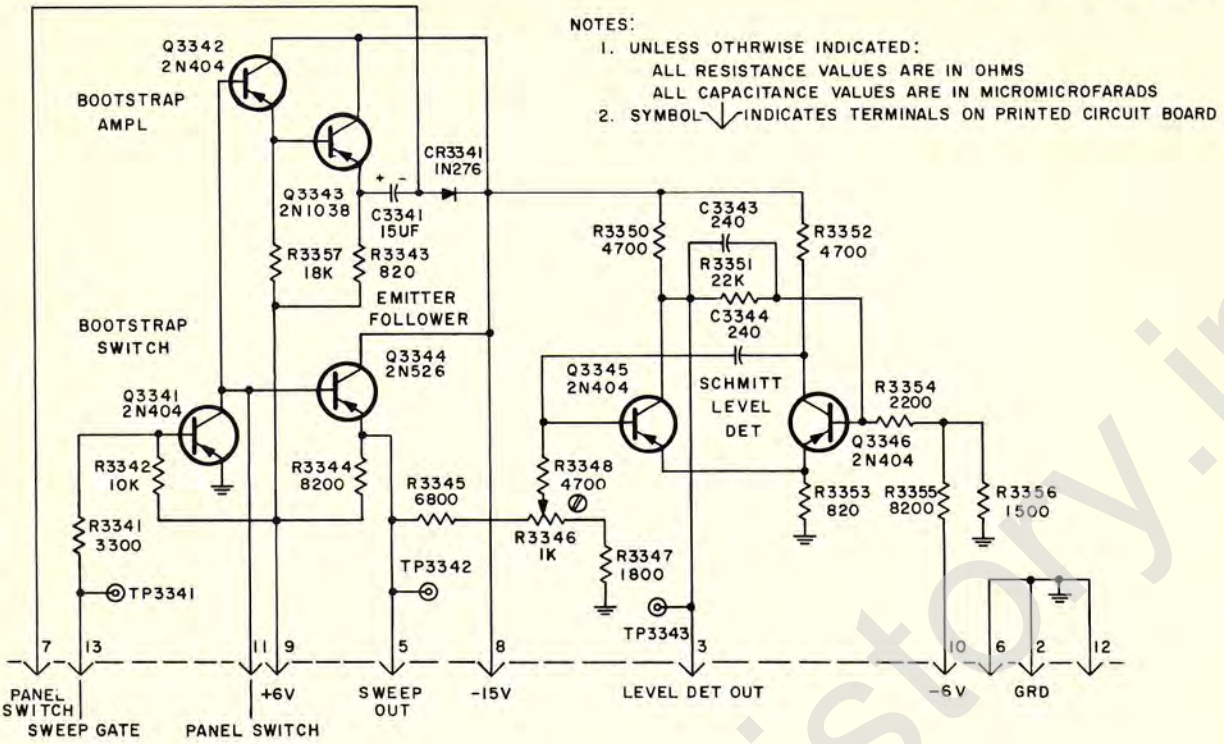


Figure 4-101. Sweep Generator SA2, Schematic Diagram

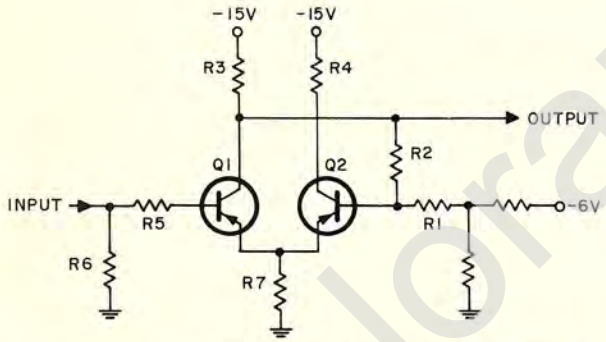


Figure 4-102. Schmitt Level Detector, Simplified Schematic Diagram

ray tube, more face area can be utilized than if only one trace were used. Because of the various modes of operation of the indicator, it is necessary that several input pulses be able to perform the trace-shift operation. Regardless of the mode of operation, the trace-shift will always receive a clock pulse from the main flip-flop when one trace has been completed. This causes the next trace to be in the alternate position, either top or bottom.

If no other provisions for switching were included, the cathode ray tube could be left in a state that would cause the first trace containing the master trigger information to be displayed on the bottom line and the second trace containing the slave information to be displayed on the top line. To prevent this undesirable condition, the master trigger is applied to the reset circuit of the trace shift flip-flop. In this way the trace-shift flip-flop will always cause the top line to be displayed immediately after the master trigger is applied. The only exception to this occurs when the BASIC PRR switch is on either the INT TRIG or the EXT TRIG position. In this case, +15 volts is applied through R3023 to gating diode CR3451 to inhibit the master trigger. If the trace-shift flip-flop is in the proper state for the top line display when the master trigger is applied, the trigger will have no effect.

The trace-shift flip-flop also provides an output to the monostable multivibrator as well as the trace-shift signals to the cathode ray tube. In the SLOW position of the SWEEP switch, the only receiver trigger being received by the main flip-flop is the indicator master trigger. In order to start the flip-flop for the second trace, the monostable multivibrator is triggered by trace-shift flip-flop output Q, which, in turn, changes the main flip-flop. In a MED or a FAST position of the SWEEP switch, both a master and a slave (either X, Y, or Z) trigger are applied to the main flip-flop, one to start the top trace and one to start the bottom trace. Therefore, if one of these positions is selected, trace-shift output Q to the monostable multivibrator is effectively cut off by a constantly applied +6-volt bias.

For a description of the flip-flop action, see paragraph 4-2*d*(1).

(e) MONOSTABLE MULTIVIBRATOR. - The monostable multivibrator operates on a negative

change of state from the trace-shift flip-flop and produces a negative output for a short period of time before returning to its stable output near 0 volt. The monostable multivibrator receives an input pulse from the trace-shift flip-flop only when the SWEEP switch is in the SLOW position. when the SWEEP switch is in any of the other four positions and the BASIC PRR switch is in one of the six pulse repetition-rate positions, a +6-volt level is applied to the input of the circuit and blocks the output from the trace shift flip-flop. The +6 volts is removed from the input of the monostable multivibrator when the BASIC PRR switch is in the INT TRIG or EXT TRIG position and there is an input to the monostable multivibrator from the trace-shift flip-flop regardless of the SWEEP switch position. The output trig gers the main flip-flop so that it will always be ready to be activated by a master trigger from the receiver.

The schematic diagram for the monostable multivibrator appears in figure 4-104. Pulses which are sharply peaked but of short duration are produced from the input square wave by the input capacitor and are applied to Q3403. This is true because the capacitor charges after a very short period of time.

Transistor Q3404 conducts while the input to the circuit is zero since a negative voltage is on both the collector and the base. The zero input voltage applied to the base of Q3403 also keeps Q3403 from conducting. This is the stable condition of the circuit. A negative pulse applied to Q3403 will cause Q3403 to conduct and instantaneously reduce its collector voltage. The voltage across capacitor C3412 will instantaneously remain constant and cause the base of Q3404 to become positive. This will cut off transistor Q3404. When Q3404 is cutoff, its collector decreases to a value of -15 volts. This negative voltage is returned to the base of Q3403 through resistor R3416, accelerating the switching action from Q3404 to Q3403. The switching action is further accelerated by the 240-micromicrofarad capacitor C3407, which operates on the leading edge of the return pulse.

The two diodes limit the maximum voltage swings to -6 volts at the points where they are inserted in the circuit. This is the operating value for the various circuits in the system. The response time is increased since it takes less time to reach -6 volts from 0 volt than it takes to reach some greater negative value. The output circuit consists of capacitor C3408 and resistor R3419. These components shape the output wave so that it will be the desirable square wave operating from 0 to -6 volts.

Almost instantaneously after switchover, Q3403 is conducting. Capacitor C3412 will discharge exponentially until the potential on the base of Q3403 is at the proper value to cause Q3404 to conduct. The time of this discharge cycle sets the duration of the output signal from the circuit. When Q3404 conducts, the collector of Q3404 increases. Transistor Q3403 is cut off since this increasing voltage is applied to its base. The stable conditions that were present before the initial incoming negative pulse was applied are again present.

A positive input pulse will not affect the circuit. A positive pulse only causes the base of Q3403 to become more positive, which is already the condition of cutoff.

(3) SQUARING AMPLIFIER. - There are several optional inputs that may be selected by the BASIC PRR switch. These are the master and slave triggers from the pulse rate generator in the receiver, the internal signal from the vertical deflection circuit, or any external gating pulse that the operator may choose to apply. The indicator normally operates on one of the basic pulse rate trigger signals. When either the SS, SL, SH, S, L, or H position is selected, the horizontal circuit is triggered by the leading edge of the first trigger of a group of code triggers. The triggers will stop being applied to the circuit before the sweep is completed. After the sweep is completed, the first trigger of a new group will then start the sweep again. With external or internal triggering, there is no guarantee that a trigger will not occur at the exact time the sweep is recovering. If

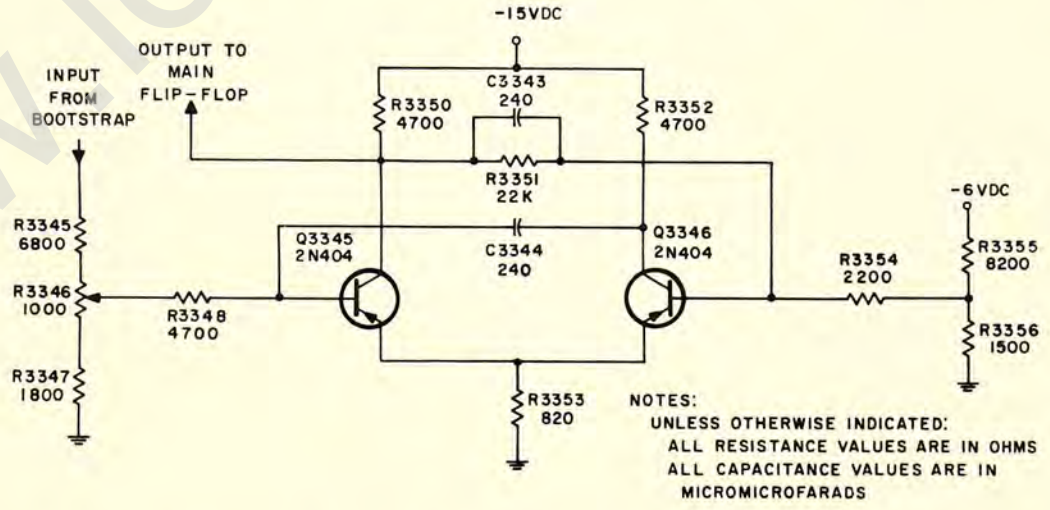


Figure 4-103. Schmitt Level Detector, Schematic Diagram

this happened, the sweep would partially recover and start again, giving erratic and nonrepresentative presentations.

To prevent this, a squaring amplifier, a diode switch, and an RC filter network are included in the circuit. The partial block diagram of this arrangement is shown in figure 4-105. This circuitry is also used in the INT TRIG position since some of the optional vertical inputs, such as a probe signal, may cause the horizontal main flip-flop to trigger at an insufficient rest time between sweep traces.

When an external signal of an irregular waveshape is applied, the squaring amplifier creates sharply spiked pulses suitable for triggering a flip-flop circuit. The first one of these will be passed by the diode switch to the main flip-flop causing it to change state. If this change-of-state information was applied immediately back to the diode switch, the switch would instantaneously cut off the signal to the main flip-flop. But there is an RC circuit in the line that prevents an instantaneous cutting off of the diode switch, so that the bias is gradually applied, thereby limiting the input spikes. The input spikes are completely cut off and are no longer present by the time the sweep of the sawtooth sweep circuit is complete and the main flip-flop has been reset by the Schmitt level detector. The cutoff bias is removed from the diode switch when the main flip-flop does change state at the end of the trace. But, again, this action cannot be instantaneous because of the RC circuit. It takes an appreciable amount of time for the switch to turn all the spiked input back on so it will reach a large enough value to trigger the main flip-flop again. Therefore, the sweep circuit has a time sufficiently long to completely recover before the sweep action has a chance to be prematurely initiated again by an input spike. The waveforms at the various points marked on the block diagram appear in figure 4-106.

Figure 4-107 is a partial schematic of this gating arrangement between the squaring amplifier and the main flip-flop. There are two sections to this gate. The first section includes diodes CR3414, CR3406, CR3413, and CR3411. The common cathode connection of these diodes is applied to the input of Q3402. When the output of the squaring amplifier is desired, then CR3414 is conducting.

The other part of the gate includes diodes CR3420 and CR3421 and their associated circuitry. To understand the operation of this gate, the purpose of the output of the main flip-flop must first be considered. The main flip-flop provides the triggering pulse necessary for activating the bootstrap circuit. The sweep trace produced would be in error if the bootstrap was triggered a second time before it had a chance to recover from the initial sweep. Resistor R3429, capacitor C3413, and diode CR3421 prevent this pretriggering from occurring. Diode CR3421 will keep a cutoff bias on CR3420 so that a quick second trigger from the squaring amplifier will not affect the main flip-flop. Resistor R3429 and capacitor

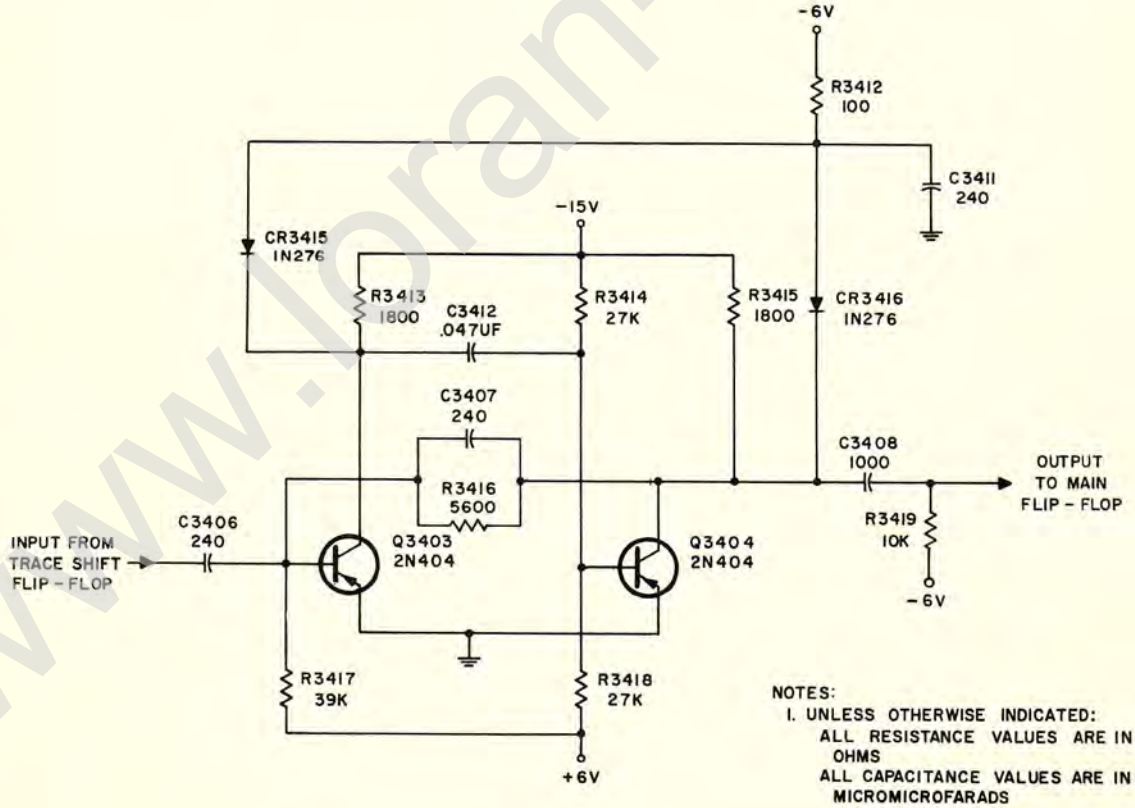


Figure 4-104. Monstable Multivibrator, Schematic Diagram

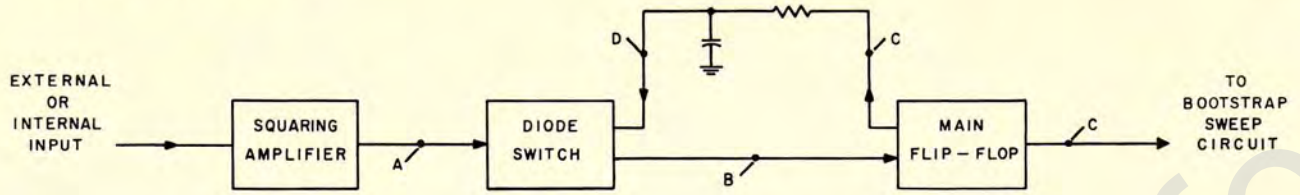


Figure 4-105. Squaring Amplifier Triggering Circuit, Block Diagram

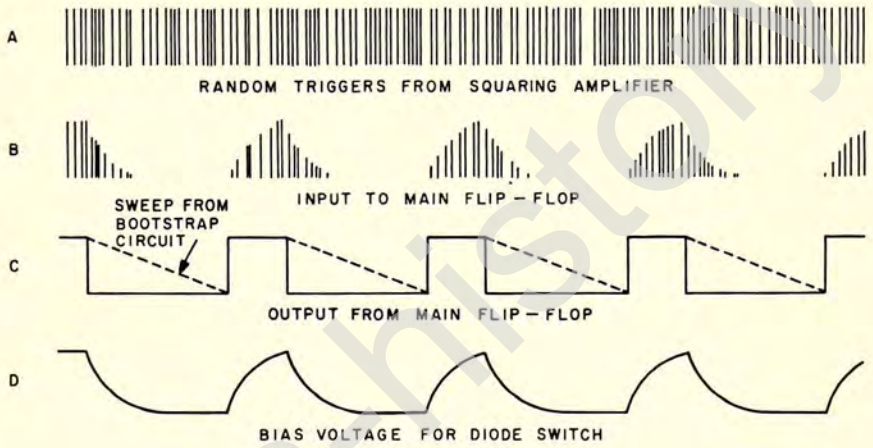


Figure 4-106. Squaring Amplifier Triggering Circuit, Waveshapes

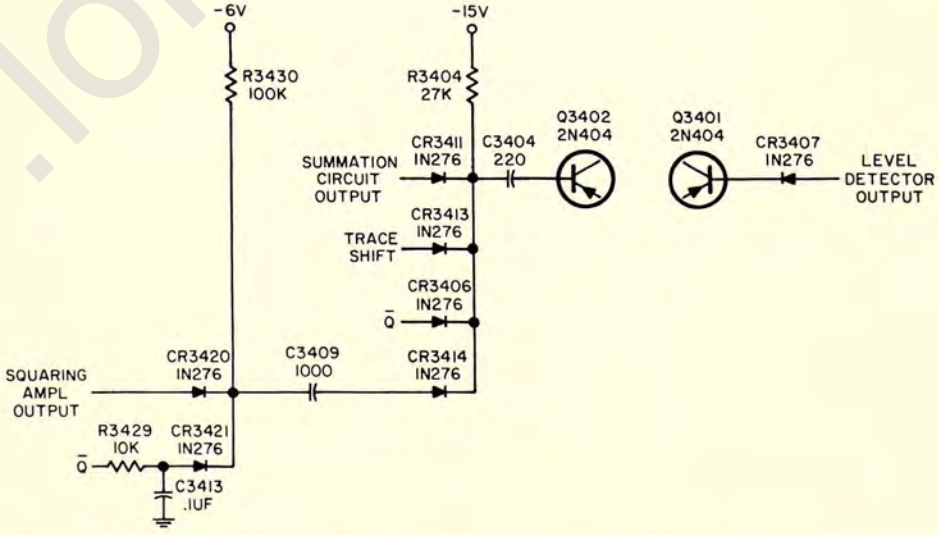


Figure 4-107. Triggering Circuit from Squaring Amplifier to Main Flip-Flop Schematic Diagram

C3413 form the time-delay circuit for CR3421. When there has been a sufficient time lapse for the bootstrap to complete its sweep and to be reset, the bias from CR3421 will be removed and an output from the squaring amplifier will be able to again trigger the main flip-flop.

Notice that a similar type circuit is not necessary for the monostable multivibrator or for the other triggering optional inputs. This is because the timing of the other possible signal is regular; whereas the input to the squaring amplifier may be erratic, and the possibility of a quick second trigger is a definite possibility.

The squaring amplifier is also a Schmitt trigger and is almost identical to the level detector. See figure 4-108. The squaring amplifier receives a signal that may be of a random nature and, when a certain negative level is reached, produces a sharply-peaked positive pulse for gating the main flip-flop.

There is only one main difference between this circuit and the level detector. The bias on the base of Q3406 is maintained at a much lower level by using only a 4700-ohm resistor, R3428, and no biasing voltage. The level of operation is only dependent on what is applied at the input to the circuit. A triggering level much less than -6 volts may be chosen by this method. However, Zener diode CR3422 will shunt excessively high voltages to ground if a large voltage that would normally be harmful to transistor Q3405 is applied. Notice also that the collectors of both transistors are clamped to -6 volts by the use of diodes. This prevents output pulses from reaching a level more negative than -6 volts.

(4) HORIZONTAL DEFLECTION AMPLIFIER. - The input to the horizontal deflection amplifier is the saw-tooth sweep from the bootstrap circuit. The input is at quite a high level so the network of R3471, R3472, and R3473 (figure 4-109) is used to attenuate the signal greatly before it is applied to the remainder of the circuit. Hence, the variable potentiometer at the input is essentially only a gain adjustment. Prior to the initiation of sweep, Q3471 is cut off and its collector potential is approximately at -15 volts. When the potential at this point is -15 volts, the potential at the base of Q3472 is -5 volts. Each Zener diode, CR3471 and CR3472, accounts for one-half of the 10-volt drop, 5 volts. The emitter at cutoff is slightly more negative than at the base, still approximately 0 volt. The current on the emitter will follow the base current when the negative sweep input is initiated. However, the biasing network of resistors R3475, R3476, R3477, and R3478 determines the current flow through Q3471 and, hence, the voltage on the collector of Q3471. The changing voltage does not materially affect the emitter voltage. Horizontal positioning can be achieved by adjustment of R3477. Notice also that Q3471 is essentially a phase-splitter with small incremental changes in voltage applied to its base.

The base of Q3472 is tied through R3479 to a specific voltage reference, +15 volts. The current flow through Q3472 is determined by resistor R3483, and the gain of Q3472 is determined by the ratio of the emitter and collector resistors. The voltage output is controlled by the voltage applied to the emitter. The voltage level is set by voltage divider R3480 and R3484 and by the +6-volt bias. Notice that the circuit of Q3473 is similar to that of Q3472 with respect to these resistors. Resistors R3480 and R3484 establish the emitter voltage reference and do not otherwise affect the resistance of the emitter circuit.

By joining R3483 and R3485 to the same voltage divider, a cancelling effect of the increases and decreases of instantaneous voltages can be achieved so that the current through R3480 and R3484 stays constant.

The outputs from Q3472 and Q3473 are supplied through 22-ohm resistors R3482 and R3487 to triode amplifiers V3471A and V3471B. These amplifiers supply the driving voltage for the horizontal deflection plates in the cathode ray tube.

c. VERTICAL CIRCUIT. - The vertical input circuit receives selected signals from the receiver and prepares them for insertion to the vertical deflection amplifier circuit, where the trace separating action also occurs. Four possible signals from the receiver may be selected for viewing. These are the r-f signal consisting of master and slave pulses, the input to the envelope strobe (output from the in-phase detector), the input to the derived envelope-strobe portion of the detector-strobe, and the agc voltage. In addition, when the indicator is used as a regular oscilloscope, an external signal may be inserted at the probe position.

(1) ATTENUATOR. - The attenuator network at the input of the circuit provides a means of selecting the range for whatever strength signal is inserted. See

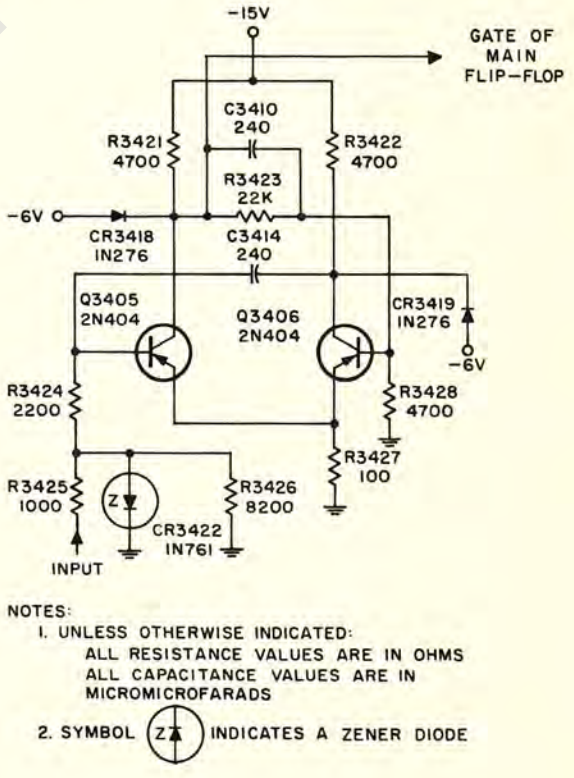


Figure 4-108. Squaring Amplifier, Schematic Diagram

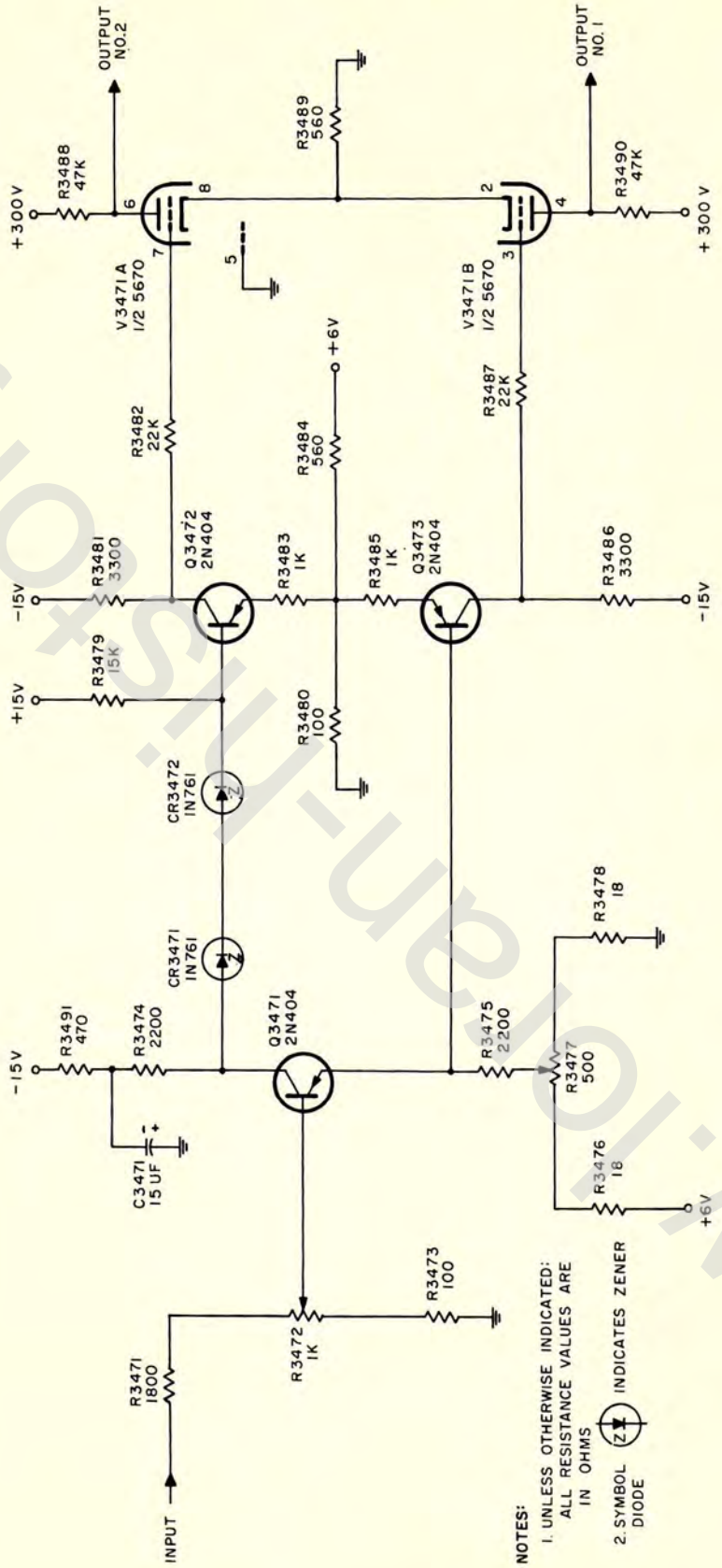


Figure 4-109. Horizontal Deflect on Amplifier, Simplified Schematic Diagram

the schematic diagram for the vertical input circuit, figure 4-110. For instance, when the 50 position is selected by the VERT SENS switch, a 100-volt peak signal will result in a full-scale representation on the scope. Other possible positions for the VERT SENS switch are the .05, .5, and 5 volt positions. The signal at the attenuator is applied to isolation amplifier stage Q3101, which also includes a continuously variable gain control. The signal supplied from this point is applied to one of three alternate paths. One path is through the 100-kc bandpass selective amplifier (which also supplies the signal through the notch filters); another bypasses the selective amplifier and only goes through the notch filters; and the third bypasses both the notch filters and the selective amplifier. Attenuator pads are provided in two of these paths for equalizing their levels. Regardless of the path taken, before the resultant signal is applied to the vertical deflection amplifier, it is applied to an amplifier, an emitter-follower, a phase splitter, and a push-pull output amplifier stage. The input signal is selected by the SIGNAL switch on the front of the indicator unit. The r-f signal generated in the receiver that is made up of the master and slave pulses is one signal that may be selected. The in-phase detector signal from the receiver, the derived envelope signal from the receiver, the receiver agc signal, or any external signal can also be selected by the SIGNAL switch.

The selected signal is then applied to the VERT SENS switch. This circuit consists of a group of four resistors. The 46, 400-ohm resistor may be shorted or used in a voltage divider arrangement with a 5620-ohm, a 464-ohm, or a 46.4-ohm resistor. The input level may thus be selected in multiples of 10. The signal is then a-c coupled to the isolation amplifier in the circuit. Emitter follower transistor Q3101 contains a variable GAIN control in its emitter circuit for adjusting the overall gain of the network.

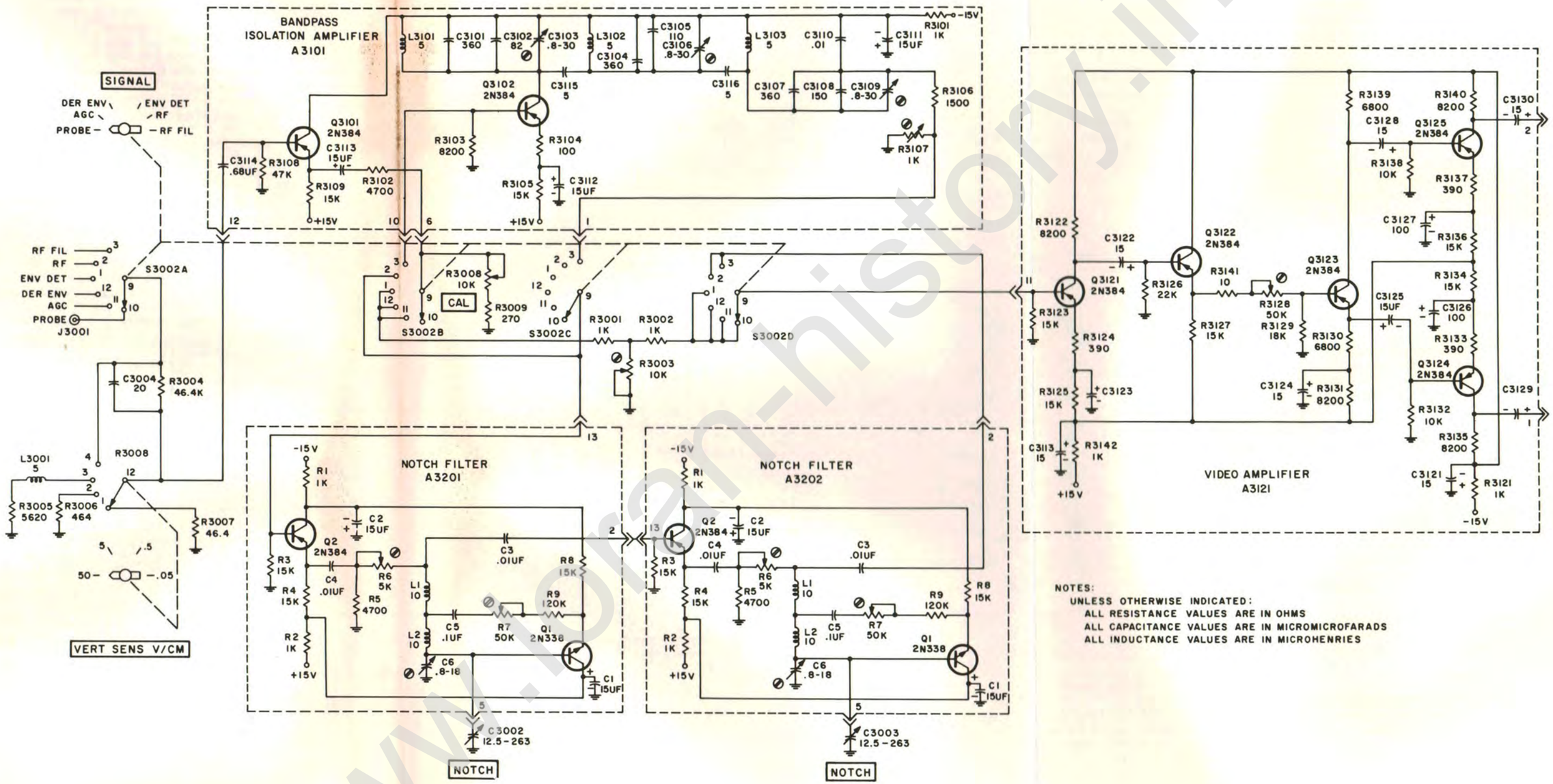
The signal from Q3101 may be applied to three different paths according to the position of the SIGNAL switch. The RF FIL position selects the 100-kc selective amplifier. Transistor Q3102 and its associated circuit comprise this amplifier stage. The base of Q3102 receives the signal. The operation of Q3102 is stabilized by degenerative feedback through small, nonbypassed resistor R3104 in the emitter circuit. The amplified signal from Q3102 is then supplied to the tuned bandpass-filter circuit.

(2) BANDPASS FILTER. - This circuit is very sharply tuned to select 100 kc by three piston-type glass capacitors that must be tuned simultaneously. There is approximately a 6-db drop at a 1-kc difference from this frequency. There is a much greater attenuation at a greater variance than 1 kc. By narrowing the passband in this respect, the signal-to-noise ratio is greatly increased. Therefore, when the received signal is extremely weak and hard to detect, the RF FIL position of the switch is selected. The signal from the filter undergoes a level adjustment in R3106 and R3107. The overall path adjustment and the two path adjustments each consist of a fixed resistor-variable reistor combination. The combination acts as a voltage divider network so that the voltage across a variable resistor to ground is one half and the fixed resistor in the signal lines is the other half.

(3) NOTCH FILTERS. - Because the RF FIL position of the SIGNAL switch is used for noisy signals, the notch filters as well as the selective amplifier are used. The two notch filters are identical in operation and each may be tuned over a range of 70 to 130 kilocycles. The two notch filters are identical stages. Each consists of an emitter-follower arrangement and a Q-multiplier. The notches reject undesirable signals in the neighborhood of the Loran-C signals to eliminate the possibility of interference. The wide tuning range of the notches makes it possible to tune both notches on the same side of 100 kc if it is desirable in a particular situation. As much as 30-db attenuation may be achieved. See figure 4-111. In essence, the notch filter is a series-tuned, LC circuit to ground. The required attenuation for rejection could be achieved without the use of an active network; but without it, the bandwidth of the notch would be too large. Without a Q-multiplier, the LC circuit would be limited by the inherent amount of parallel resistance associated with the circuit.

The voltage at the junction point can be made nearly equal to the voltage returned to Q1 by adjusting R7, since the gain through the emitter follower is approximately unity. Theoretically, with this method it is possible to obtain an infinite Q by completely eliminating the inherent resistance of the tuned circuit. The Q-multiplier provides the circuit with a negative resistance that will counteract the undesirable effects of the large parallel positive resistance. See figure 4-112 for the schematic diagram of a notch filter. In effect, Q2 is an emitter-follower which couples its positive feedback to the split inductor of the tuned circuit. Potentiometer R7 merely limits the amount of the signal that is fed back. Resistor R7 is used in this filter circuit to adjust the positive feedback and, therefore, to control the depth of the notch. Resistor R6 controls the width of the notch, also having some side effect on the depth. Capacitor C3002 (or C3003) on the front of the panel adjusts the notch frequency. Capacitor C6, paralleled with C3002 (or C3003), is a trimmer capacitor for calibrating the circuit. The signal from the second notch filter is coupled by C3 to an isolation amplifier stage, Q3121, the first stage of the vertical amplifier. Hence, the signal has gone through the selective amplifier and both notch filters if the SIGNAL switch is set to the RF FIL position.

The signal does not go through the selective amplifier when the switch is in the RF position, but is supplied directly to the notch filters. The notch filters are bypassed when the SIGNAL switch is placed in any of the four remaining positions. In these positions, the signal passes through the 10,000-ohm resistors and a variable 10,000-ohm resistor, where the level is adjusted. In two of the three possible signal paths, there are level adjustments so that the scope presentation for any of the three may be approximately equalized when switched from one to another by the SIGNAL switch.



NOTES:
UNLESS OTHERWISE INDICATED:
ALL RESISTANCE VALUES ARE IN OHMS
ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS
ALL INDUCTANCE VALUES ARE IN MICROHENRIES

Figure 4-110. Vertical Input Circuit, Schematic Diagram

(4) PROBE ADJUST BOARD E3001. - Probe adjust board E3001, together with STROBE adjust R3025 provide a means for displaying the strobe sample point on the face of the oscilloscope. The inputs applied to the circuit are the IMT, IXT, and IYT triggers supplied from the agc monitor circuit in the receiver. These pulses are each square waves varying between +6 volts and -6 volts. The ordinary neutral level of the indicator triggers is -6 volts. At the time of a guard strobe trigger in the receiver the pulse goes from its -6-volt level to +6 volts. Each indicator trigger stays at +6 volts until the time of the signal strobe (sample) point, at which time it drops to the -6-volt level again. The probe-adjust circuit triggers on this negative-going trailing edge.

Diodes CR3001 and CR3002 and resistor R3014 form an OR circuit at the input to the probe adjust circuit. The IMT trigger is supplied to CR3001 and either IXT or IYT, as selected by S3013, is supplied to diode CR3002. Neither slave trigger is selected when S3013 is placed in the SLOW position and only the master sample part can be displayed.

The input arrangement of the circuit is shown in figure 4-113. When the indicator triggers are at their neutral -6 volts, the diodes of the gate are reverse biased and the junction at their cathodes is at a -6-volt level as established by the -6 volts supplied to R3014. At this same time, the +6 volts supplied through R3015 to the base of PNP transistor Q3001 will keep Q3001 cut off.

When a trigger input goes from -6 volts to +6 volts the applicable diode will conduct and raise the cathode junction to +6 volts. The change of voltage is positive-going so that the voltage reflected across C3007 will only make the base of Q3001 more positive, which has no effect on its operation. When the trailing edge of the applied signal occurs, the voltage applied to the diode drops from +6 volts to -6 volts. This cuts off the diode and returns the diode junction to -6 volts. The changing voltage across C3007 is now negative-going, driving the base of Q3001 below the ground potential applied to its emitter and causing it to conduct.

For the remainder of the circuit see the diagram shown in figure 4-114, which is essentially a monostable multivibrator. During neutral conditions of the circuit Q3002 is conducting because of the -6 volts applied to its base through R3018. The collector and the emitter are very nearly the same when Q3002 conducts; therefore, the output from the circuit is 0 volt. Since Q3001 is not conducting its collector is held to -6 volts by diode clamp CR3003. When Q3001 conducts its collector goes from -6 volts to 0 volt, the voltage on its emitter. The voltage across the coupling capacitor instantaneously stays constant thereby raising the base of Q3002 to a positive potential, which cuts off Q3002. Resistor R3016 provides a feedback path for the minus voltage which is now on the collector of Q3002 to the base of Q3001, accelerating the cut-off action of Q3001. The collector output of Q3002 is clamped to -6 volts by CR3004 so that the strobe output cannot exceed this value. The circuit returns to its neutral condition when the voltage across C3007 stabilizes by discharging through resistor R3014.

Front panel STROBE adjust R3025 and fixed resistor R3024 provide a means of adjusting the

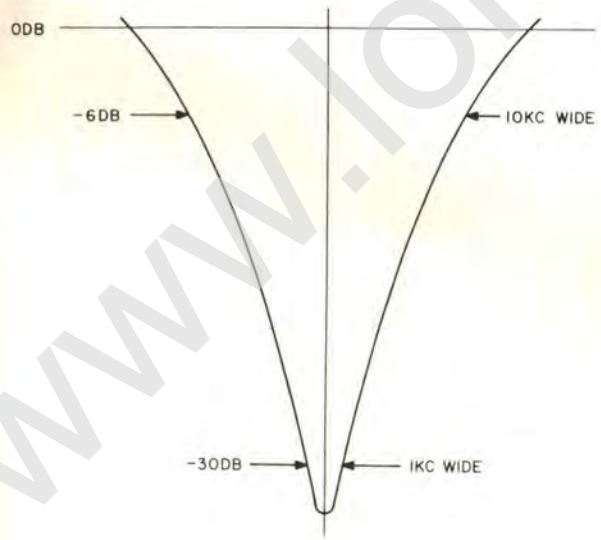


Figure 4-111. Notch Rejection Diagram

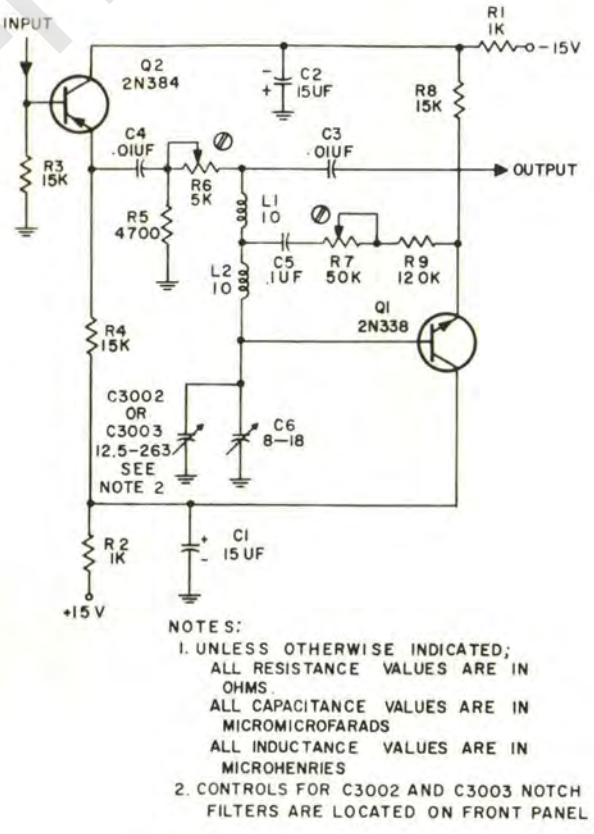


Figure 4-112. Notch Filter, Simplified Schematic Diagram

level of the strobe signal before its application to the video amplifier circuit.

Resistors R3001, R3002, and R3003, also mounted on board E3001, form a probe gain adjustment to control the level for every input selected by the SIGNAL control except RF and RF FIL, as shown in figure 4-110.

(5) VERTICAL AMPLIFIERS. - The vertical, or video, amplifier portion of the circuit is common to all signal paths and consists of an amplifier stage, followed by an emitter follower, a phase-splitter, and a push-pull amplifier. See figure 4-110 for the schematic diagram . The signal is applied across a 15,000-ohm input resistor to the first amplifier, Q3121. The amplified signal is then applied to emitter follower Q3122 and then d-c coupled to Q3123. Transistor Q3123 is a phase splitter which develops one output at the emitter and another output on the collector. These two outputs are approximately equal in magnitude with reference to ac. The emitter circuit differs from the collector circuit by the 8200-ohm resistor and the 15-uf capacitor that keep the transistor biased and in a conducting state. Both outputs from Q3123 are RC coupled to an amplifier stage, one to Q3124, and the other to Q3125. Each of these stages is identical to the first amplifier stage of the vertical amplifier circuit, Q3121. Both unbypassed and bypassed emitter resistors are employed to produce satisfactory gain and still allow adequate bandwidth characteristics. The large bypassed resistor also enhances the stability of the circuit. Actually each amplifier operates independently of the other, but push-pull action is achieved because the input signal into the amplifiers are 180° apart. The outputs from the video amplifier are coupled to the vertical deflection amplifiers.

(6) VERTICAL DEFLECTION AMPLIFIER. - The vertical deflection amplifier circuit receives the r-f signal from the receiver through the vertical input circuit and prepares it for display on the cathode ray tube. Figure 4-115 is the schematic diagram of the circuit. The circuit consists of two emitter followers, two diode switches used to gate the trace-shift biases, and two vacuum-tube amplifiers. There are two controls: the vertical positioning potentiometer is used to position both traces simultaneously; the trace separator circuit is used to position one trace with respect to the other, either closer or farther apart.

The input from the vertical input circuit enters the vertical deflection circuit at the bases of transistors Q3151 and Q3152. These transistors both operate to a -15-volt collector bias. A balanced input resistor network composed of R3152, R3154, and R3155 ensures that the bias level on each input is the same.

Facilities are provided for vertically positioning the display on the screen. Notice that there is a voltage divider network between -15 volts and ground consisting of R3151, R3152, and part of R3154. As R3154 is varied, the resistor ratio of this voltage divider is also varied. This would, in itself, change the ultimate vertical deflection of the

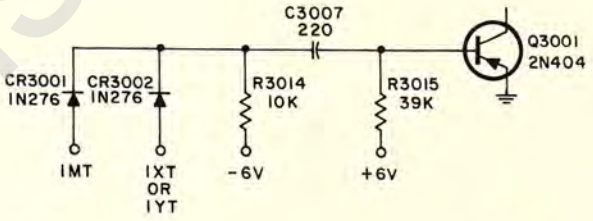


Figure 4-113. Input Circuit to Probe Adjust Board E3001

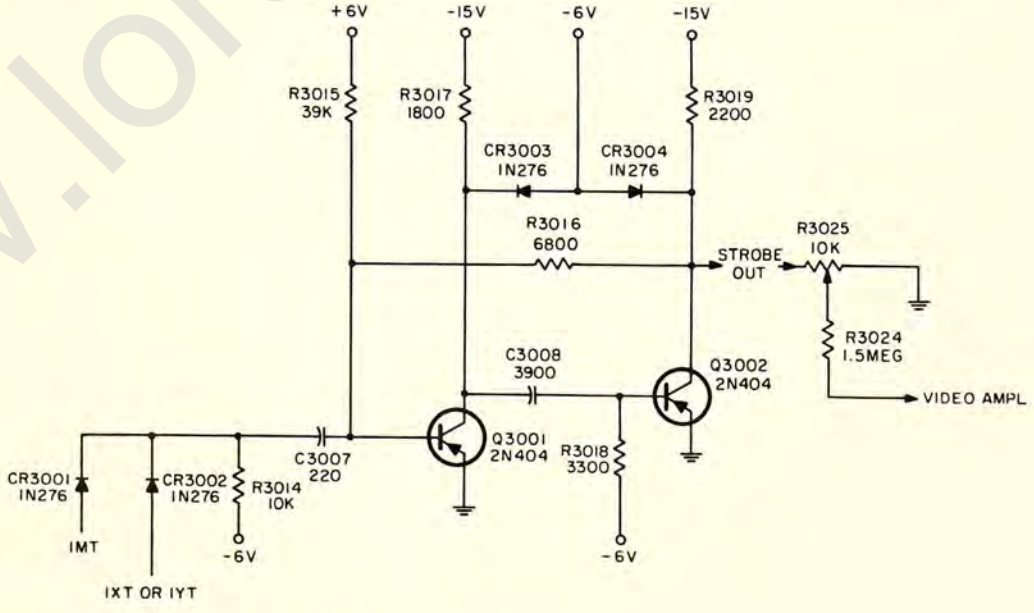


Figure 4-114. Probe Adjust Board E3001, Schematic Diagram

trace. But this condition is compounded because R3154 is not only a part of the voltage divider circuit for Q3151, but also is part of the voltage divider circuit for Q3152. As the voltage on the base of Q3151 increases, the voltage on the base of Q3152 decreases. This results in a push-pull effect of the two outputs of the circuit. By this method, compensation for any unbalanced pair of components can be made. Resistor R3154 will therefore control both the up and down position of both traces simultaneously.

The outputs from Q3151 and Q3152 are taken from their respective emitters so as to provide proper impedance levels to be applied to the final vacuum-tube stages. Input resistors R3159 and R3157 are used to provide the necessary d-c coupling and to provide one-half of a voltage divider used to change the voltage to V3151.

The level change of the inputs to both halves of V3151 is the means used to accomplish the trace shift. Both trace shift inputs are alternately either 0 or -6 volts. While the first trace shift input is 0 volt, the second will be -6 volts. Conversely, when the second trace shift input is 0 volt, the first trace shift will be -6 volts. It is assumed that at the first instance of time the $\overline{Q}$ input is -6 volts. Under this condition, the cathode of diode CR3151 is at some level between -6 volts and ground, and hence more negative than the anode. Diode CR3151 will conduct. At the same instant of time, the second trace shift input, Q, will be 0 volt. Diode CR3152 will be cut off since the anode of CR3152 will be more negative than the anode. Therefore, the voltage on the grid of V3151B will be established by voltage divider R3159 and R3160. During the alternate cycle of trace shift inputs, when $\overline{Q}$ is 0 and Q is -6 volts, diode CR3152 will conduct and CR3151 will cut off. Now, there will be a voltage established on the grid of V3151A determined by resistors R3157 and R3161. This results in a reference voltage level applied to the grid of V3151B which alternates between a low and a high value. At the same time, the grid reference level on V3151A will be going through the alternate sequence of first being high and then low and then high. Since the two voltages are applied to the two vertical deflection plates, they work together so that for the first period of time the vertical inputs are first being applied on the top trace and then on the bottom trace. Adjustment of R3168 determines how close the sweeps will be to one another. This establishes the anode bias on CR3151 and CR3152 and, hence, through the respective voltage dividers, the potentials at the grids of V3151B and V3151A.

The vacuum-tube stages provide the high voltage necessary to drive the vertical deflection plates of the electrostatic deflecting cathode ray tube. The push-pull arrangement provides optimum gain and linearity for the range of input signals.

One other use for the deflection circuit is to provide the means by which an internal trigger may be extracted for triggering the main flip-flop of the horizontal sweep circuit. When the INT TRIG position of the BASIC PRR switch is selected, there are

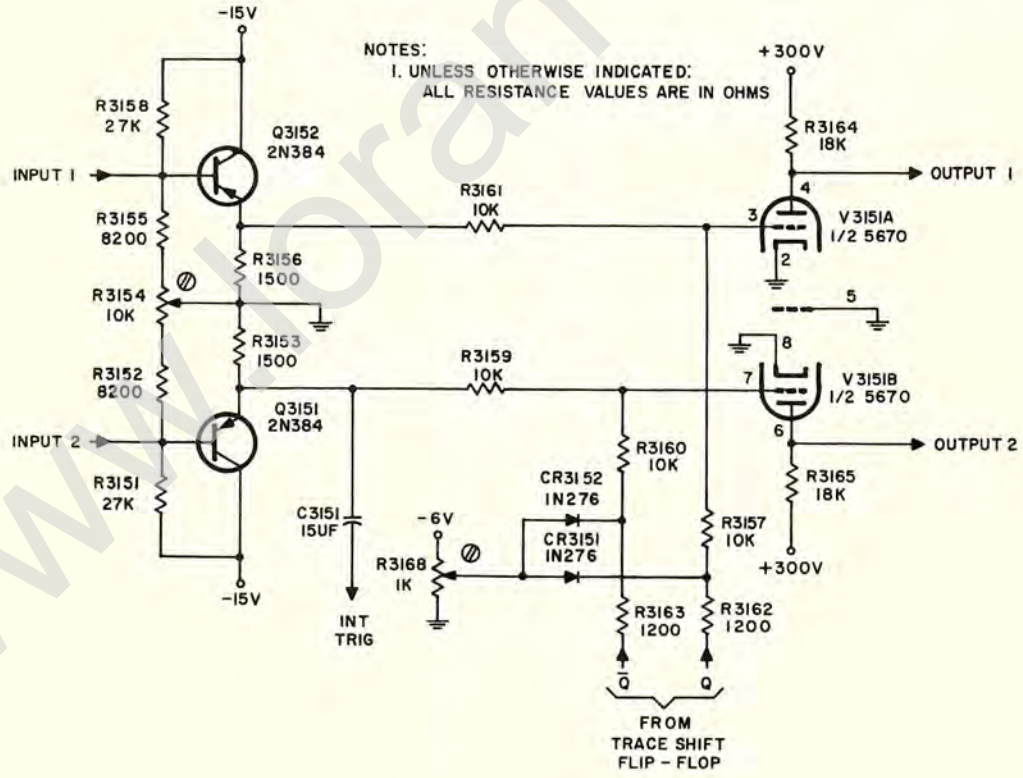


Figure 4-115. Vertical Deflection Amplifier, Schematic Diagram

no means inherent to the circuit that will change the state of the main flip-flop and trigger a second sweep trace. Capacitor C3151 is used to couple this needed trigger from the emitter of Q3151 to the horizontal sweep circuit.

d. CATHODE RAY TUBE CIRCUIT AND POWER SUPPLIES. - The cathode ray tube displays the traces presented to it by the remainder of the indicator circuit. The low voltage power supply furnishes power for the entire indicator. The high voltage supply is necessary primarily for the operation of the cathode ray tube.

(1) BLANK-UNBLANK CIRCUIT. - See the block diagram of the blank-unblank circuit in figure 4-116, to the schematic diagram in figure 4-117, and to the time sequence diagram of figure 4-118. The input to the circuit is derived from the main flip-flop network of the sweep generator circuit. The signal is either -6 volts or 0 volt. It is desirable to have a signal which has a wider degree of separation than 6 volts; one in that the separation can be varied; and one that is tied to a negative level below the cathode bias on the cathode ray tube so that it can be used to cut off the tube.

The change in voltage level from approximately 0 to -1100 volts is accomplished with the use of a Colpitts oscillator. The oscillator is tuned to operate at a frequency far above any signals used in the system. This high frequency is not critical and has been selected at around 750 kilocycles. The -6 volts applied to the input triggers the oscillator. The oscillator signal is then applied to capacitor C3448. The d-c voltage drop across this capacitor accomplishes the required change in level. The a-c signal is rectified by the diodes, and the applied signal to the Schmitt trigger alternated from a level near -1100 volts to a slightly more negative voltage. This difference in level is not enough to provide the necessary control for the cathode ray tube but is sufficiently large to trigger the Schmitt circuit.

The Schmitt circuit is similar in operation to the circuit used in the level detector and in the squaring amplifier of the sweep generator. Transistor Q3802 is not conducting when the oscillator is on since there is no current in its collector circuit and the emitter is at the applied bias voltage of approximately -1200 volts. The drop across the portion of R3821 between the center tap and the -1200-volt bias will keep CR3803 cut off. Therefore, there will be no current flow in the control grid circuit of the cathode ray tube and -1200 volts will be applied. Notice that the cathode voltage is more positive than this by the amount of drop across the Zener diodes CR3804 and CR3805. Thus, the cathode ray tube is cut off. The tube is cut off independently from the adjustment of R3821, and diode CR3803 is biased so that it will not conduct.

When the oscillations stop, a positive-going voltage will cut off Q3801 and cause Q3802 to conduct. The voltage on the emitter of Q3802 becomes more positive. The voltage on the center tap of R3821 limits the rise since the diode operates below saturation. The anode voltage on CR3803 will rise to a level just slightly more positive than its cathode so that the diode will conduct. Resistor R3821 provides the desired variable control for the control grid voltage on the cathode ray tube. Notice that this is provided only when the cathode ray tube is conducting. As explained above, R3821 will be ineffective when the cathode ray tube is not conducting and will not limit the extent to which the tube is cut off in any way. During ON periods of the cathode ray tube, R3821 does control the brightness.

A focus control is also provided by the blank-unblank circuit. Notice that there is a voltage divider network in the joint emitter circuit of Q3801 and Q3802. One side of the divider is tied to ground through R3820. The other side is set by the emitter voltage of the conducting transistor, either Q3801 or Q3802. The two emitter voltages are not materially different during their respective conducting cycles. Hence, the drop across the whole network is constant and relatively independent from the operation on the

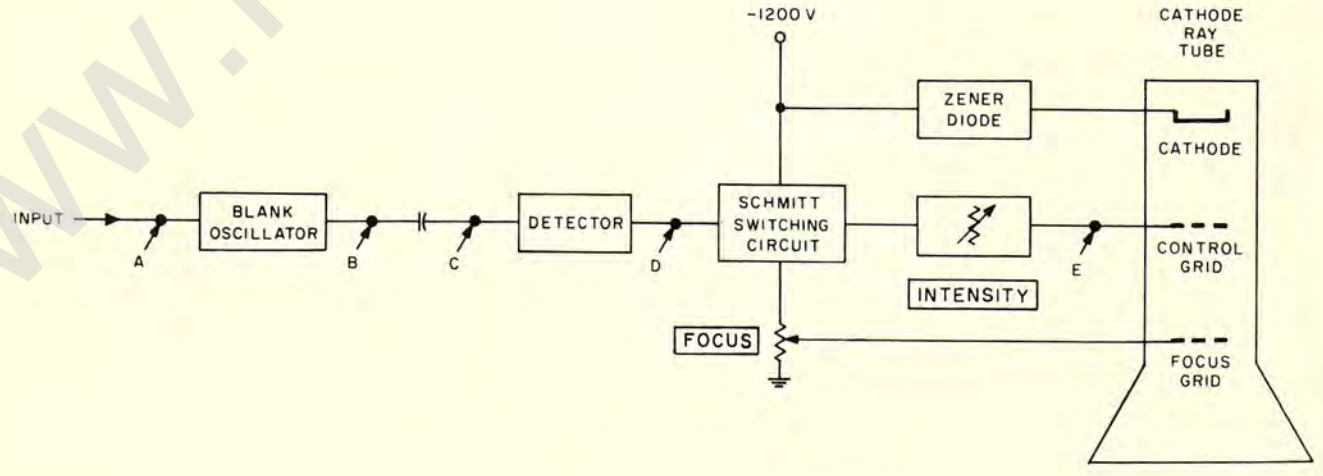


Figure 4-116. Blank-Unblank Circuit, Block Diagram

voltage divider so that it can effectively vary the anode voltage over its desired range to achieve the required focus.

The ASTIGMATISM control, R3820, adjusts the voltage on the main anode of the cathode ray tube, pin 8. The voltage that may be applied is between 0 volt (ground) and +300 volts.

(2) CATHODE RAY TUBE. - The cathode ray tube used in the indicator is an electrostatic-type tube with the tube elements arranged as illustrated in the figure 4-119.

The tube is approximately 12 inches in length and has a nominal flat-face diameter of approximately 5 inches. The phosphor used to coat the surface of the tube is of the P1 type. This is a medium persistent substance that traces a green line when illuminated. The pin connections for the 12 pins and the cap are also shown in the diagram. The typical operating voltages, using the cathode voltage as a reference, are shown in table 4-8.

TABLE 4-8. TYPICAL OPERATING VOLTAGES FOR CRT

Cathode (reference)	- 0 volt dc
Heaters	- 0 volt dc (6.3 volts ac)
Control Grid	- Cutoff voltage: -90 to -45 volts dc Operating voltage: not more positive than 0 volt dc
Focus Grid	- +200 to +600 volts dc
Main Anode	- +1200 volts dc
Vertical and Horizontal Deflection Plates	- +1200 volt dc
Post Acceleration Anode	- +2400 volt dc

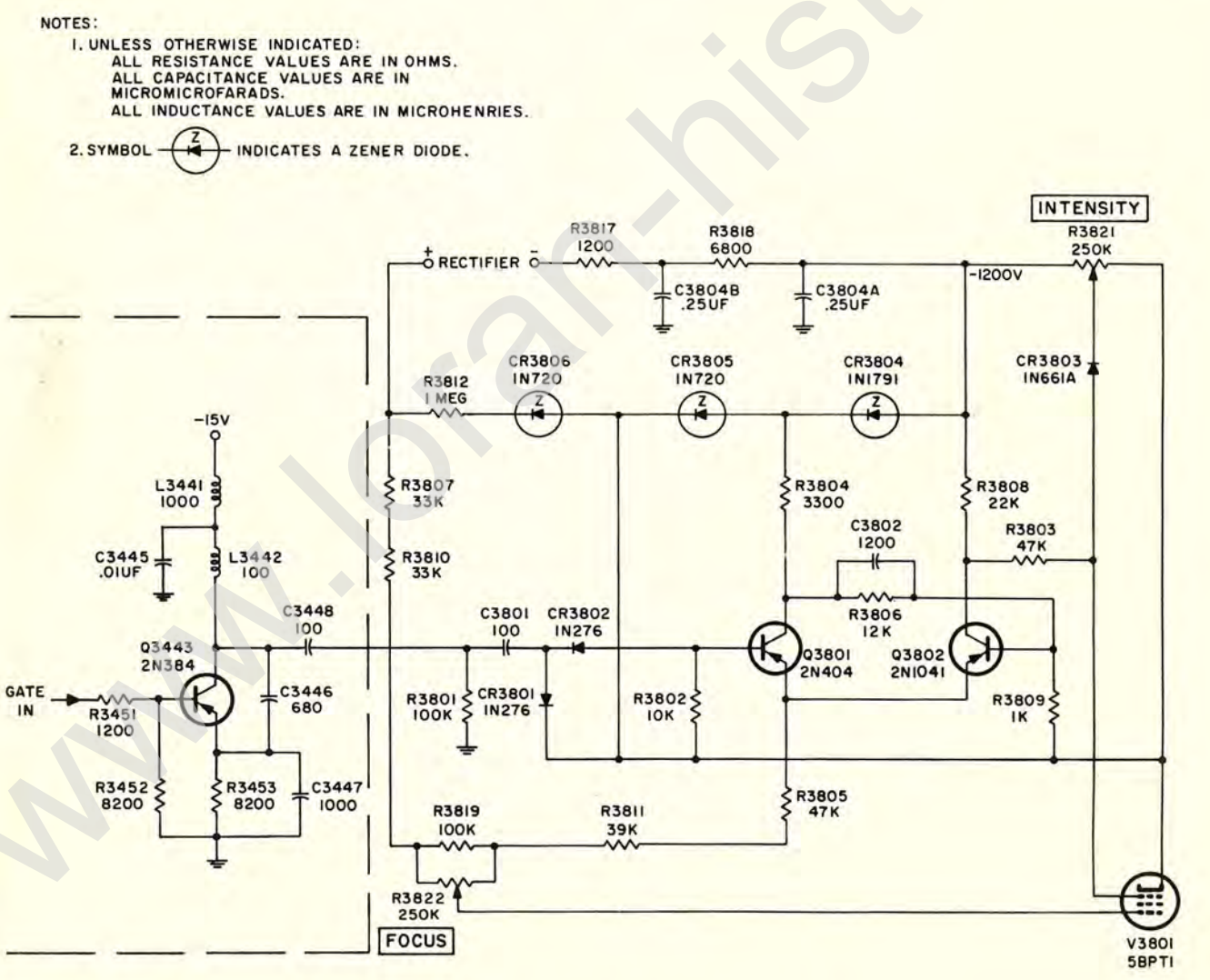


Figure 4-117. Blank-Unblank Circuit, Schematic Diagram

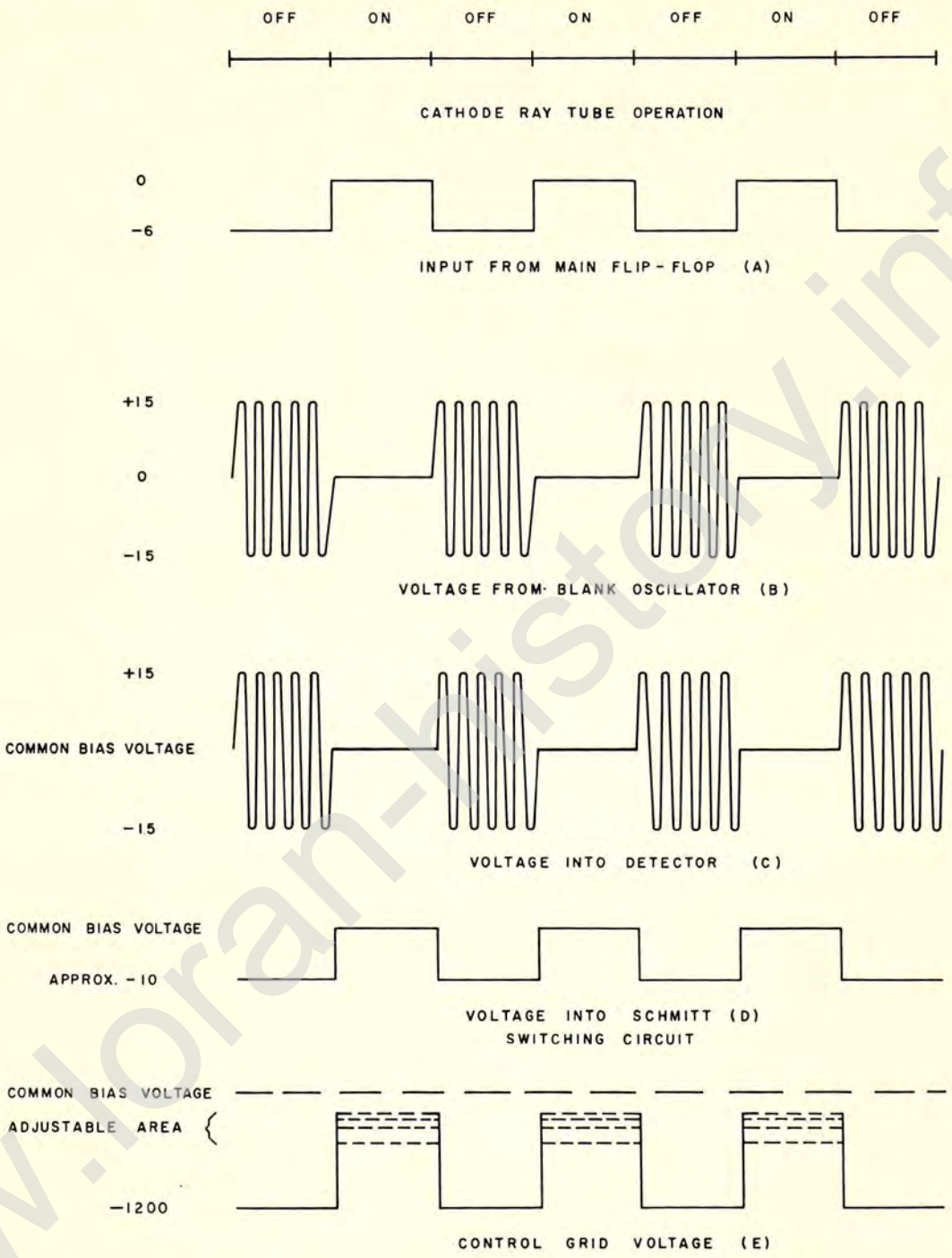


Figure 4-118. Blank-Unblank Circuit, Time Sequence Diagram

(3) CRT CONTROL NETWORK. - The cathode ray tube, has the following controls for regulating the overall appearance of the scope trace: (1) INTENSITY, (2) FOCUS, and (3) ASTIG, in addition to the trace position controls discussed in paragraph 4-3*c*(5). A simplified circuit arrangement for these controls is illustrated in figure 4-120.

The intensity is controlled by an adjustment which is contained within the blank-unblank circuit. The control does this by merely changing the bias on the control grid. The rate of electron flow from the cathode becomes greater as the potential on the grid is increased. This increases the brightness of the scope trace. The astigmatism adjustment is made

by varying the main anode potential. When the main anode is at approximately the same potential as the deflection plates, the overall illumination of the scope will be approximately the same. The focus control changes the potential of the focus grid. This is a sharpness adjustment that increases the trace definition in the area over which the trace passes.

To maintain the relative potential of the various elements of the tube and still minimize the high voltage potential from a zero reference, the main anode of the tube is tied to ground and two 1200-volt supplies are used, one positive with respect to ground and the other negative. The focus control is achieved by a voltage divider between ground and the -1200-volt cathode.

(4) LOW VOLTAGE POWER SUPPLY. - The low voltage supply for the indicator unit supplies +6 volts, -6 volts, +15 volts, -15 volts, and +300 volts dc and 6.3 volts ac for the operation of the circuit. See figure 4-121 for the schematic diagram.

The power transformer has three alternate primary tap connections. One is for a normal 115-volt, 400-cps input; the other two, the 125-volt tap and the 105-volt tap, are for making compensating connections when the source voltage becomes abnormal.

One of the secondary windings on the transformer derives the +300 volts used with the astigmatism control and the +300-volt B+ voltage for the tubes of the vertical and horizontal deflection amplifiers. A full-wave bridge rectifier using silicon diodes is used. A smaller secondary voltage may be used to create the same desired output voltage by using the bridge rather than a simple pair of diodes. Resistor R3601 prevents large surge currents from damaging the diodes in the bridge. Diodes CR3605, CR3606, CR3607, and CR3608 are Zener diodes which provide regulated +300 volts. The current through the diodes will increase as the load voltage is decreased. Similarly, the current through the diodes will decrease as the load voltage increases. This stabilizes the voltage across resistors R3603, R3604, R3612, and R3613.

The 6-volt supply is actually a combination of two separate rectifier-regulator circuits using the same secondary coil of the transformer. Since only a small output voltage is required, a pair of diodes is used to rectify the signal. Resistor R3605 protects the diodes of the positive supply, CR3609 and CR3611, against surge currents. The first Zener diode, CR3613, provides a regulated output of 10 volts, ±5 percent, across R3606. Zener diode CR3614 provides the final output voltage at a very stable 6 volts. The two stages of regulation ensure low ripple and good regulation.

The negative half of the supply is identical in operation with the positive half described above except that it operates with the negative half cycles of the applied voltage.

The 15-volt supply is similar to the 6-volt supply. Again, the positive voltage is derived from just one pair of diodes. This time, two separate negative (-15 volts) voltages are derived. One is for the horizontal circuit of the indicator and the other is for the vertical circuit. The two supplies will isolate transients created in one circuit from interfering with the performance of the other. Zener diodes are used to effectively reduce the voltage ripple and to provide two stages of regulation. In each of these supplies, the first diode reduces the voltage to 27 volts with a

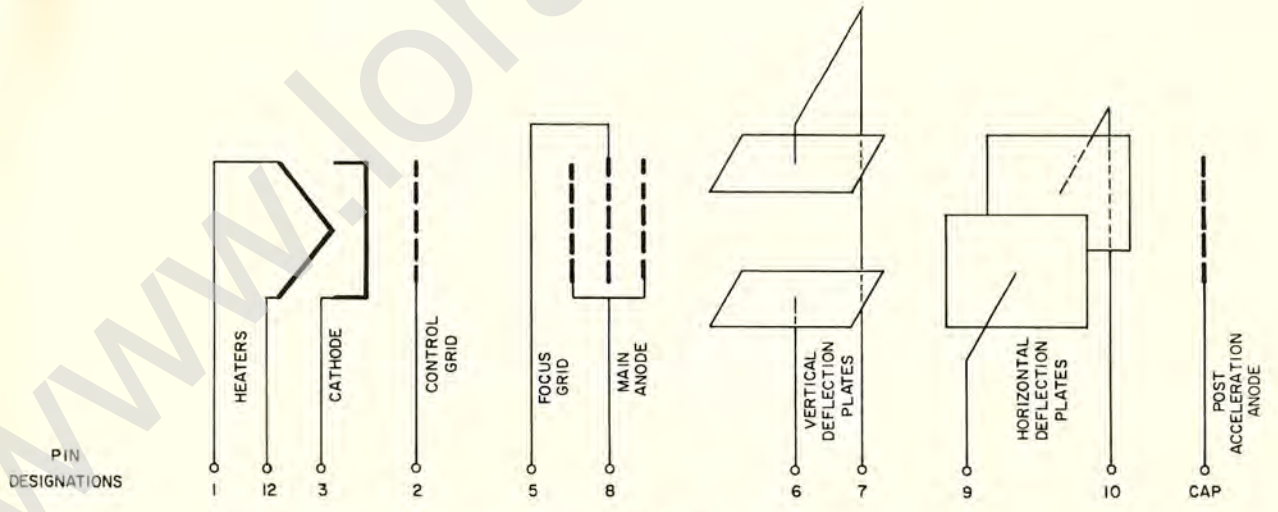


Figure 4-119. Tube Elements of Cathode Ray Tube

very small ripple, and the second provides the final -15-volt output with a negligible ripple.

The low voltage supply also has a secondary winding for supplying the heater voltage for the output tubes of the horizontal and vertical amplifiers.

(5) HIGH VOLTAGE POWER SUPPLY. - The high voltage supply for the indicator circuit is shown in the schematic diagram of figure 4-122. The supply furnishes positive 1200 volts for the post anode of the cathode ray tube, negative 1200 volts for the blank-unblank circuit, filament voltage for the cathode ray tube, and astigmatism bias voltage for the main anode of the cathode ray tube.

The primary of the transformer operates from a source voltage of 115 volts, 400 cps. There are three alternate taps on the transformer so that if the rated input voltage varies materially from 115 volts, the output can be maintained at a relatively stable condition. One of these is a 125-volt tap and the other is a 105-volt tap. There are three secondary outputs. Two of these are approximately 900 volts rms (1270 volts peak), and the other is approximately 6.3 volts. The voltage used for the post anode is around 1200 volts, but this can vary materially without greatly affecting the tube operation. Three silicon diodes are used in series to create a half-wave rectified output, which is subsequently filtered and smoothed by C3803 and R3813. Any surge voltage that could be injurious to the diodes is suppressed by R3813. The output is approximately 1200 volts. The current requirements are very small, hence the diodes are well protected.

The other secondary of the power transformer that is rated at a 900-volt rms value is rectified in a full-wave bridge circuit. Two diodes are used in each leg of the bridge to help protect the diodes from high peak inverse voltages. Resistor R3817 helps to protect the diodes in the bridge against current surges. The output from the rectifier is filtered by both sections of C3804 and R3808 so that the output has very low ripple.

The negative side of the first secondary and the positive side of the second secondary are tied together so that effectively there is a 2400-volt separation between the plus and minus voltages. Figure 4-119 illustrates how this separation is achieved. This junction is then connected to the center tap of the ASTIG (astigmatism) potentiometer. This variable resistor has one side connected to ground and the other side connected to +300 volts. By this method, the voltage on the main anode of the cathode ray tube can be varied with respect to the potential on the deflection plates. The astimatism control maintains the focus over the entire tube face.

By connecting the common side of the blank-unblank circuit to this variable resistor, all of the control voltages for the cathode ray tube will vary the same amount with any ripple voltages in the power supply.

The third secondary of the power transformer provides the heater voltage for the cathode ray tube. Since the cathode operates at a large negative voltage, it is necessary to strap one side of the heater voltage to the cathode in order to protect the heaters. Hence, the heaters also operate at high negative potential. This makes it impossible for the low voltage supply for the indicator unit to furnish the heater voltage for the cathode ray tube.

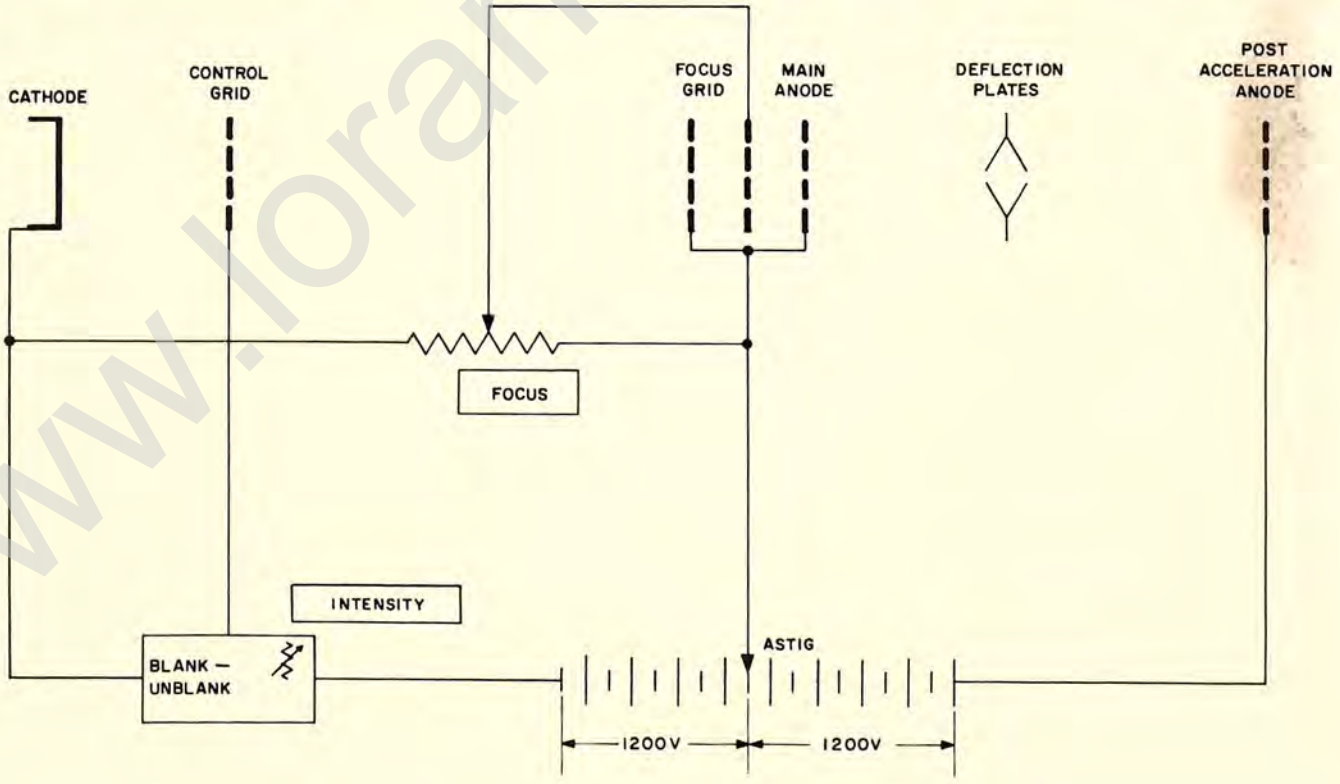


Figure 4-120. CRT Control Network, Simplified Schematic Diagram

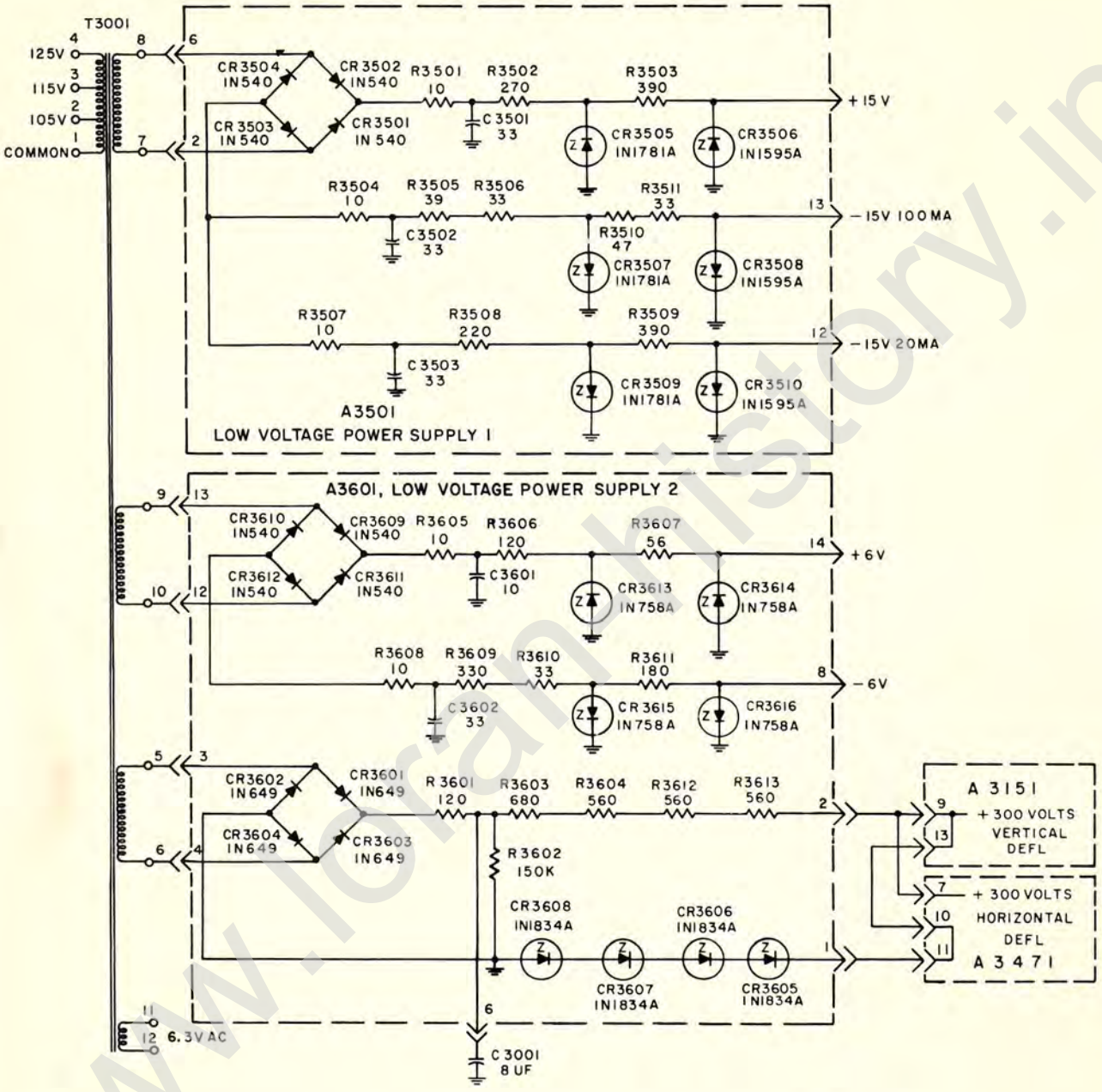


Figure 4-121. 6, 15, and 300-Volt Power Supplies, Schematic Diagram

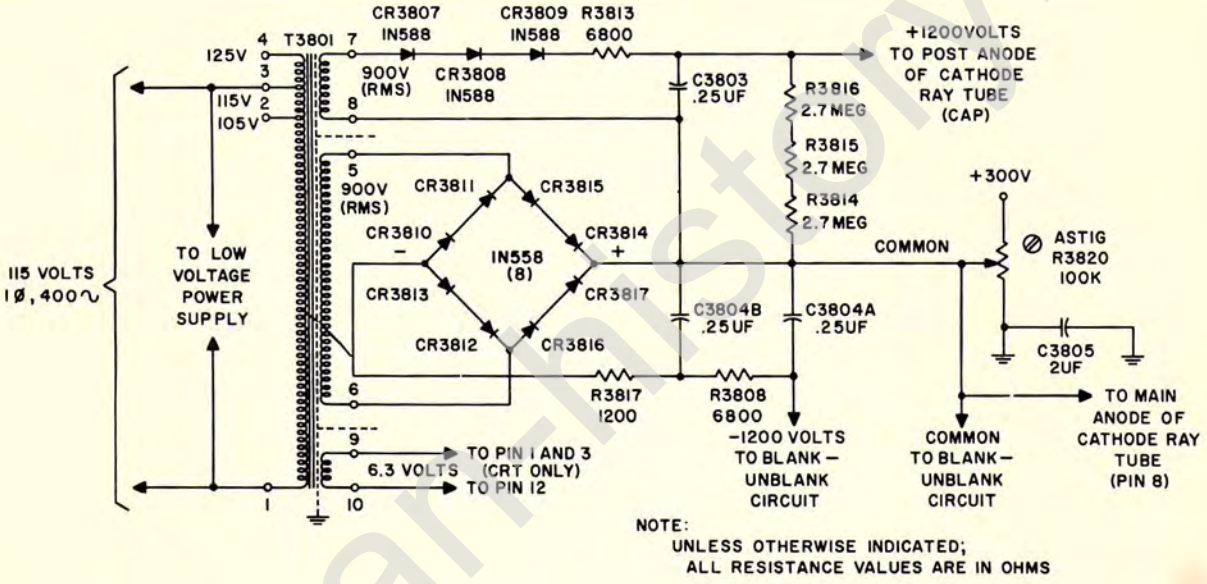


Figure 4-122. High Voltage Power Supply, Schematic Diagram