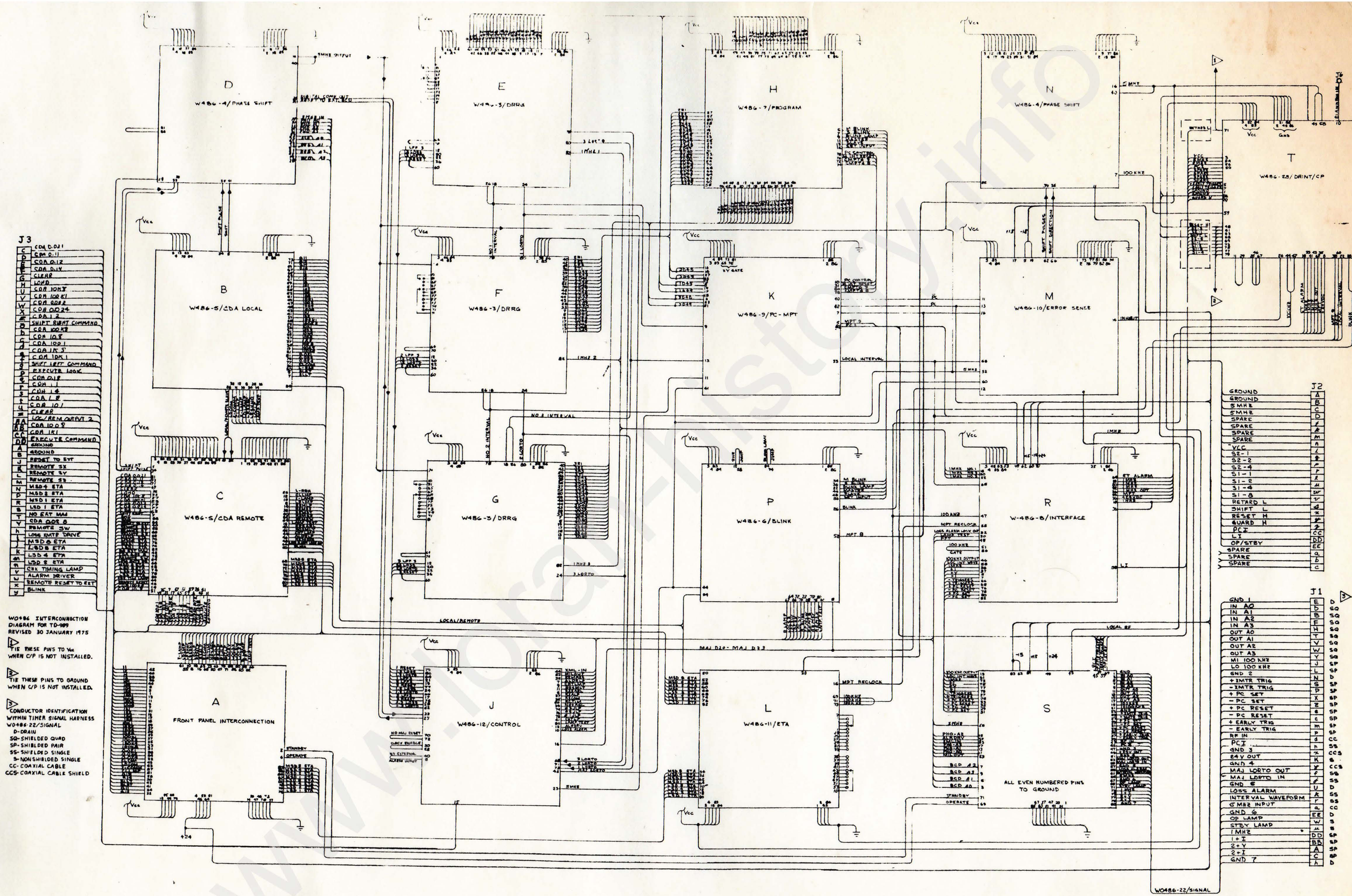
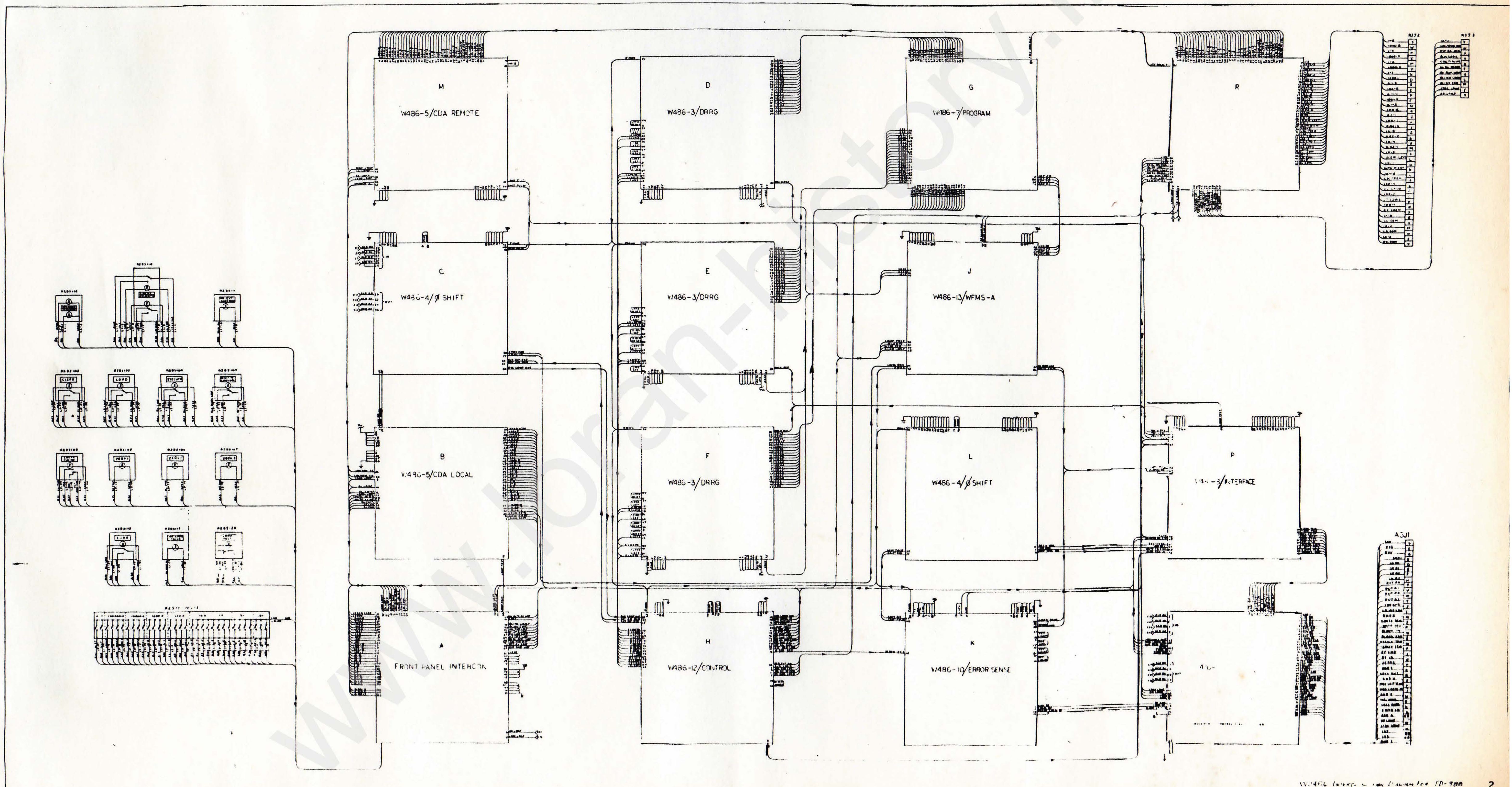
LORAN REPLACEMENT EQUIPMENT (LRE) ENGINEERING MANUAL

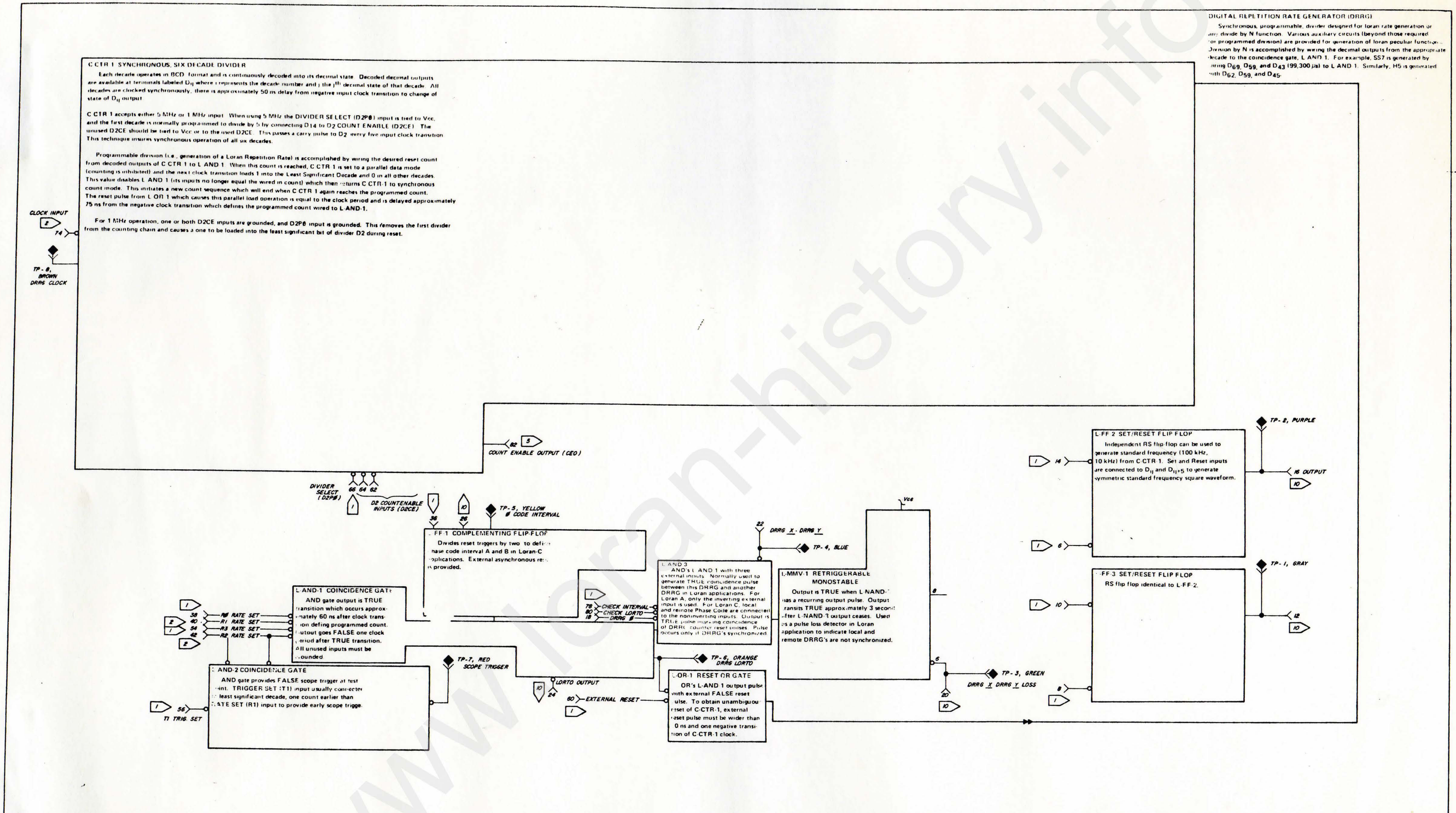
DEPARTMENT OF TRANSPORTATION
UNITED STATES COAST GUARD

UNCLASSIFIED

INDEX


WO486 INTERCONNECTION DIAGRAM FOR TD-989
REVISED 30 JANUARY 1975
1 TIE THESE PINS TO Vcc WHEN C/P IS NOT INSTALLED.
2 TIE THESE PINS TO GROUND WHEN C/P IS NOT INSTALLED.
3 CONDUCTOR IDENTIFICATION WITHIN TIMER SIGNAL HARNESS WO486-22/SIGNAL
D-DRAIN
SQ-SHIELDED QUAD
SP-SHIELDED PAIR
SS-SHIELDED SINGLE
S-NONSHIELDED SINGLE
CC-COAXIAL CABLE
CCS-COAXIAL CABLE SHIELD
D
W486-4/PHASE SHIFT
E
W486-3/DRRG
H
W486-7/PROGRAM
N
W486-4/PHASE SHIFT
T
W486-23/DRINT/CP
B
W486-5/CDA LOCAL
F
W486-3/DRRG
K
W486-9/PC-MPT
M
W486-10/ERROR SENSE
C
W486-5/CDA REMOTE
G
W486-3/DRRG
P
W486-6/BLINK
R
W-486-8/INTERFACE
A
FRONT PANEL INTERCONNECTION
J
W486-12/CONTROL
L
W486-11/ETA
S
ALL EVEN NUMBERED PINS TO GROUND
J3
J2
J1
WO486-22/SIGNAL
LOCAL/REMOTE
MAJ D20 - MAJ D33
LOCAL INTERVAL
NO 3 INTERVAL
GROUND
GROUND
5MHZ
5MHZ
VCC
RETARD L
SHIFT L
RESET H
GUARD H
PCI
LI
OP/STBY
IN A0
IN A1
IN A2
IN A3
OUT A0
OUT A1
OUT A2
OUT A3
MI 100 KHZ
LO 100 KHZ
RF IN
24V OUT
MAJ LORTO OUT
MAJ LORTO IN
LOSS ALARM
INTERVAL WAVEFORM
5MHZ INPUT
OP LAMP
STBY LAMP
CDA 0.021
CLEAR
LOAD
SHIFT RIGHT COMMAND
SHIFT LEFT COMMAND
EXECUTE LOCK
EXECUTE COMMAND
RESET TO EXT
CHK TIMING LAMP
ALARM DRIVER
REMOTE RESET TO EXT
BLINK


M
W486-5/CDA REMOTE
D
W486-3/DRRG
G
W486-7/PROGRAM
R
C
W486-4/Ø SHIFT
E
W486-3/DRRG
J
W486-13/WFMS-A
B
W486-5/CDA LOCAL
F
W486-3/DRRG
L
W486-4/Ø SHIFT
P
A
FRONT PANEL INTERCON
H
W486-12/CONTROL
K
W486-10/ERROR SENSE
A3J1



W0486-3/DRRG: DIGITAL REPETITION RATE GENERATOR (Dated: 3-23-70)

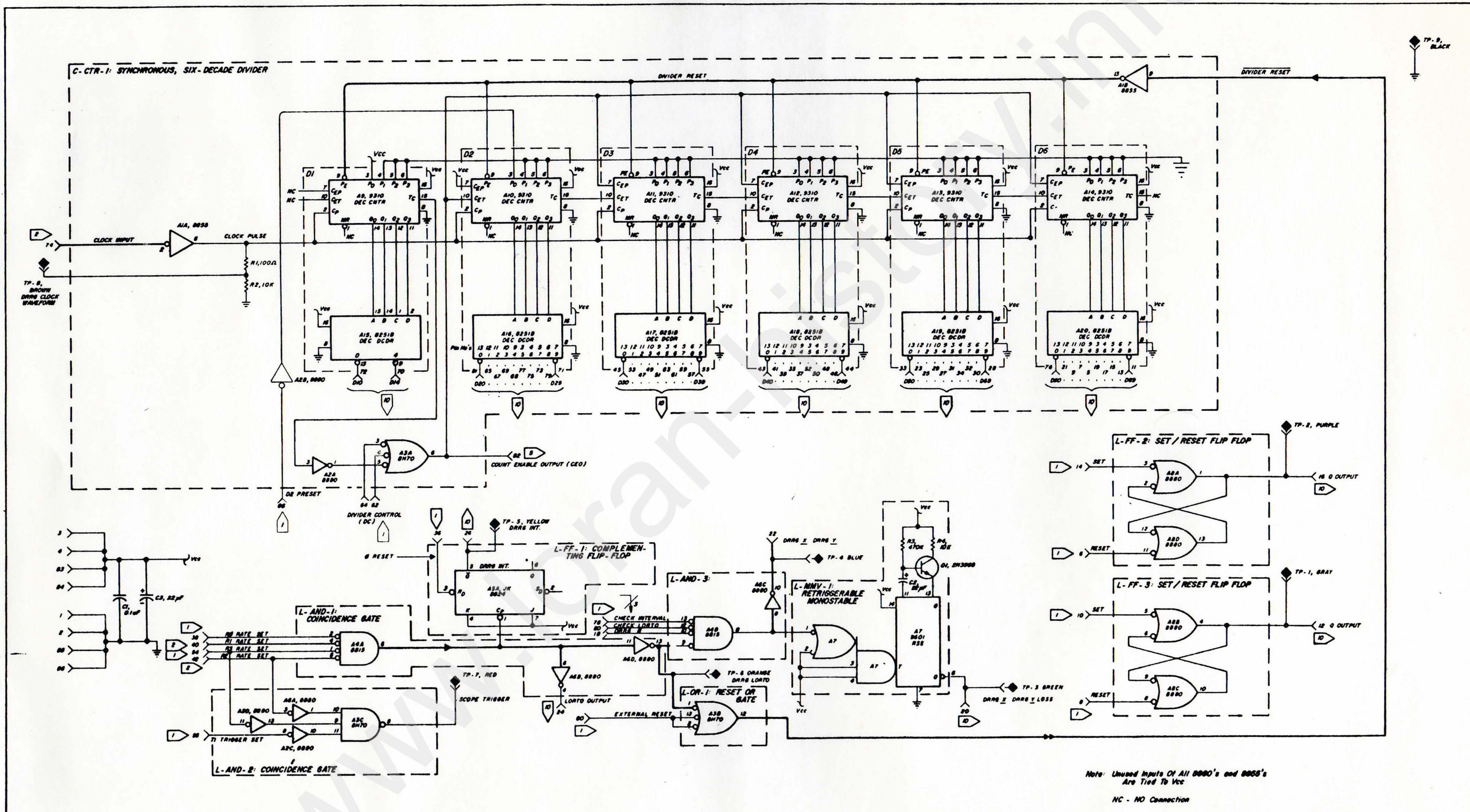
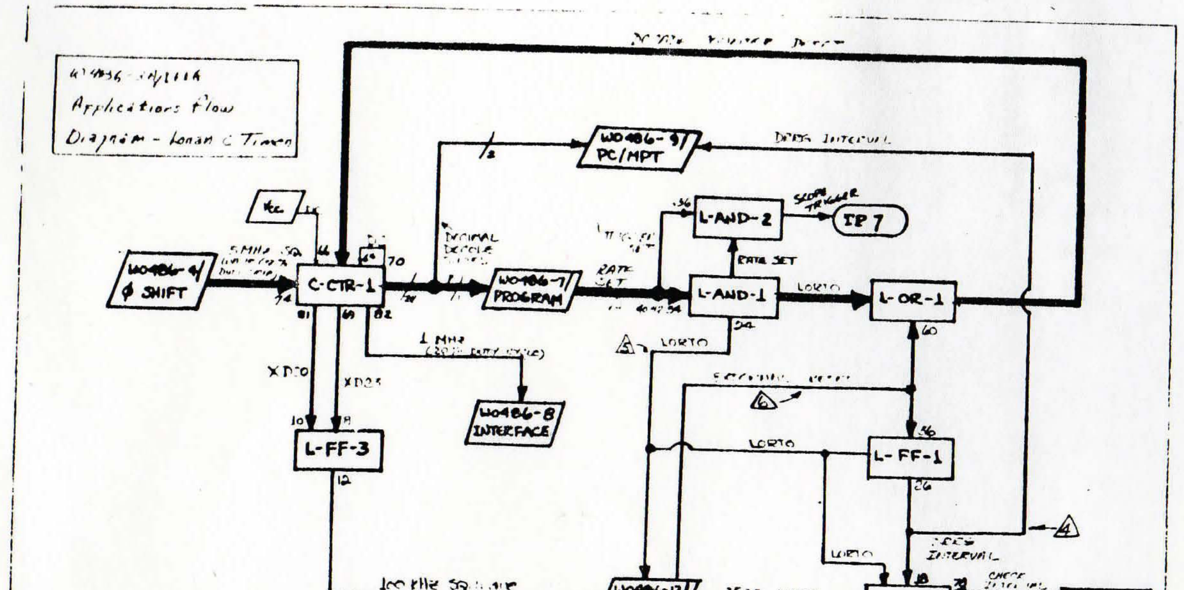
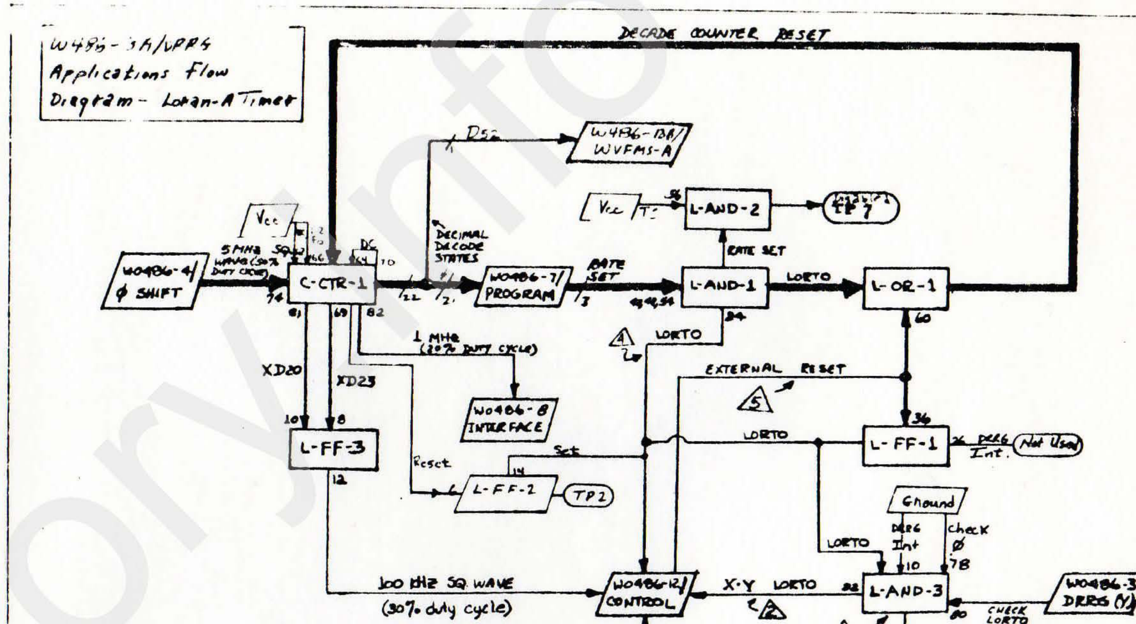


Figure E-2, (REVISED: 12-10-71) (REVISED 2-22-75)
WO486-3/DRRG DIGITAL REPETITION RATE GENERATOR (Dated 3-23-70)



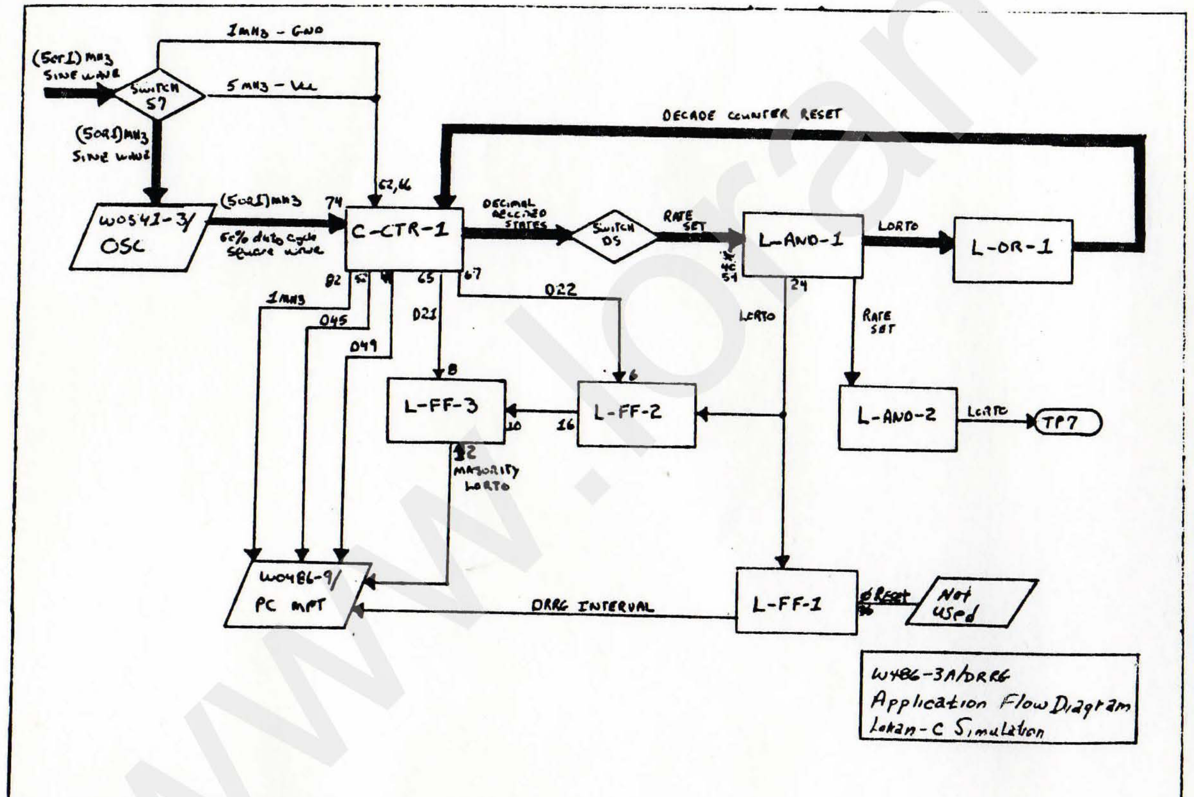
FLAG NOTES

1. Receives a LORTO and DRRG INTERVAL from one of the other two DRRG modules in the TD-988 timer. These waveforms are designated "CHECK LORTO" and "CHECK INTERVAL." They are compared for coincidence against the locally generated LORTO and DRRG INTERVAL.
2. X-Y LORTO waveform is the coincidence pulse mentioned under 1 above. A coincidence pulse indicates that both the LORTO and DRRG INTERVAL from both DRRG X and DRRG Y are in synchronization.
3. X-Y DRRG loss waveform supplied the logic waveform for detection of a malfunction of either DRRG X or DRRG Y.
4. DRRG INTERVAL = RATE = 1/2 GRR
5. LORTO Waveform - negative-going pulse 200 ns in duration.
6. REfer to W0486-3/DRRG Blocked Text diagram L-OR-1 section.



FLAG NOTES

1. Receives a LORTO from one of the other two DRRG modules in the TD-988 Timer. This waveform is designated "CHECK LORTO". It is compared for coincidence against the locally generated LORTO.
2. X-Y LORTO waveform is the coincidence pulse mentioned under 1 above. A coincidence pulse indicates that the LORTO from both DRRG X and DRRG Y are in synchronization.
3. X-Y DRRG lo waveform supplies the logic waveform for detection of a malfunction of either DRRG X or DRRF Y.
4. LORTO waveform - negative-going pulse 200 ns in duration.
5. Refer to W0486-3A/DRRG Block Text diagram L-OR-1 section.



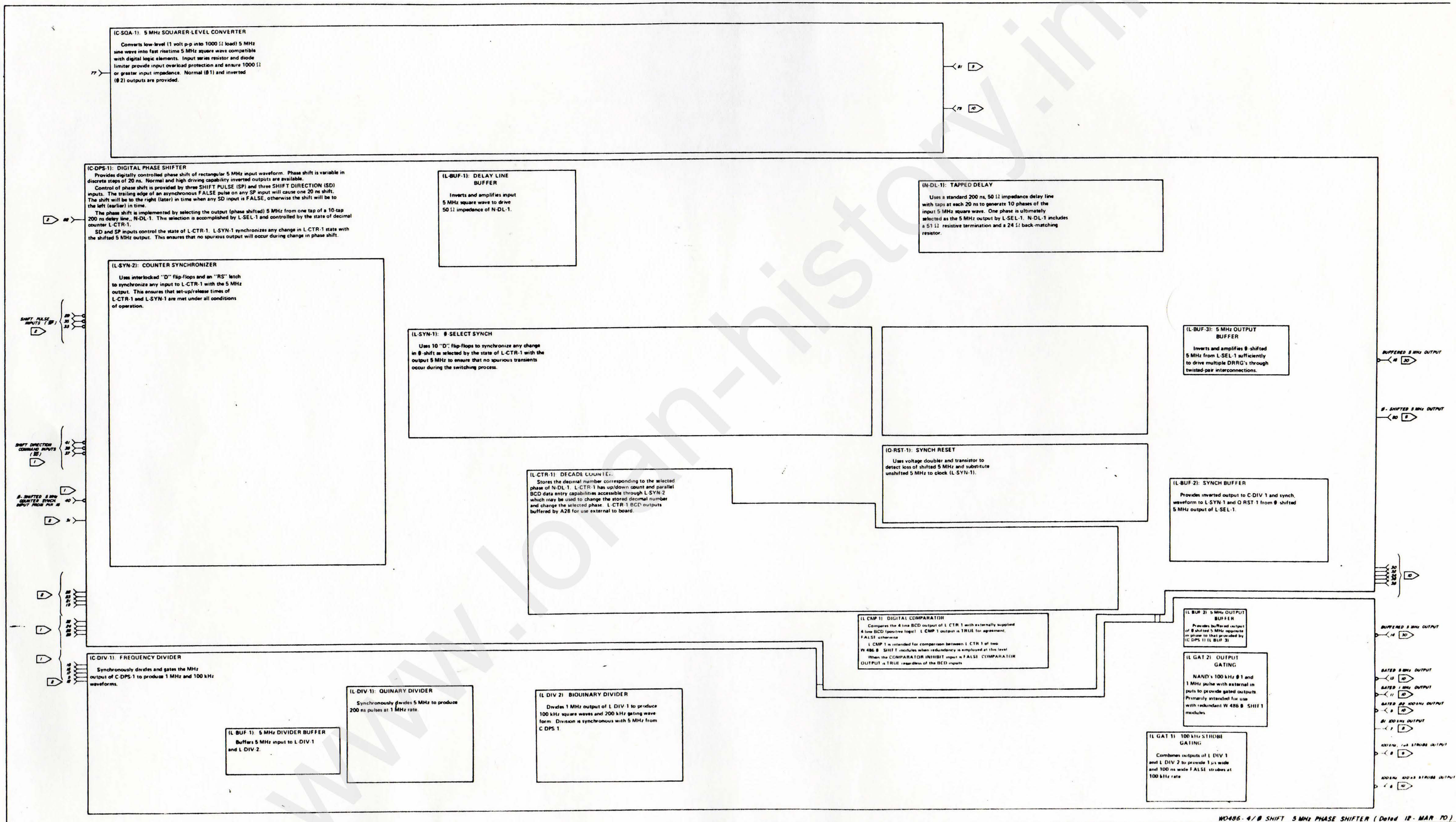
W0-486-3A1 DRRG (POWER REQUIREMENTS BASED ON MANUFACTURERS SPEC)

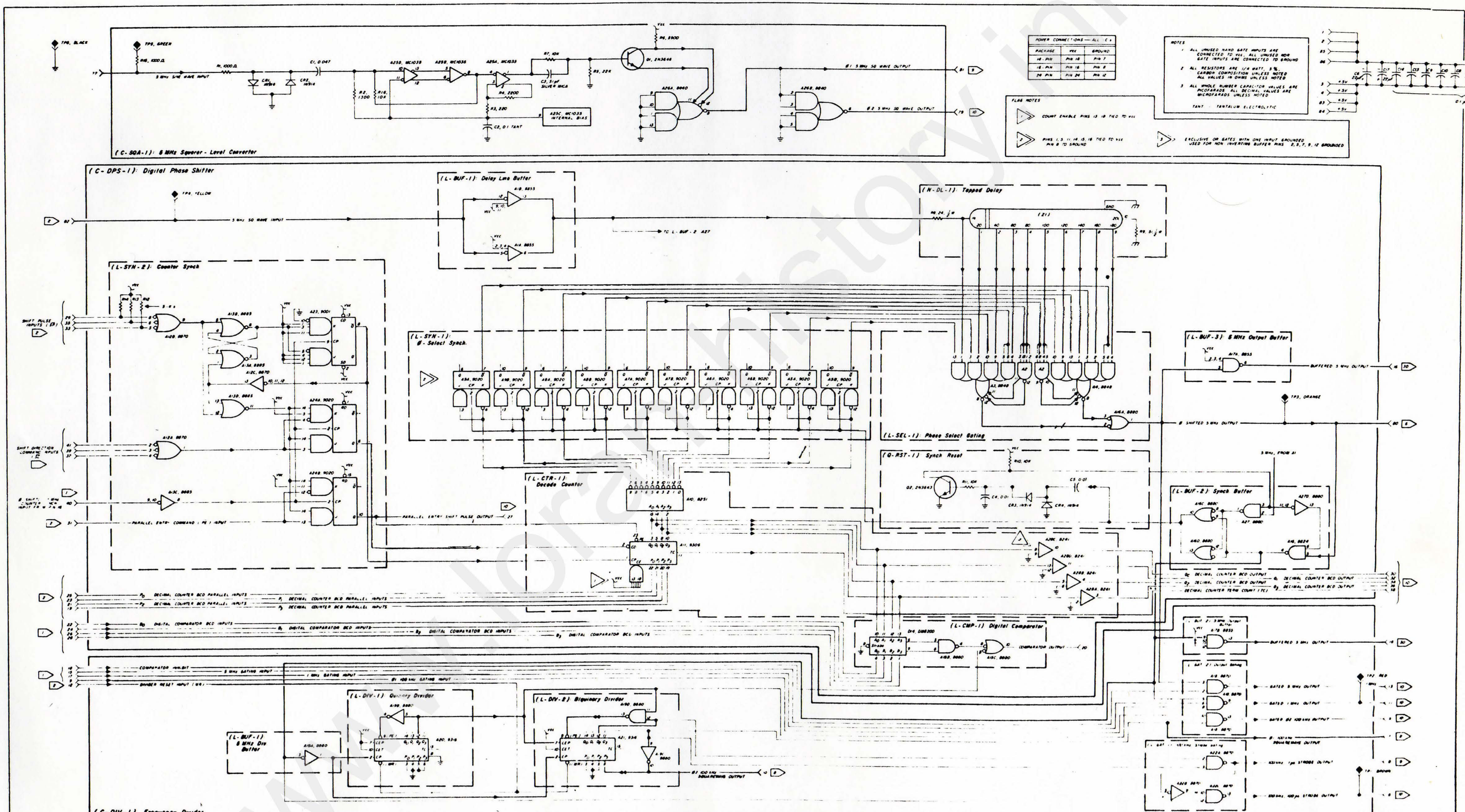
MFRS PREFIX	IC TYPE	MFRS SUFFIX	MFR	NO USED	POWER SUPPLY VCC PIN#	GND PIN#	CUR PER PACK	TOTAL CUR
N	8855	A	SIGNETICS	1	14	7	20.0	20.0
N	8880	A	SIGNETICS	3	14	7	14.0	42.0
N	8H70	A	SIGNETICS	1	14	7	26.0	26.0
N	8815	A	SIGNETICS	1	14	7	16.0	16.0
N	8824	B	SIGNETICS	1	16	8	25.0	25.0
U6A	9601	59X	FAIRCHILD	1	14	7	25.0	25.0
U6B	9310	59X	FAIRCHILD	6	16	8	70.0	420.0
N	8251	B	SIGNETICS	6	16	8	25.7	154.2

TOTAL PER BOARD 728.2

W0486-3A/DRRG

Supplemental Information


(C-SQA-1): 5 MHz SQUARER-LEVEL CONVERTER
Converts low-level (1 volt p-p into 1000 Ω load) 5 MHz sine wave into fast risetime 5 MHz square wave compatible with digital logic elements. Input series resistor and diode limiter provide input overload protection and ensure 1000 Ω or greater input impedance. Normal (θ1) and inverted (θ2) outputs are provided.
(C-DPS-1): DIGITAL PHASE SHIFTER
Provides digitally controlled phase shift of rectangular 5 MHz input waveform. Phase shift is variable in discrete steps of 20 ns. Normal and high driving capability inverted outputs are available.
Control of phase shift is provided by three SHIFT PULSE (SP) and three SHIFT DIRECTION (SD) inputs. The trailing edge of an asynchronous FALSE pulse on any SP input will cause one 20 ns shift. The shift will be to the right (later) in time when any SD input is FALSE, otherwise the shift will be to the left (earlier) in time.
The phase shift is implemented by selecting the output (phase shifted) 5 MHz from one tap of a 10-tap 200 ns delay line,, N-DL-1. This selection is accomplished by L-SEL-1 and controlled by the state of decimal counter L-CTR-1.
SD and SP inputs control the state of L-CTR-1. L-SYN-1 synchronizes any change in L-CTR-1 state with the shifted 5 MHz output. This ensures that no spurious output will occur during change in phase shift.
(L-BUF-1): DELAY LINE BUFFER
Inverts and amplifies input 5 MHz square wave to drive 50 Ω impedance of N-DL-1.
(N-DL-1): TAPPED DELAY
Uses a standard 200 ns, 50 Ω impedance delay line with taps at each 20 ns to generate 10 phases of the input 5 MHz square wave. One phase is ultimately selected as the 5 MHz output by L-SEL-1. N-DL-1 includes a 51 Ω resistive termination and a 24 Ω back-matching resistor.
(L-SYN-2): COUNTER SYNCHRONIZER
Uses interlocked "D" flip-flops and an "RS" latch to synchronize any input to L-CTR-1 with the 5 MHz output. This ensures that set-up/release times of L-CTR-1 and L-SYN-1 are met under all conditions of operation.
SHIFT PULSE INPUTS (3)
SHIFT DIRECTION COMMAND INPUTS (3)
(L-SYN-1): θ-SELECT SYNCH
Uses 10 "D" flip-flops to synchronize any change in θ-shift as selected by the state of L-CTR-1 with the output 5 MHz to ensure that no spurious transients occur during the switching process.
(L-BUF-3): 5 MHz OUTPUT BUFFER
Inverts and amplifies θ-shifted 5 MHz from L-SEL-1 sufficiently to drive multiple DRRG's through twisted-pair interconnections.
BUFFERED 5 MHz OUTPUT
θ-SHIFTED 5 MHz OUTPUT
(Q-RST-1): SYNCH RESET
Uses voltage doubler and transistor to detect loss of shifted 5 MHz and substitute unshifted 5 MHz to clock (L-SYN-1).
(L-CTR-1): DECADE COUNTER
Stores the decimal number corresponding to the selected phase of N-DL-1. L-CTR-1 has up/down count and parallel BCD data entry capabilities accessible through L-SYN-2 which may be used to change the stored decimal number and change the selected phase. L-CTR-1 BCD outputs buffered by A28 for use external to board.
(L-BUF-2): SYNCH BUFFER
Provides inverted output to C-DIV-1 and synch. waveform to L-SYN-1 and Q-RST-1 from θ-shifted 5 MHz output of L-SEL-1.
(L-CMP-1): DIGITAL COMPARATOR
Compares the 4 line BCD output of L-CTR-1 with externally supplied 4 line BCD (positive logic). L-CMP-1 output is TRUE for agreement, FALSE otherwise.
L-CMP-1 is intended for comparison between L-CTR-1 of two W 486 θ SHIFT modules when redundancy is employed at this level.
When the COMPARATOR INHIBIT input is FALSE, COMPARATOR OUTPUT is TRUE regardless of the BCD inputs.
(L-BUF-2): 5 MHz OUTPUT BUFFER
Provides buffered output of θ shifted 5 MHz opposite in phase to that provided by (C-DPS-1) (L-BUF-3).
(C-DIV-1): FREQUENCY DIVIDER
Synchronously divides and gates the MHz output of C-DPS-1 to produce 1 MHz and 100 kHz waveforms.
(L-DIV-1): QUINARY DIVIDER
Synchronously divides 5 MHz to produce 200 ns pulses at 1 MHz rate.
(L-DIV-2): BIQUINARY DIVIDER
Divides 1 MHz output of L-DIV-1 to produce 100 kHz square waves and 200 kHz gating waveform. Division is synchronous with 5 MHz from C-DPS-1.
(L-BUF-1): 5 MHz DIVIDER BUFFER
Buffers 5 MHz input to L-DIV-1 and L-DIV-2.
(L-GAT-2): OUTPUT GATING
NAND's 100 kHz θ1 and 1 MHz pulse with external inputs to provide gated outputs. Primarily intended for use with redundant W 486 θ SHIFT modules.
(L-GAT-1): 100 kHz STROBE GATING
Combines outputs of L-DIV-1 and L-DIV-2 to provide 1 μs wide and 100 ns wide FALSE strobes at 100 kHz rate.
BUFFERED 5 MHz OUTPUT
GATED 5 MHz OUTPUT
GATED 1 MHz OUTPUT
GATED θ2 100 kHz OUTPUT
θ1 100 kHz OUTPUT
100 kHz, 1 μs STROBE OUTPUT
100 kHz, 100 ns STROBE OUTPUT
W0486 - 4/θ SHIFT 5 MHz PHASE SHIFTER (Dated 12-MAR-70)



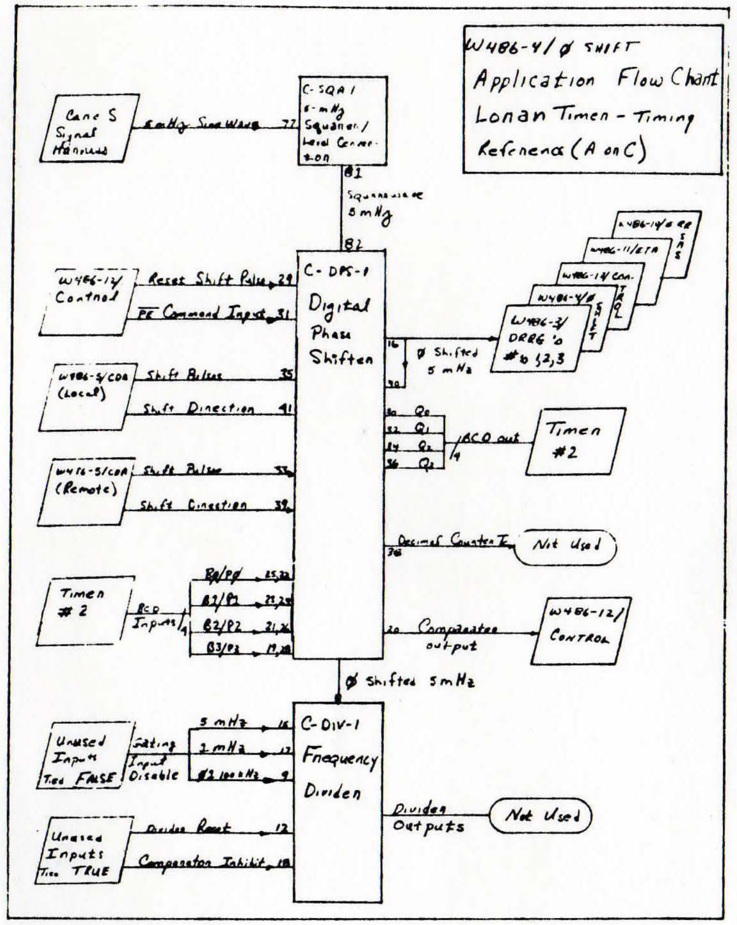
WO486-4/Ø SHIFT 5 MHz PHASE SHIFTER (Dated 12-MAR-70)

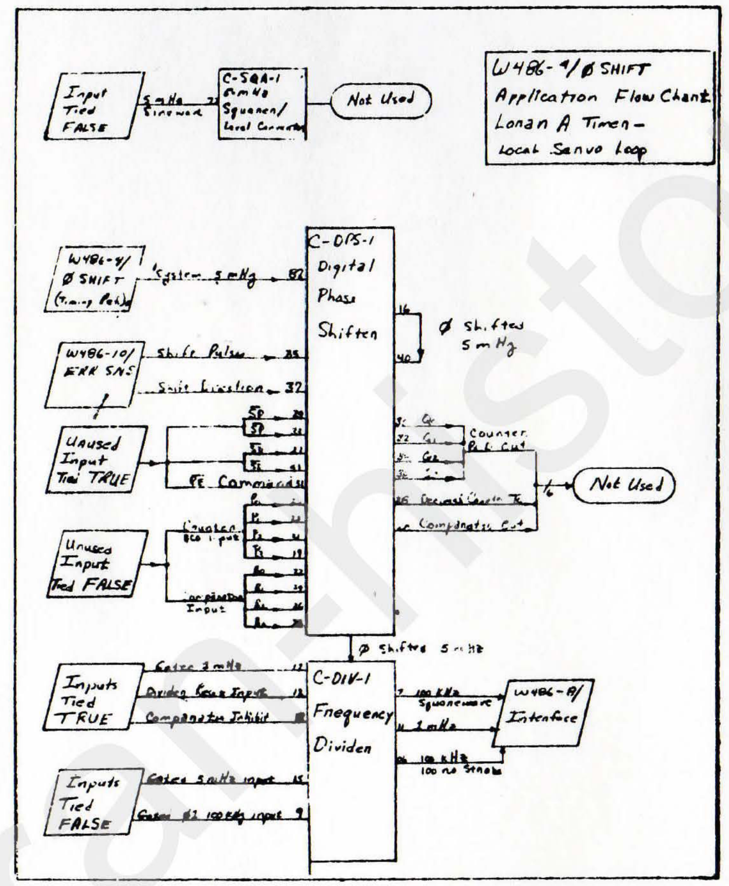
7

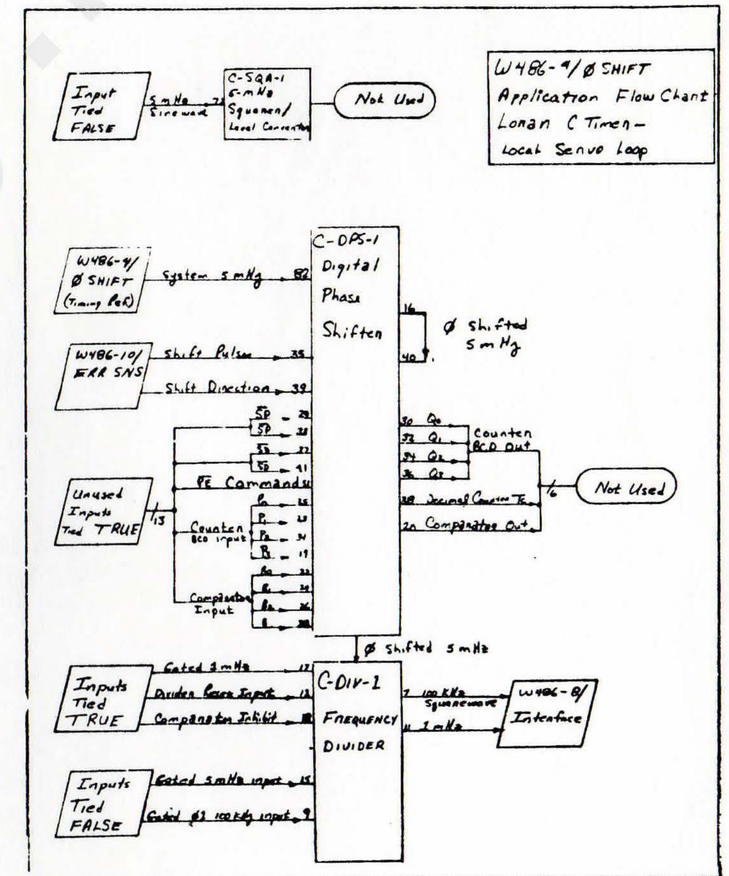
(REVISED 2-22-75) (REVISED 12-10-71)

Figure 1-4

ORIGINAL





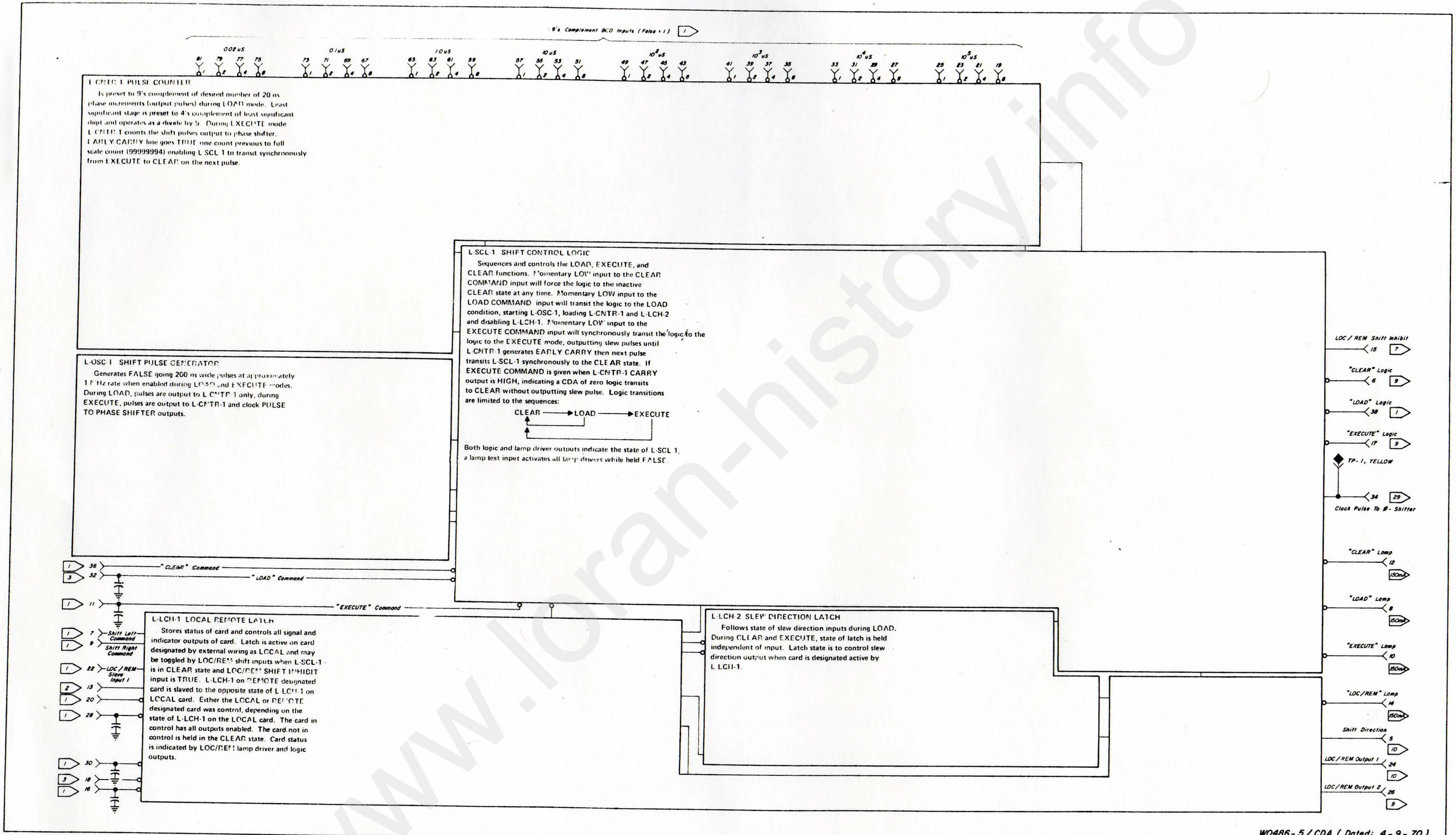


WC 486-4/Ø-SHIFT (POWER REQUIREMENTS BASED ON MANUFACTURERS SPEC) -

MFRS PREFIX	I.C TYPE	MFRS SUFIX	MFR	NO USED	POWER SUPPLY VCC PIN #	GND PIN #	CUR PER PACK	TOTAL CUR
N	8855	A	SIGNETICS	2	14	7	20.0	48.0
N	8806	A	SIGNETICS	1	14	7	3.4	3.4
N	8848	A	SIGNETICS	2	14	7	8.0	16.0
U7B	9020	59X	FAIRCHILD	6	16	8	28.0	168.0
N	8251	B	SIGNETICS	1	16	8	25.7	25.7
U6N	9306	59X	FAIRCHILD	1	24	12	70.0	70.0
N	8870	A	SIGNETICS	3	14	7	17.7	53.1
N	3885	A	SIGNETICS	1	14	7	20.0	20.0
DM	8200	-	NATIONAL	1	14	7	50.0	50.0
N	8880	A	SIGNETICS	4	14	7	14.0	56.0
U7B	9316	59X	FAIRCHILD	2	16	8	70.0	140.0
U6A	9001	59X	FAIRCHILD	1	14	7	19.0	19.0
MC	1035	P	MOTOROLA	1	14	7	30.0	30.0
N	8840	A	SIGNETICS	1	14	7	11.0	11.0
N	8241	A	SIGNETICS	1	14	7	40.0	40.0

TOTAL
PER BOARD
777.2

W0486-4/Ø SHIFT DIGITAL PHASE SHIFTER
Supplemental Information 12-10-71


9's Complement BCD Inputs (False = 1)
.002 uS
0.1 uS
1.0 uS
10 uS
10^2 uS
10^3 uS
10^4 uS
10^5 uS
L-CNTR-1 PULSE COUNTER
Is preset to 9's complement of desired number of 20 ns phase increments (output pulses) during LOAD mode. Least significant stage is preset to 4's complement of least significant digit and operates as a divide by 5. During EXECUTE mode L-CNTR-1 counts the shift pulses output to phase shifter. EARLY CARRY line goes TRUE one count previous to full scale count (99999994) enabling L-SCL-1 to transit synchronously from EXECUTE to CLEAR on the next pulse.
L-OSC-1 SHIFT PULSE GENERATOR
Generates FALSE going 200 ns wide pulses at approximately 1 MHz rate when enabled during LOAD and EXECUTE modes. During LOAD, pulses are output to L-CNTR-1 only, during EXECUTE, pulses are output to L-CNTR-1 and clock PULSE TO PHASE SHIFTER outputs.
L-SCL-1 SHIFT CONTROL LOGIC
Sequences and controls the LOAD, EXECUTE, and CLEAR functions. Momentary LOW input to the CLEAR COMMAND input will force the logic to the inactive CLEAR state at any time. Momentary LOW input to the LOAD COMMAND input will transit the logic to the LOAD condition, starting L-OSC-1, loading L-CNTR-1 and L-LCH-2 and disabling L-LCH-1. Momentary LOW input to the EXECUTE COMMAND input will synchronously transit the logic to the logic to the EXECUTE mode, outputting slew pulses until L-CNTR-1 generates EARLY CARRY then next pulse transits L-SCL-1 synchronously to the CLEAR state. If EXECUTE COMMAND is given when L-CNTR-1 CARRY output is HIGH, indicating a CDA of zero logic transits to CLEAR without outputting slew pulse. Logic transitions are limited to the sequences:
CLEAR → LOAD → EXECUTE
Both logic and lamp driver outputs indicate the state of L-SCL-1, a lamp test input activates all lamp drivers while held FALSE.
L-LCH-1 LOCAL REMOTE LATCH
Stores status of card and controls all signal and indicator outputs of card. Latch is active on card designated by external wiring as LOCAL and may be toggled by LOC/REM shift inputs when L-SCL-1 is in CLEAR state and LOC/REM SHIFT INHIBIT input is TRUE. L-LCH-1 on REMOTE designated card is slaved to the opposite state of L-LCH-1 on LOCAL card. Either the LOCAL or REMOTE designated card was control, depending on the state of L-LCH-1 on the LOCAL card. The card in control has all outputs enabled. The card not in control is held in the CLEAR state. Card status is indicated by LOC/REM lamp driver and logic outputs.
L-LCH-2 SLEW DIRECTION LATCH
Follows state of slew direction inputs during LOAD. During CLEAR and EXECUTE, state of latch is held independent of input. Latch state is to control slew direction output when card is designated active by L-LCH-1.
"CLEAR" Command
"LOAD" Command
"EXECUTE" Command
Shift Left Command
Shift Right Command
LOC / REM Slave Input 1
LOC / REM Shift Inhibit
"CLEAR" Logic
"LOAD" Logic
"EXECUTE" Logic
TP-1, YELLOW
Clock Pulse To Ø-Shifter
"CLEAR" Lamp
"LOAD" Lamp
"EXECUTE" Lamp
"LOC/REM" Lamp
150mA
Shift Direction
LOC/REM Output 1
LOC/REM Output 2
W0486-5 / CDA (Dated: 4-9-70)

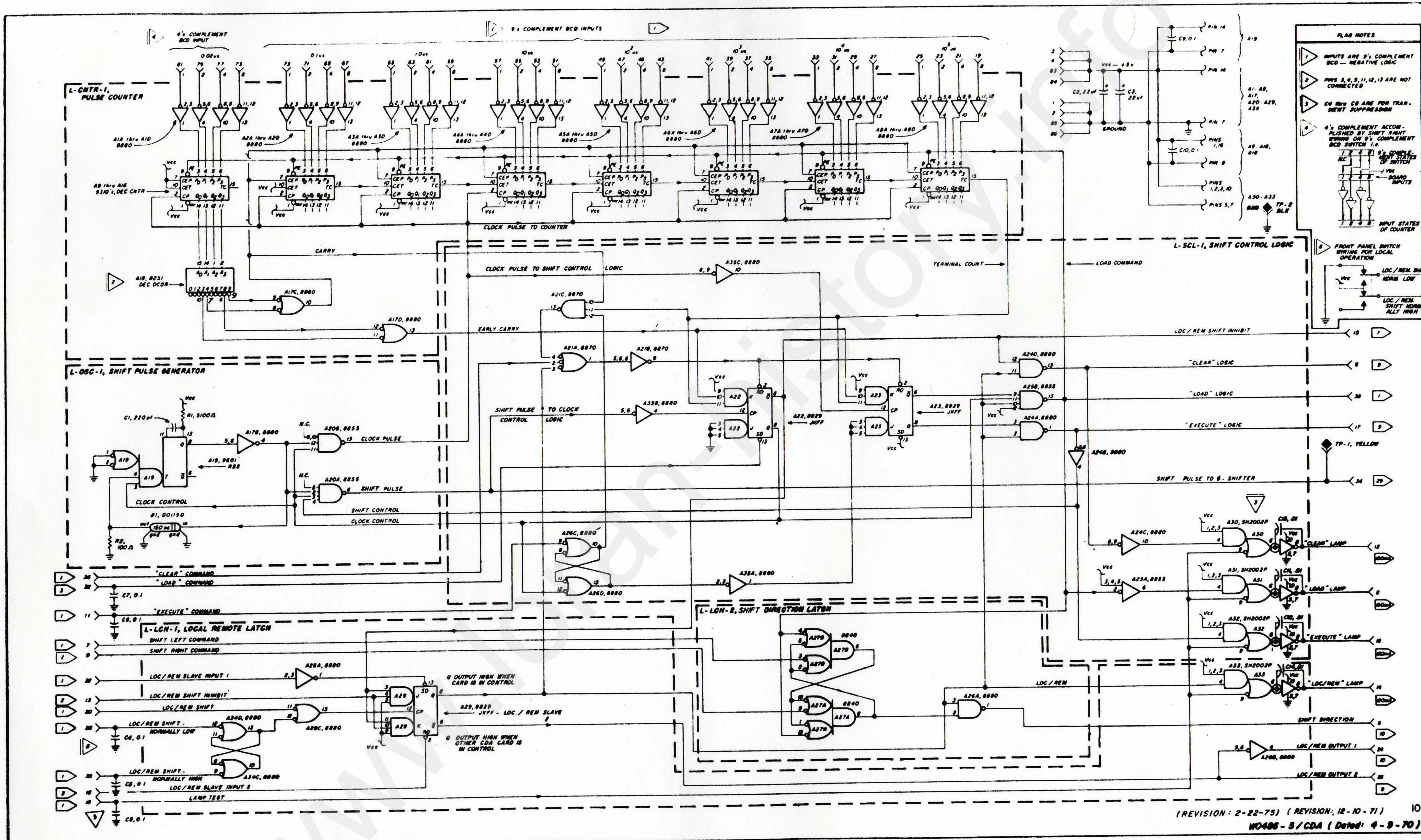
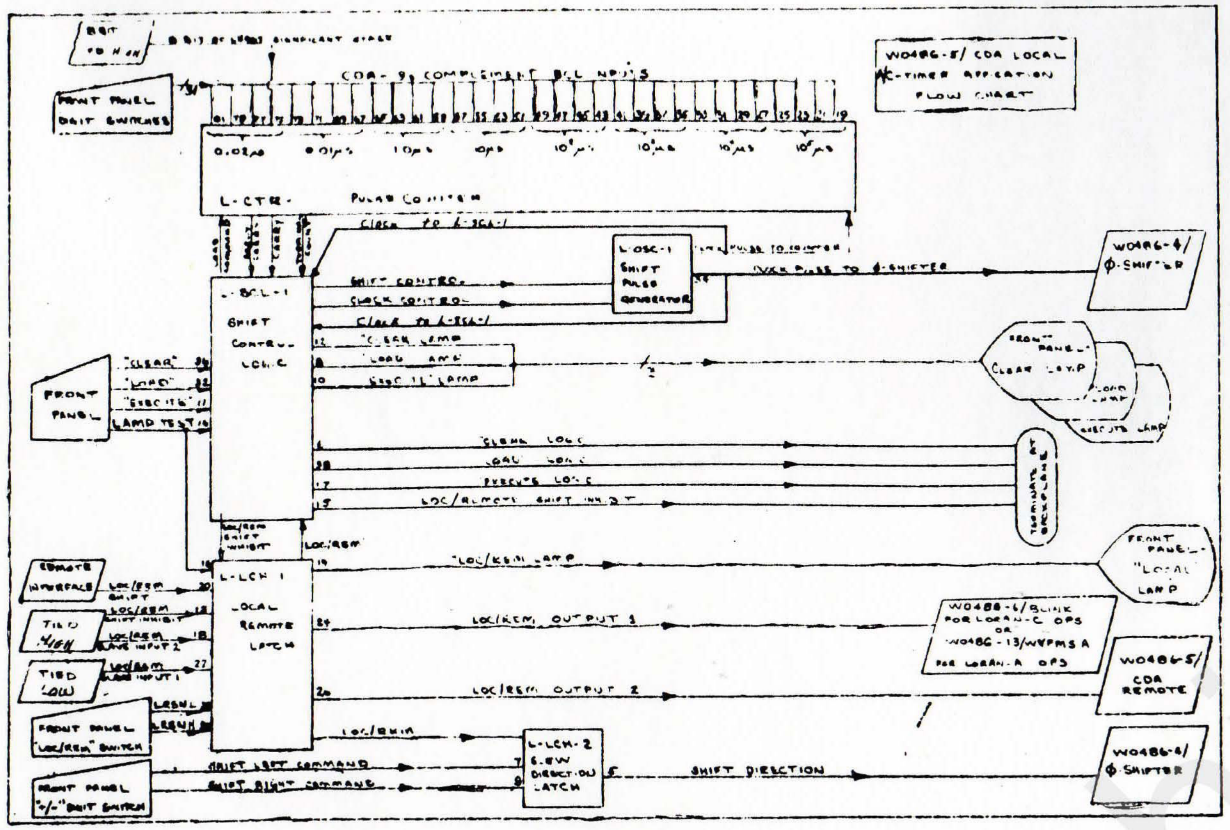
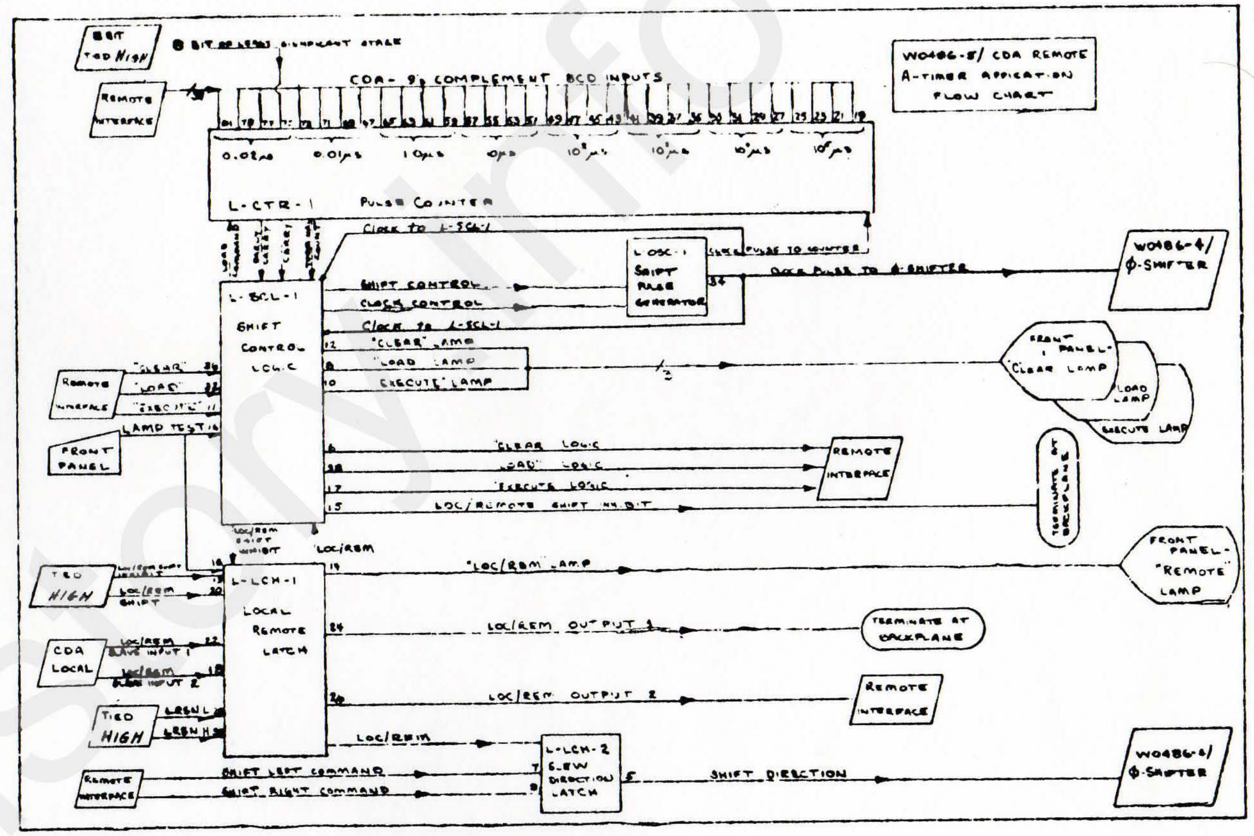
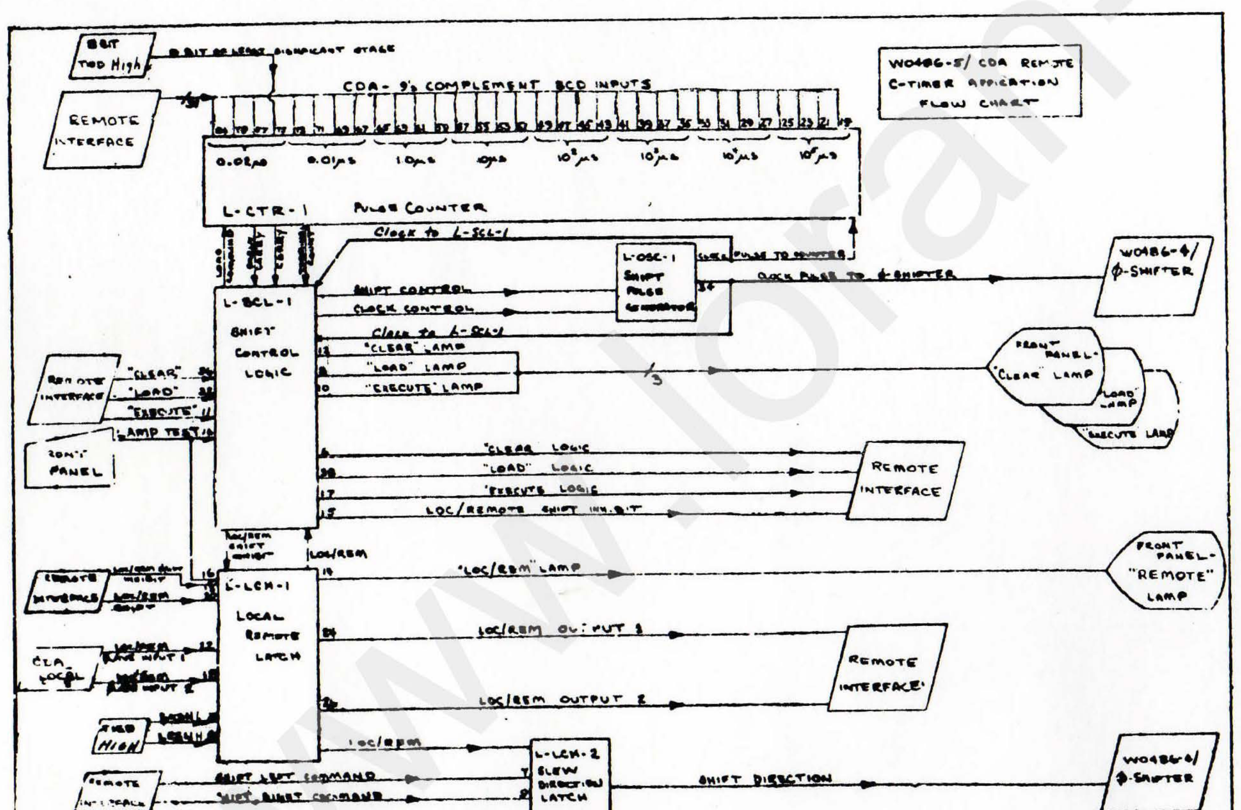


Figure E-6

ORIGINAL





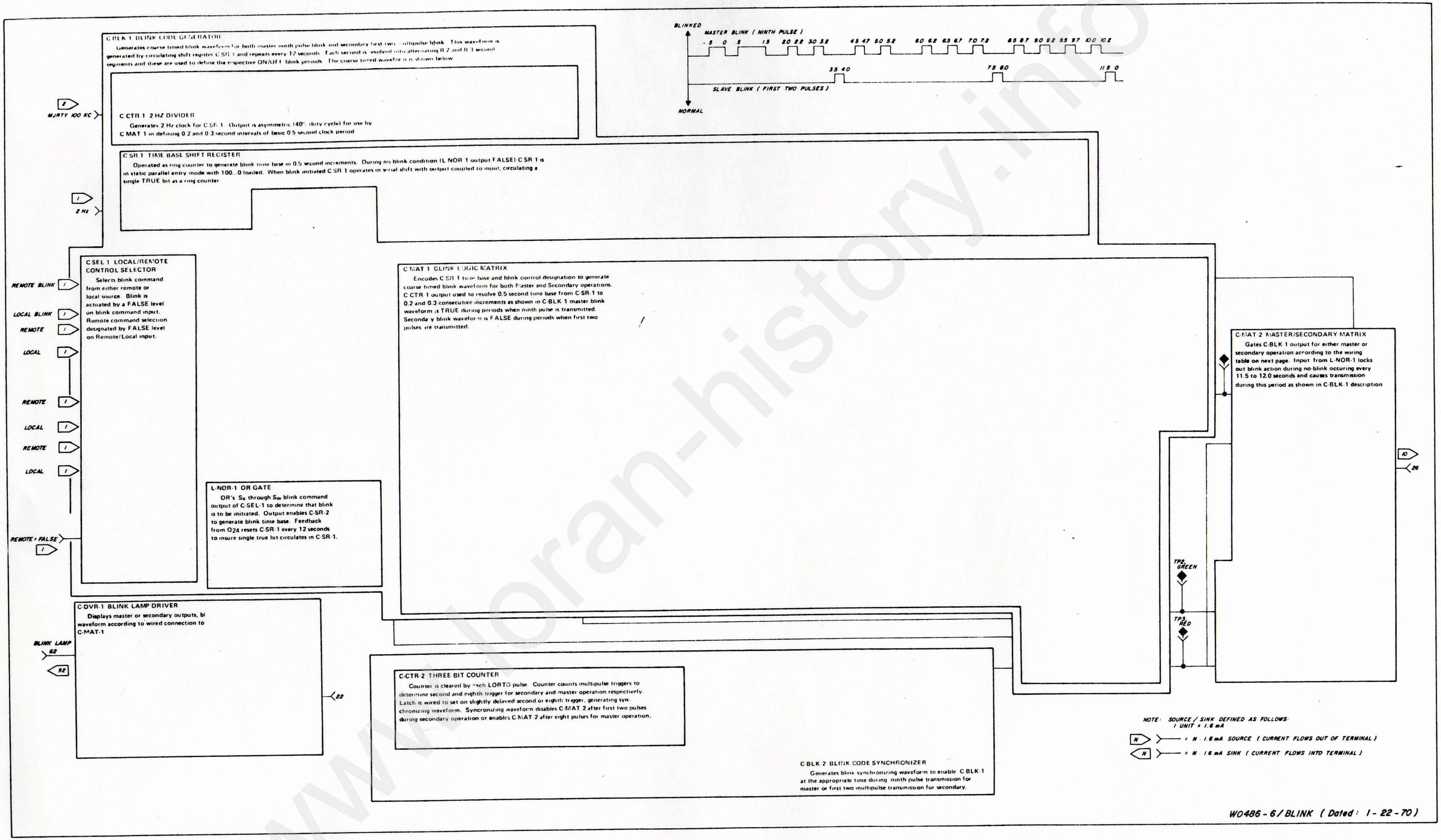


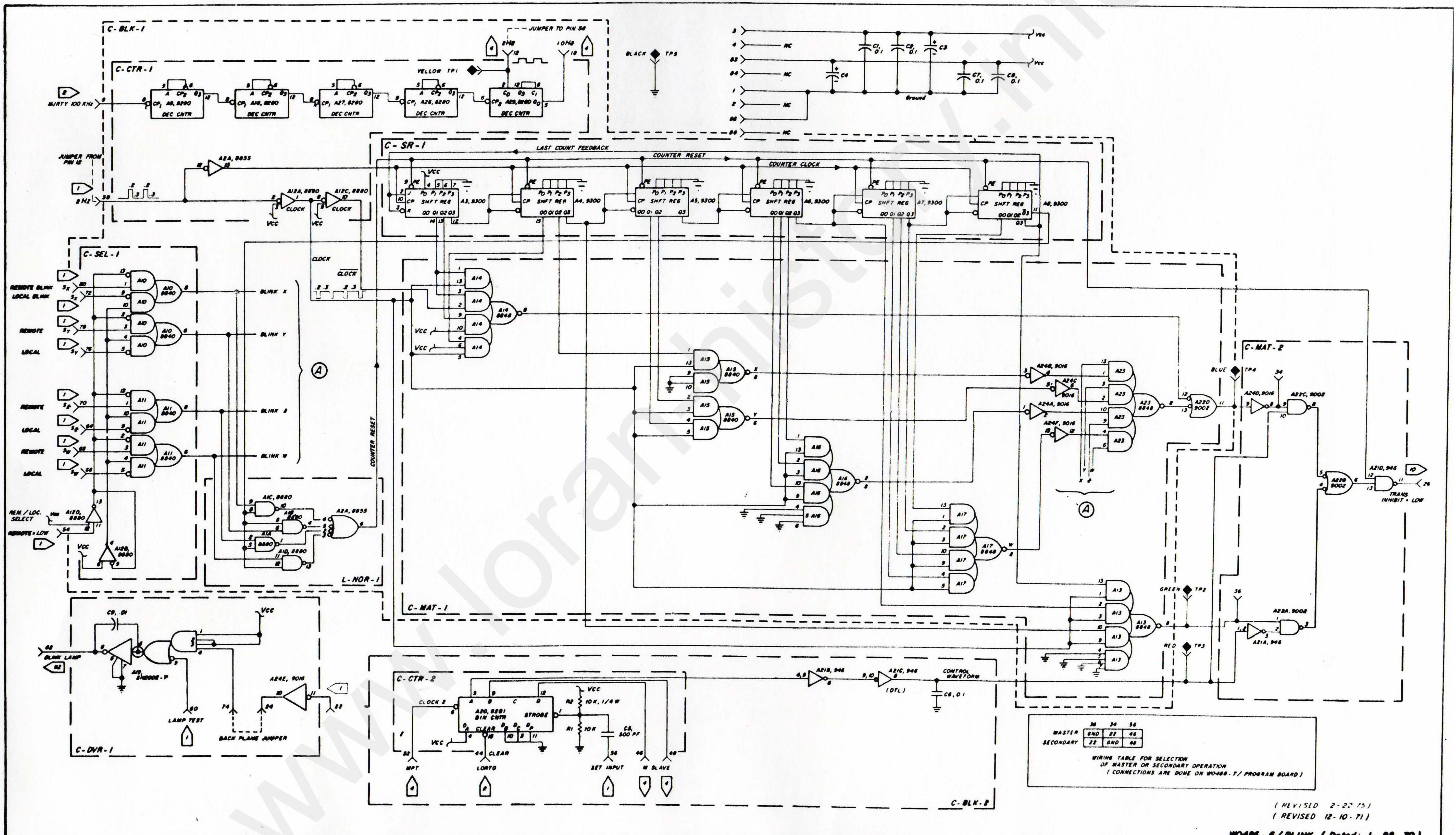
WO-486-5A/CDA (POWER REQUIREMENTS BASED ON MANUFACTURERS SPEC)

MFRS PREFIX	IC TYPE	MFRS SUFIX	MANFRS	NO USED	POWER SUPPLY VCC PIN#	GND PIN#	CUR PER PACK	TOTAL CUR
N	8880	A	SIGNETICS	14	14	7	14.0	196.0
U6B	9310	59X	FAIRCHILD	8	16	8	70.0	560.0
N	8251	B	SIGNETICS	1	16	8	25.7	25.7
U6A	9601	59X	FAIRCHILD	1	14	7	25.0	25.0
N	8855	A	SIGNETICS	2	14	7	20.0	40.0
N	8870	A	SIGNETICS	1	4	11	12.7	12.7
N	8829	A	SIGNETICS	3	14	7	22.0	66.0
H6F	2002	9XX	FAIRCHILD	4	10	5	30.0	120.0

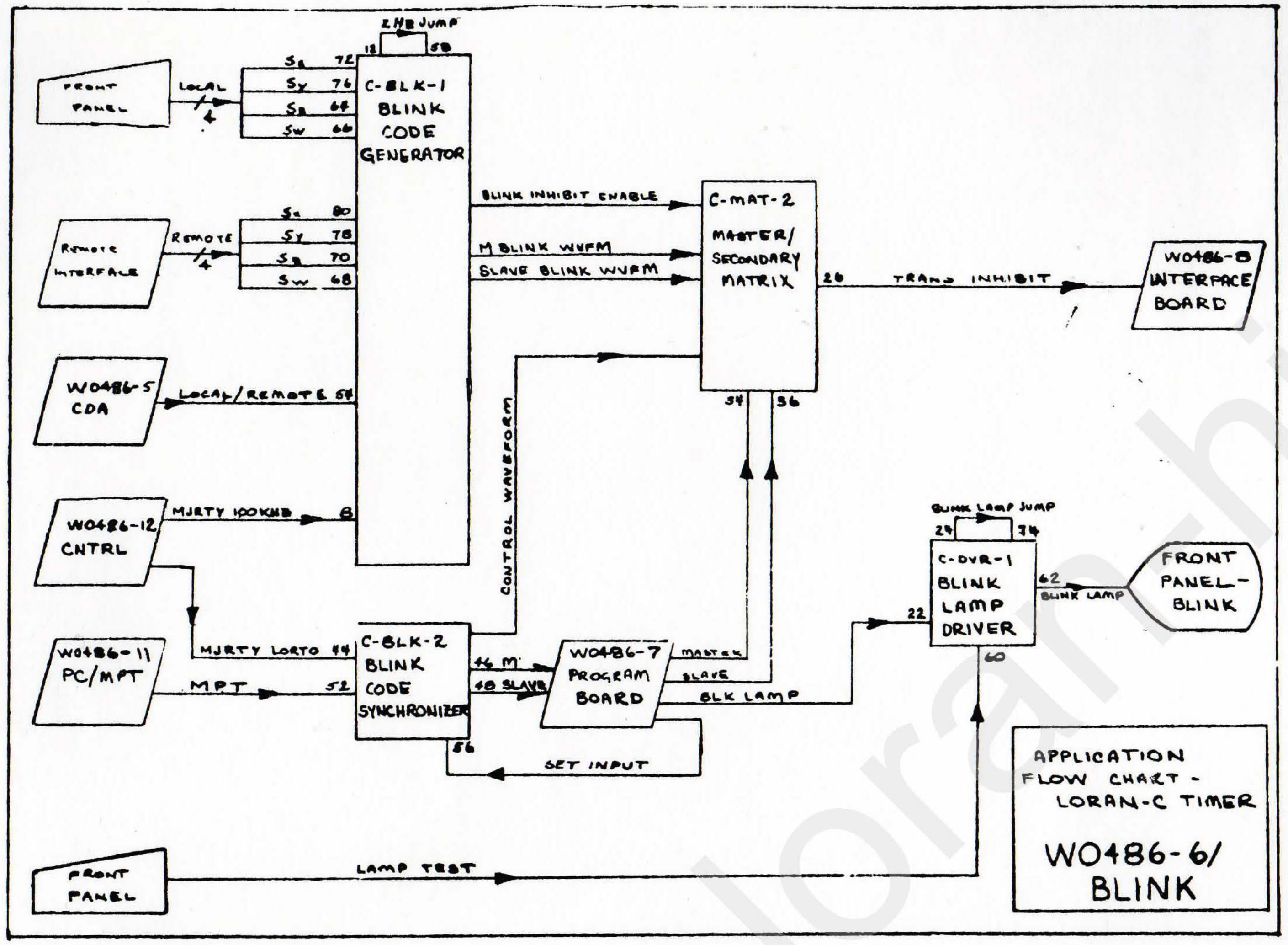
TOTAL PER BOARD 1050.4 MA

W0486-5/CDA Coding Delay Adjust
12-10-71
Supplemental Information


C BLK 1 BLINK CODE GENERATOR
Generates coarse timed blink waveform for both master ninth pulse blink and secondary first two multipulse blink. This waveform is generated by circulating shift register C SR 1 and repeats every 12 seconds. Each second is resolved into alternating 0.2 and 0.3 second segments and these are used to define the respective ON/OFF blink periods. The coarse timed waveform is shown below.
BLINKED
MASTER BLINK (NINTH PULSE)
-.5 0 .5 1.5 2.0 2.2 3.0 3.2 4.5 4.7 5.0 5.2 6.0 6.2 6.5 6.7 7.0 7.2 8.5 8.7 9.0 9.2 9.5 9.7 10.0 10.2
3.5 4.0 7.5 8.0 11.5 0
SLAVE BLINK (FIRST TWO PULSES)
NORMAL
MJRTY 100 KC
C CTR 1 2 HZ DIVIDER
Generates 2 Hz clock for C SR 1. Output is asymmetric (40% duty cycle) for use by C MAT 1 in defining 0.2 and 0.3 second intervals of basic 0.5 second clock period.
2 Hz
C SR 1 TIME BASE SHIFT REGISTER
Operated as ring counter to generate blink time base in 0.5 second increments. During no blink condition (L NOR 1 output FALSE) C SR 1 is in static parallel entry mode with 100...0 loaded. When blink initiated C SR 1 operates in serial shift with output coupled to input, circulating a single TRUE bit as a ring counter.
C SEL 1 LOCAL/REMOTE CONTROL SELECTOR
Selects blink command from either remote or local source. Blink is actuated by a FALSE level on blink command input. Remote command selection designated by FALSE level on Remote/Local input.
REMOTE BLINK
LOCAL BLINK
REMOTE
LOCAL
REMOTE
LOCAL
REMOTE
LOCAL
REMOTE = FALSE
L-NOR-1 OR GATE
OR's S_X through S_W blink command output of C-SEL-1 to determine that blink is to be initiated. Output enables C-SR-2 to generate blink time base. Feedback from Q_{24} resets C-SR-1 every 12 seconds to insure single true bit circulates in C-SR-1.
C MAT 1 BLINK LOGIC MATRIX
Encodes C SR 1 time base and blink control designation to generate coarse timed blink waveform for both Master and Secondary operations. C CTR 1 output used to resolve 0.5 second time base from C-SR-1 to 0.2 and 0.3 consecutive increments as shown in C-BLK-1 master blink waveform is TRUE during periods when ninth pulse is transmitted. Secondary blink waveform is FALSE during periods when first two pulses are transmitted.
C-MAT-2 MASTER/SECONDARY MATRIX
Gates C-BLK-1 output for either master or secondary operation according to the wiring table on next page. Input from L-NOR-1 locks out blink action during no-blink occuring every 11.5 to 12.0 seconds and causes transmission during this period as shown in C-BLK-1 description
TP2 GREEN
TP3 RED
C-DVR-1 BLINK LAMP DRIVER
Displays master or secondary outputs, bl waveform according to wired connection to C-MAT-1
BLINK LAMP
62
92
22
C-CTR-2 THREE BIT COUNTER
Counter is cleared by each LORTO pulse. Counter counts multipulse triggers to determine second and eighth trigger for secondary and master operation respectively. Latch is wired to set on slightly delayed second or eighth trigger, generating synchronizing waveform. Syncronizing waveform disables C-MAT-2 after first two pulses during secondary operation or enables C-MAT-2 after eight pulses for master operation.
C-BLK-2 BLINK CODE SYNCHRONIZER
Generates blink synchronizing waveform to enable C-BLK-1 at the appropriate time during ninth pulse transmission for master or first two multipulse transmission for secondary.
NOTE: SOURCE / SINK DEFINED AS FOLLOWS:
1 UNIT = 1.6 mA
N = N · 1.6 mA SOURCE (CURRENT FLOWS OUT OF TERMINAL)
N = N · 1.6 mA SINK (CURRENT FLOWS INTO TERMINAL)
W0486-6/BLINK (Dated: 1-22-70)


C-BLK-1
C-CTR-1
C-SR-1
C-SEL-1
L-NOR-1
C-MAT-1
C-MAT-2
C-DVR-1
C-CTR-2
C-BLK-2
JUMPER TO PIN 58
YELLOW TP1
BLACK TP5
BLUE TP4
GREEN TP2
RED TP3
LAST COUNT FEEDBACK
COUNTER RESET
COUNTER CLOCK
SHFT REG
DEC CNTR
BIN CNTR
STROBE
CLOCK
BLINK X
BLINK Y
BLINK Z
BLINK W
REMOTE BLINK
LOCAL BLINK
REMOTE
LOCAL
REM./LOC. SELECT
REMOTE = LOW
BLINK LAMP
LAMP TEST
BACK PLANE JUMPER
CONTROL WAVEFORM
(DTL)
SET INPUT
M SLAVE
LORTO
TRANS INHIBIT = LOW
Ground
MASTER
SECONDARY
WIRING TABLE FOR SELECTION OF MASTER OR SECONDARY OPERATION
(CONNECTIONS ARE DONE ON W0486-7/ PROGRAM BOARD)
(REVISED 2-22-73)
(REVISED 12-10-71)
W0486-6/BLINK (Dated: 1-22-70)

ORIGINAL



WO 486-6A /BLINK

MFRS PREFIX	IC TYPE	MFRS SUFFIX	MFR.	NO. USED	POWER SUPPLY Vcc PIN #	GND PIN #	CURRENT PER PACK	TOTAL CUR
N	8880	A	SIGNETICS	2	14	7	14.0	28.0
N	8855	A	SIGNETICS	1	14	7	20.0	20.0
U6B	9300	59X	FAIRCHILD	6	16	8	70.0	420.0
N	8280	A	SIGNETICS	5	14	7	35.0	175.0
N	8840	A	SIGNETICS	3	14	7	11.0	33.0
N	8848	A	SIGNETICS	5	14	7	8.0	40.0
H6F	2002	9XX	FAIRCHILD	1	10	5	30.0	30.0
N	8281	A	SIGNETICS	1	14	7	35.0	35.0
U6A	9946	59X	FAIRCHILD	1	14	7	13.0	13.0
U6A	9002	59X	FAIRCHILD	1	14	7	15.0	15.0
U6A	9016	59X	FAIRCHILD	1	14	7	28.0	28.0

TOTAL PER BOARD 845.0

W0486-6/BLINK 12-10-71

Supplemental Information

C-REC-1 RECORDER CHANNEL 1 PHASE COMPARATOR

Generates DC output proportional to the phase lead between the FALSE going edge of the VARIABLE input and the selected edge of the majority of the REFERENCE inputs. Output corresponding to 0-360 degrees of phase lead is 0-1 mA through 4k or less floating load and 0-8V into 50k or greater grounded load. CHART POSITIONING switch selects FALSE going edge of REFERENCE as phase standard when in NORMAL position or TRUE going edge when in RECENTER position, allowing positioning of recorder trace near chart center. VARIABLE and REFERENCE signals may have different duty cycles but must be of same frequency between 200 Hz and 1 MHz.

VOLTAGE OUTPUT and feedback for filter is provided by voltage drop across 4.99k resistor. Drop is proportional (5v/mA) to 0-1 mA current flowing in external circuit between CURRENT OUTPUT and CURRENT RETURN. If CURRENT OUTPUT unused, or if external circuit voltage drop exceeds 5v, zener conducts and maintains current through 4.99k resistor.

OPERATION

Majority gate forms inverted majority of REFERENCE inputs. EXCLUSIVE-OR gate output is in-phase REFERENCE majority when CHART POSITION switch is in the NORMAL position, or inverted REFERENCE majority when the switch is in the RECENTER position.

The FALSE going edge of waveform clocks JK FF to the SET position (Q is TRUE).

Edge detector generates a FALSE pulse approximately 15 ns wide at each FALSE going transition of the VARIABLE input. This pulse asynchronously RESETS the JK FF.

JK FF output is a FALSE pulse with width equal to the time difference between transitions of the VARIABLE input and REFERENCE majority. Q's duty cycle (FALSE time period) is proportional to the phase lead of the VARIABLE with respect to the REFERENCE.

JK FF outputs inverted and applied to the non-inverting input of an active 100 Hz 10-pass filter. Inverting input of the filter is held low by A23C to provide zero reference. Both inverter outputs are pulled-up to Vcc by 1000-ohm resistors to provide full 0-to-Vcc voltage swing.

C-REC-2 RECORDER CHANNEL 2 PHASE COMPARATOR

Same as C-REC-1

C-PCG-1 PHASE CODE TRIGGER GENERATOR

Generates phase code SET trigger on TRUE going tra... ...SE CODE INPUT waveform when PHASE CODE MODE input is TRUE. Output is fast rise... ...ntially decaying trigger of nominally 24 V amplitude and 3 μs 50 % width into ... balanced grounded or floating load.

Operation: Open-collector power driver grounds low end of 1:1:1 pulse transformer primary when driver input logic is satisfied. 0.1 μF capacitor discharges into transformer primary, generating fast-rising, exponentially decaying trigger. When driver turns off, 0.1 μF capacitor recharges to 24 V in approximately 500 μs. Diode across primary limits reverse transients. 100-ohm shunt resistor provides termination to absorb transmission line reflections. Transformer secondary is floating to provide isolation and flexibility in driving 100-ohm balanced or 50-ohm unbalanced loads. Transformer tertiary feeds voltage divider to provide TTL compatible trigger for on-card fault monitoring.

C-PCG-2 PHASE CODE TRIGGER GENERATOR

Same as C-PCG-1 except PHASE CODE RESET trigger generated on FALSE going edge of PHASE CODE INPUT

C-TDL-1 TRANSMITTER DRIVE LOSS ALARM

Senses loss of 100 kHz output, Interval, early triggers, transmitter triggers, or phase code triggers. Will detect loss of phase coding waveform when phase coded 100 kHz is selected (PHASE CODE MODE held FALSE). Phase code trigger and waveform loss alarm is inhibited when DISABLE PC ALARM input held FALSE. Output driver provided for front-panel indicator. Logic level output goes FALSE to indicate signal loss. Lamp test input activates lamp driver when held false.

Operation:

I Phase Code Loss

When PHASE CODE MODE is TRUE, PC SET and PC RESET TRIGGER MONITOR pulses from C-PCG-1 and C-PCG-2 alternately set and reset the latch A19C, D. A19C output is reconstruction of PHASE CODE waveform and is applied to A10B. Second A10B input comes from A6D in C-CSL-1 and is FALSE when PHASE CODE MODE is TRUE. A10B output is reconstructed PHASE CODE waveform.

With PHASE CODE MODE input FALSE, PC SET and PC RESET triggers are no longer generated and A19C output is randomly TRUE or FALSE. A6D output from C-CSL-1 is now the inverted PHASE CODE waveform and A10B output is either inphase or inverted PHASE CODE waveform depending on the state of A19C, D.

FALSE-going transitions of A10B output trigger A15, a retriggerable single-shot with approximately 3-second runout. A15 Q output remains TRUE so long as A10B output makes transitions less than 3 seconds apart. A15's inverted Q output will transit TRUE if A15 is not retriggered. With DISABLE PC ALARM input TRUE, A16B output will go FALSE indicating an ALARM condition by causing LOST TRANSMITTER DRIVE ALARM LOGIC and LOST TRANSMITTER DRIVE LAMP outputs to go FALSE. With DISABLE PC ALARM input FALSE, A16B output is held TRUE, preventing ALARM indication to be affected by A15.

II 100 kHz Loss

100 kHz SINE WAVE OUTPUT is coupled by C41 to a peak detector and filter. Filter output drives Q1 into conduction when 100 kHz is present. Q1 collector pulls A12, retriggerable 3-second single-shot, inputs FALSE, partially satisfies the input logic. Loss of 100 kHz causes Q1 cutoff and prevents A12 from triggering. If 100 kHz is gated, A12 inputs are only enabled during the time that 100 kHz is gated ON.

III Interval Loss

BLANKING (buffered INTERVAL-FALSE during local interval) output is inverted by A16C and applied to A12 input logic. A12 input logic is satisfied only during the local interval (BALANCING output FALSE).

IV Trigger Loss

The EARLY TRIGGER MONITOR pulse (occurring at the beginning of the INTERVAL waveform) resets the latch A19A, B. This disables A12 input logic. The MPT MONITOR pulse sets the A19A, B latch? if all other inputs to A12 are enabled, this transition triggers the single-shot.

A12 must be retriggered at least once each 3 seconds; this required:

1. 100 kHz output be present
2. BLANKING present
3. EARLY TRIGGER and MPT must reset then set A19A,B.

These conditions must be simultaneously present such that A12 input logic is alternately disabled then enabled. If these conditions are not met, A12 delay runs out and Q goes FALSE causing LOST TRANSMITTER DRIVE ALARM LOGIC output and LOST TRANSMITTER DRIVE LAMP outputs to go FALSE, giving an ALARM indication.

C-CSL-1 100 kHz PHASE CODER, SHAPER, LINE DRIVER

Uses RC filter to shape 100 kHz square wave input into sine wave. Sine wave is amplified by operational amplifier, A2, and booster amplifier, A3, to level of nominally 15 volts peak-to-peak into 50 or 100 ohm unbalanced, grounded load. 100 kHz is gated on when 100 kHz GATING INTERVAL INPUT is FALSE. The 100 kHz is phase coded by the PHASE CODE INPUT when PHASE CODE MODE is FALSE. When PHASE CODE MODE is TRUE, 100 kHz continuously coded POSITIVE.

OPERATION:

With PHASE CODE MODE input TRUE, A6D output is FALSE and output of A10A is POSITIVE coded 100 kHz (non-inverted). With PHASE CODE MODE input FALSE, A6D output is inverted PHASE CODE waveform and A10A output is phase coded 100 kHz. 100 kHz square wave from A10A drives open-collector gates A1A through A1C. When the 100 kHz GATING INTERVAL input is FALSE, A1A, B, C output is a 15 V p-p 100 kHz square wave which is applied to an R-C filter network. Filter output is 100 kHz sine wave and is applied via the 100 kHz LEVEL trimpot to operational amplifier, A2 and booster A3 which form a power amplifier with 40 dB voltage gain and are capable of driving 15 V p-p into a 50 or 100-ohm load. Since C-CSL-1 is normally internal to a cycle compensation loop, its absolute input to output time delay is uncritical and is not calibrated.

L-IBA-1 INTERVAL BUFFER AMPLIFIER

Buffers the timer INTERVAL waveform for external use such as control of receiver blanking. Output is TTL logic level with 60 unit load drive capability. Output waveform is FALSE during interval.

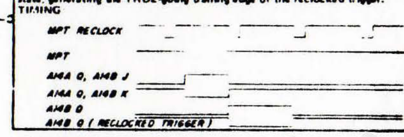
L-TTR-1 TRANSMITTER TRIGGER RECLOCK

Circuit nine times MPT to MPT RECLOCK waveform.

OPERATION:

FALSE-going edge of MPT toggles A14A to the SET state. A14B J input is driven TRUE, k input is driven FALSE. The next FALSE transition of MPT RECLOCK toggles A14B to SET State (Q is TRUE, Q is FALSE) generating the FALSE-going leading edge of the reclocked trigger and asynchronously RESETTING A14A. This puts A14B J input FALSE and k input TRUE. The next FALSE-going transition of MPT RECLOCK toggles A14B to RESET state, generating the TRUE-going trailing edge of the reclocked trigger.

TIMING



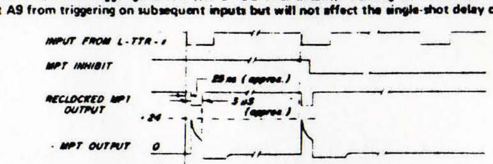
C-TTG-1 TRANSMITTER TRIGGER GENERATOR

Generates fast rising, exponentially decaying trigger at leading edge of reclocked transmitter trigger. Output has nominal 24V peak amplitude and 3 μs 50% width into 100 Ω balanced or 50 Ω grounded load. Triggers are inhibited when MPT INHIBIT input is FALSE.

OPERATION:

FALSE-going edge of input from L-TTR-1 triggers 3 μs single-shot, A9, when MPT INHIBIT input is TRUE, generating a FALSE-going, 3 μs-wide RECLOCKED MPT OUTPUT pulse. TRUE-going reclocked MPT pulse from A9 drives trigger generator (see C-PCG-1 for details). Putting MPT INHIBIT FALSE will prevent A9 from triggering on subsequent inputs but will not affect the single-shot delay cycle once triggered.

TIMING:



C-ETG-1 EARLY TRIGGER GENERATOR

Generates fast rising exponentially decaying trigger at start of INTERVAL (FALSE-going edge). Output is nominally 24 V peak amplitude and 3 μs 50% width into 100 Ω unbalanced loads.

OPERATION:

See C-PCG-1 for further explanation of trigger generator.

W0486-8/INTERFACE

Interfaces timer waveforms with various external equipment, providing level shifting, waveshaping, phase coding and phase comparison functions:

L-TTR-1 reclocks coarse MPT to MPT RECLOCK waveform.

C-TTG-1 generates high-level transmitter triggers (MPT) for driving 50 Ω or 100 Ω loads.

L-IBA-1 buffers the local INTERVAL waveform for external use such as blanking.

C-ETG-1 generates high-level EARLY TRIGGERS (at the start of the INTERVAL waveform in loran applications).

C-CSL-1 Phase-codes, gates and filters 100 kHz square wave input to produce 100 kHz sine wave. Sine wave is amplified to 15V p-p. Output has capability to drive 50 Ω or 100 Ω grounded loads.

C-PCG-1 and C-OCG-2 generate high-level phase code set and reset triggers, respectively, in Loran-C applications.

C-REC-1 and C-REC-2 are phase comparators with analog outputs for driving either current or voltage type meters, or chart recorders.

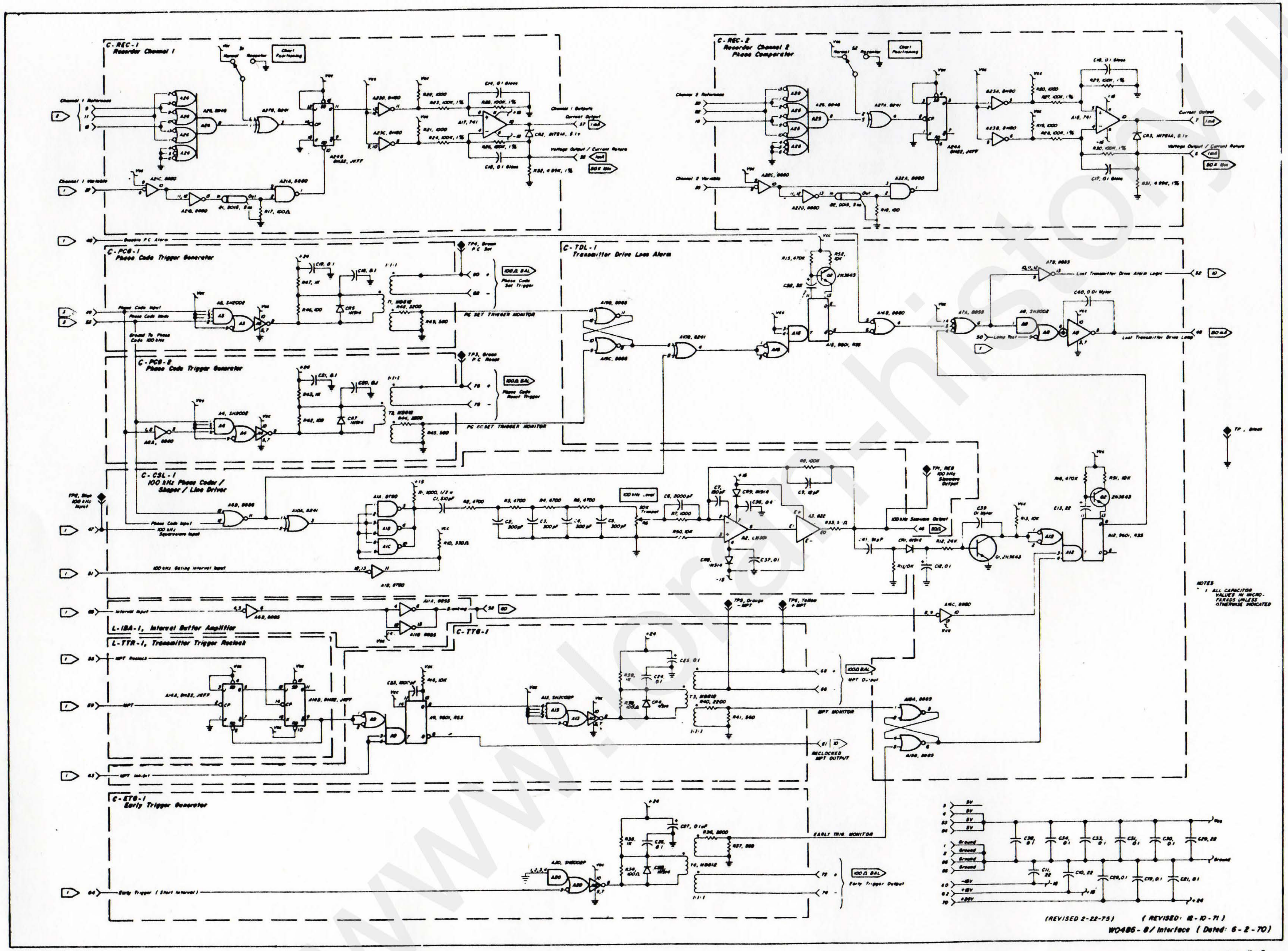
Comparator is used to monitor local compensation loop activity in loran timer applications.

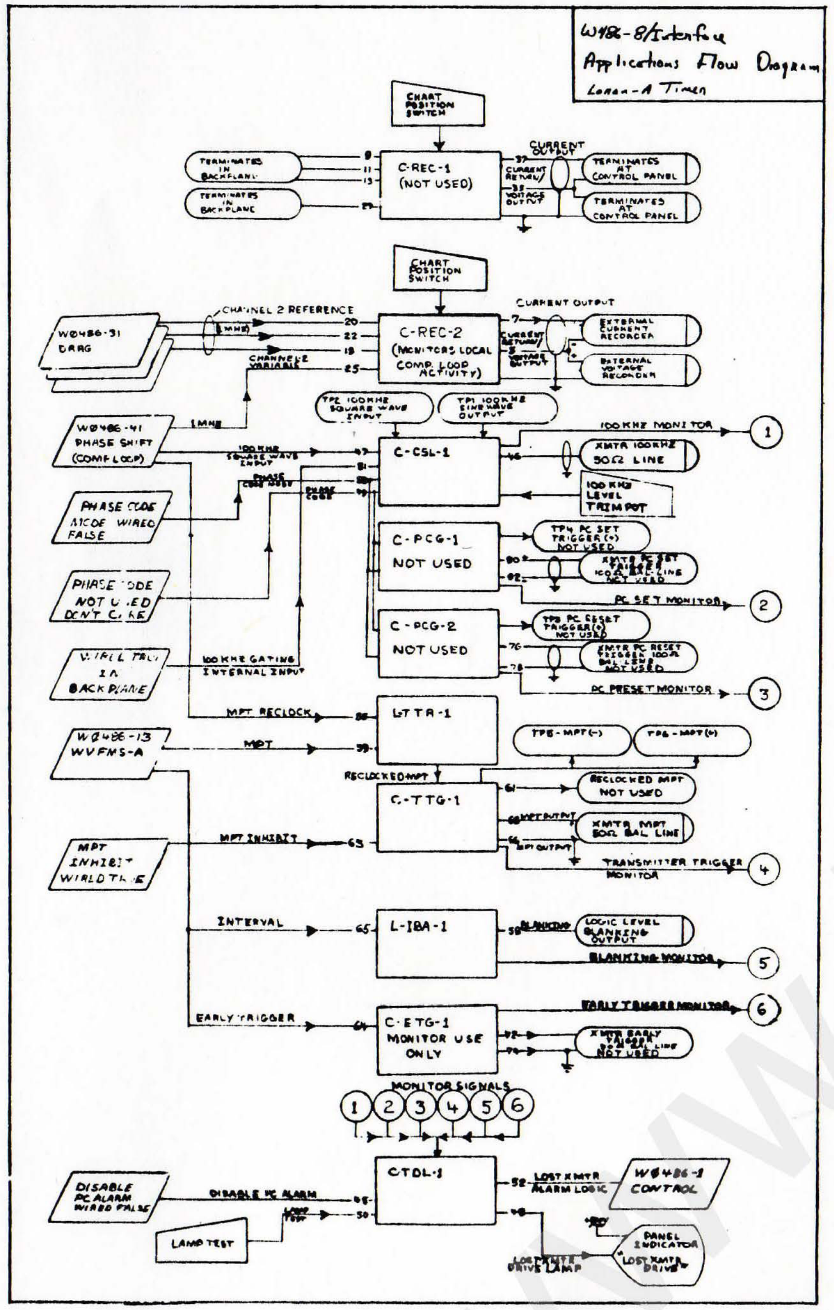
C-TDL-1 monitors outputs of C-CSL-1, C-PCG-1, C-PCG-2, C-TTG-1, C-ETG-1, and L-IBA-1 and indicates loss of any of these outputs by operating a lamp driver and setting a logic level output FALSE.

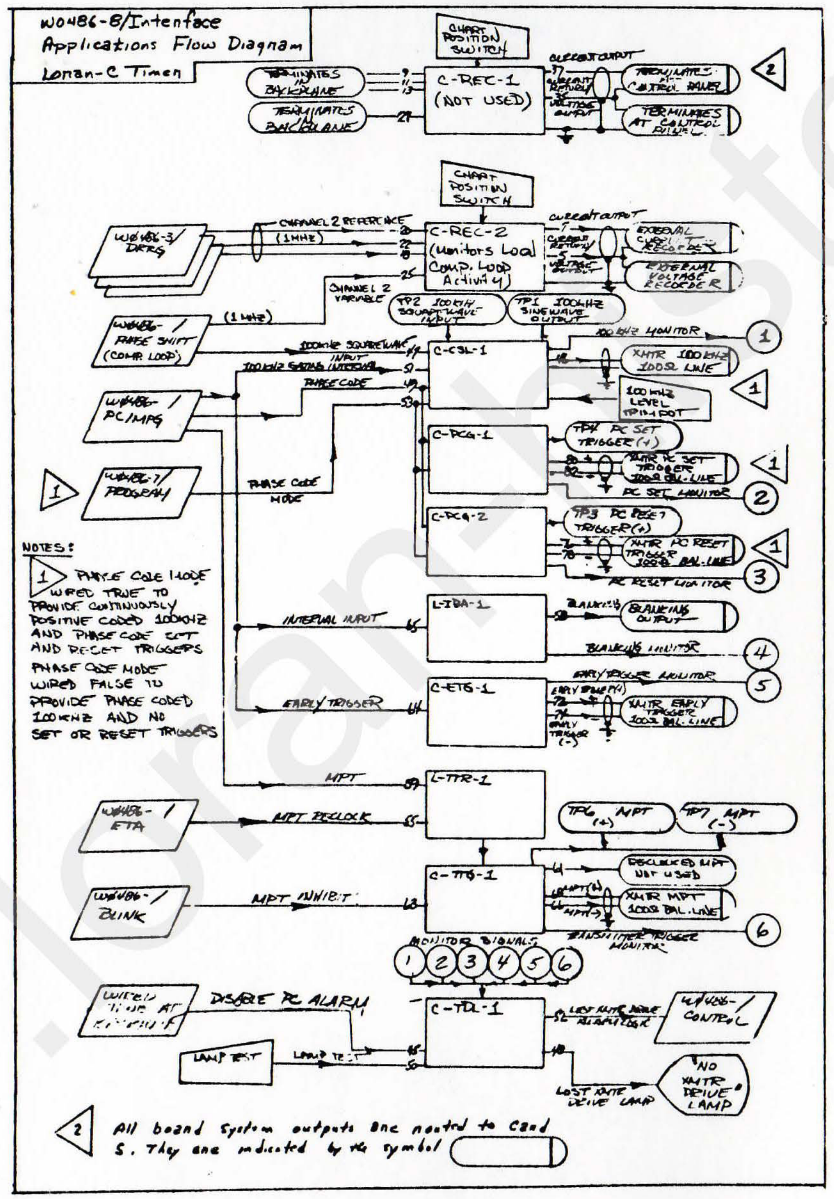
(REVISED: 12-10-71)

W0486-8/Interface (Dated: 6-2-70)

ORIGINAL


C-REC-1 Recorder Channel 1
C-REC-2 Recorder Channel 2 Phase Comparator
C-PCG-1 Phase Code Trigger Generator
C-TDL-1 Transmitter Drive Loss Alarm
C-CSL-1 100 kHz Phase Coder / Shaper / Line Driver
L-IBA-1, Interval Buffer Amplifier
L-TTR-1, Transmitter Trigger Reclock
C-ETG-1 Early Trigger Generator
(REVISED 2-22-75)
(REVISED: 12-10-71)
WO486-8/ Interface (Dated: 6-2-70)





W0486/INTERFACE (POWER REQUIREMENTS BASED ON MANUFACTURES SPEC)

MFRS PREFIX	IC TYPE	MFRS SUFIX	NO USED	MFR	POWER SUPPLY # VCC PIN #	GD PIN #	CURRENT PER PACK-MA	TOTAL CURRENT-MA
N	8T80	A	1	SIGNETICS	14	7	15.2	15.2
MCF	2002	9XX	5	FAIRCHILD	10	5	30.0	150.0
N	8885	A	1	SIGNETICS	14	7	28.4	28.4
N	8855	A	3	SIGNETICS	14	7	20.0	60.0
UCA	9601	59X	3	FAIRCHILD	14	7	25.0	75.0
N	8241	A	2	SIGNETICS	14	7	40.0	80.0
N	8H22	B	2	SIGNETICS	16	8	17.0	34.0
N	8800	A	3	SIGNETICS	14	7	14.0	42.0
N	8480	A	1	SIGNETICS	14	7	26.0	26.0
N	8840	A	2	SIGNETICS	14	7	8.0	16.0

\# 5VDC

TOTAL PER BOARD 541.62

MFRS PREFIX	IC TYPE	MFRS SUFIX	NO USED	MFR.	POWER SUPPLY # VCC PIN NO	GND PIN NO	CURRENT PER PACK MA	TOTAL CURRENT MA
LM	301	AN	1	NATIONAL	7 + 4 −	—	0.10	0.10
U6C	7741	393	2	FAIRCHILD	11 + 6 −	—	2.8	5.60
	022		1	BECKMAN	8 + 5 −	—	100.0	100.0

\# ± 15VDC

TOTAL PER BOARD 105.7 MA

W0486-8/INTERFACE 12-10-71
SUPPLEMENTAL INFORMATION

W 486 9/PC/MPT

This module generates Phase Code, Multipulse triggers and interval waveforms for either timer or other Loran C systems use. Programming for module use is summarized in Table 1.

For timer operation C MAJ 1 and C MAJ 2 provide two phases of majority 1 kHz for use by C-CNT 2 and C MPTG which, in conjunction with C PCWG, generates Phase Code and Multi-pulse triggers.

For simulator, or other system operation, C CTR 1, controlled by C INTG 1 provides another source of 1 kHz. C MAJ 1 and C MAJ 2, Programmed as Selection Gates mix this 1 kHz with that provided by the DRRG and additional programming of C PCWG produces master and slave Phase Code plus appropriate multipulses.

SECTION	APPLICATION TIMER SLAVE	MASTER	OTHER LORAN C SYSTEM
C INTG 1	X1 to Ground X2 to Ground X3 to Ground X4 to Ground X5 to Ground	X1 to Ground X2 to Ground X3 to Ground X4 to Ground X5 to Ground	X1 to DRRG D_{6I} X2 to DRRG D_{5I} X3 to DRRG D_{4I} X4 to DRRG D_{3I} X5 to DRRG D_{2I}
	Y1 to Ground Y2 to Ground Y3 to Ground Y4 to Ground Y5 to Ground	Y1 to Ground Y2 to Ground Y3 to Ground Y4 to Ground Y5 to Ground	Y1 to DRRG D_{6I} Y2 to DRRG D_{5I} Y3 to DRRG D_{4I} Y4 to DRRG D_{3I} Y5 to DRRG D_{2I}
	MI SET TO MAJORITY LORTO TS RST TO MI RST	MI SET TO MAJORITY LORTO TMRST TO MIRST	MI SET TO DRRG LORTO TMRST TO MI RST
C DSSG 1	I1 to I6 I2 to DRRG 1 kHz ø9 I3 to I2 I4 to DRRG2 1 kHz ø9 I5 to I4 I6 to DRRG3 1 kHz ø9	Connections I1 through I6 same as for Slave operation	I1 to Master Interval I2 to DRRG 1 kHz ø9 I3 to X INT I4 to C CNT 1 1 kHz ø9 I5 to Y INT I6 to C CNT 1 1 kHz ø9
C DSSG 2	J1 to J6 J2 to DRRG1 1 kHz ø5 J3 to J2 J4 to DRRG2 1 kHz ø5 J5 to J4 J6 to DRRG3 1 kHz ø5	Connections I1 through J6 same as for Slave operation	J1 to Master Interval J2 to DRRG 1 kHz ø5 J3 to X INT J4 to C CNT 1 1 kHz ø5 J5 to Y INT J6 to C CNT 1 1 kHz ø5
C PCWG 1	M1 to DRRG1 GRR Interval M2 to DRRG2 GRR Interval M3 to DRRG3 GRR Interval	Connections same as for Slave Operation	M1 to M2 M2 to M3 M3 to DRRG GRR Interval

C INTG 1 INTERVAL GENERATOR

Generates up to three intervals for control of module dividers and for external output. Operation is dependent on programming.

Timer Operation. Only one interval, Master is generated. Majority LORTO sets an R S latch whose outputs are used internally to control C CNT 2 and buffered for additional system use. The interval is terminated 1400 μs after the correct number of multi pulses have been generated, i.e., master timer interval 10,900 μs, slave timer interval 8,900 μs.

Other System. Up to three intervals are generated. Master interval is produced as outlined above, duration 10,900 μs. Two slave intervals, X and Y, may be generated. The intervals are initiated when the X or Y gates detect coincidence by decoding a DRRG to $X_1X_2,X_3X_4X_5$, 0 μs. The coincidence presets C CNT 1 and sets an R S latch. The latch outputs control C MPTG, C CNT 1 and are buffered for other system use.

Slave interval duration is 7900 μs. The module will operate correctly whenever the minimum intervals shown at right are observed.
These spacings insure proper generation of the module's dividers.

M ≥ 21090 μs X
≥ 27,901 μs
≥ 27,901 μs
Y

TP 6, Red X INT · TP-5, Blue Y INT · TP-1, Yellow M INT · SLAVE INTERVAL RESET · TRIGGER ENABLE · TMRST · TSRST

C CNT 2 : MULTI PULSE INTERVAL COUNTER

Multi-pulse intervals are generated by a synchronous binary counter whose output is continuously decoded into 0 through 9 and 11 decimal states.

The counter is enabled only during an Interval as defined by C INTG 1. The counter clock is 1 kHz, producing 1000 μs increments at the divider output.

State 8 is used to reset the slave intervals in C INTG 1 while states 9 and 11 are used to reset the Master interval latch for timer slave (TSRST) or master (TMRST) operation respectively. The decoded outputs 0 through 9, excluding 8 are used in forming phase code and multipulse triggers.

C MPTG 1 : MULTIPULSE TRIGGER GENERATOR

TRUE 1 kHz ø5 pulses are ANDed with an enabling waveform from C-CNT-2 and the specified decoded outputs from C-INTG-1 to produce multi-pulse triggers commencing 500 μs after an interval is initiated. The triggers are digitally differentiated and buffered to produce FALSE, 200 ns, multipulse triggers. The first eight of these pulses are available for system use as MPT8 and these same first 8 pulses plus a ninth pulse (if module is programmed for master operation) are available as MPT9.

TP-2, Green MPT 8 · TP-3, Orange MPT 9

C MAJ 1 : FREQUENCY SOURCE SELECTION GATE

Six inputs to a AND OR invert gate are provided so that a desired frequency source/majority is gated to C-CNT 2.

Timer Operation: For timer operation the module is connected so that the AND-OR gate performs majority logic. Output is a TRUE 1 kHz ø9 majority.

Other System Use: For Loran-C systems other than timers the selection gate operates so that only one frequency source at a time is passed to C-INTG 1. This is accomplished by connecting the M, X and Y interval waveforms to one of the inputs of the 3 AND gates and 1 kHz from the DRRG or C-CNT-1 to the other AND gate inputs. Since only one interval is TRUE at any one time, the desired 1 kHz is passed.

1 kHz ø9

C MAJ 2 : FREQUENCY SOURCE SELECTION GATE

Identical to C-DSSG-1 except 1 kHz ø5 is selected and the output goes to C-MPTG-1.

1 kHz ø5

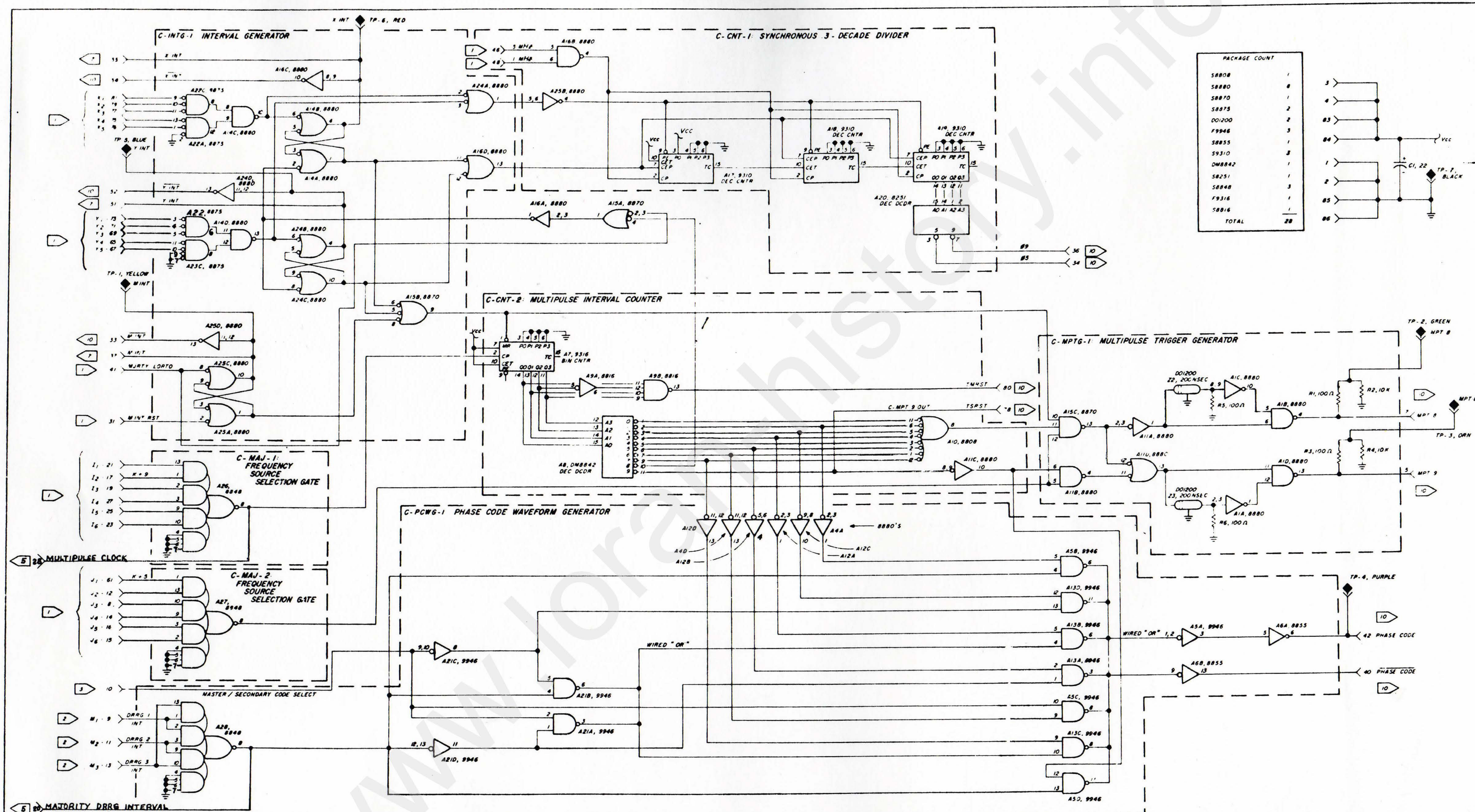
C PCWG 1 PHASE CODE WAVEFORM GENERATOR

AND OR invert gate detects a majority DRRG ... output is gated with the MASTER / SECONDARY CODE SELECT input and multi-pulse intervals provided from C CNT 2. The output of this three level gating arrangement is a double railed standard Loran C phase code ... The code is tabulated below.

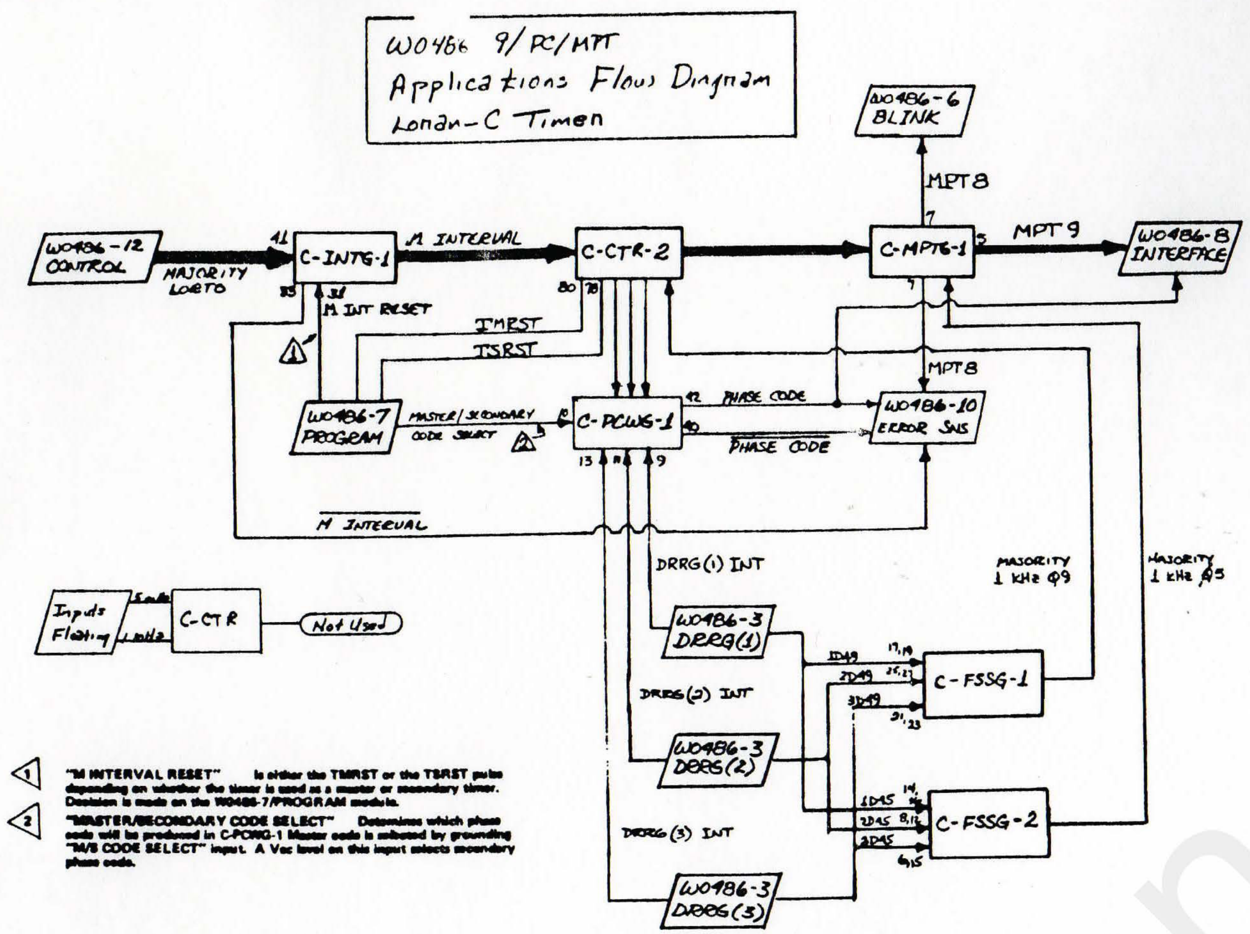
PULSE MODE/INT	1	2	3	4	5	6	7	8	Mex
M_A	+	+	–	–	+	–	+	–	+
M_B	+	–	–	+	+	+	+	+	–
S_A	+	+	+	+	+	–	–	+	
S_B	+	–	+	–	+	+	–	–	

Master code is selected by grounding MASTER/SECONDARY CODE SELECT INPUT. A TRUE Level on this input selects secondary phase code.

TP-4, Purple PHASE CODE · 42 PHASE CODE · 40 $\overline{PHASE\ CODE}$ · MASTER / SECONDARY CODE SEL



(REVISED 2-22-75)



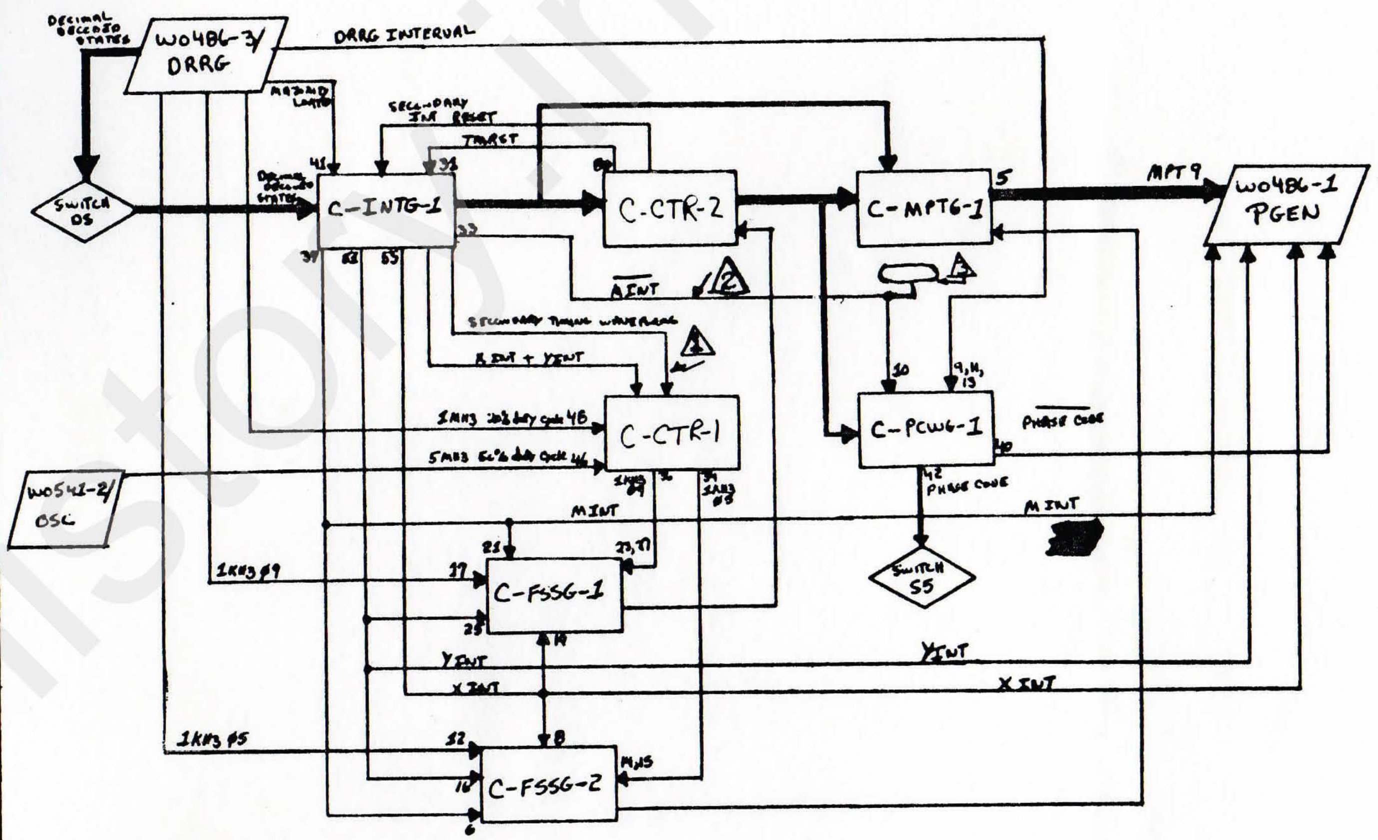
⚠1 "M INTERVAL RESET" is either the TMRST or the TSRST pulse depending on whether the timer is used as a master or secondary timer. Decision is made on the W0486-7/PROGRAM module.

⚠2 "MASTER/SECONDARY CODE SELECT" Determines which phase code will be produced in C-PCWG-1 Master code is selected by grounding "M/S CODE SELECT" input. A Vcc level on this input selects secondary phase code.

W0486-9A/PC/MPT (POWER REQUIREMENTS BASED ON MANUFACTURERS SPECIFICATIONS)

MFRS. PREFIX	IC TYPE	MFRS SUFFIX	MFR	NO USED	POWER SUPPY VCC PIN #	GND PIN #	CURRENT PER PACK	TOTAL CURRENT
N	8880	A	SIGNETICS	8	14	7	14.0	112.0
U6A	9946	59X	FAIRCHILD	3	14	7	13.0	39.0
N	8855	A	SIGNETICS	1	14	7	20.0	20.0
U7B	9316	59X	FAIRCHILD	1	16	8	70.0	70.0
DM	8842	N	NATIONAL	1	16	8	56.0	56.0
N	8816	A	SIGNETICS	1	14	7	11.8	11.8
N	8808	A	SIGNETICS	1	14	7	5.9	5.9
N	8870	A	SIGNETICS	1	14	7	17.7	17.7
U6B	9310	59X	FAIRCHILD	3	16	8	70.0	210.0
N	8251	B	SIGNETICS	1	16	8	25.7	25.7
N	8875	A	SIGNETICS	2	14	7	21.0	21.0
N	8848	A	SIGNETICS	3	14	7	8.0	24.0

TOTAL PER BOARD 725.1 MA



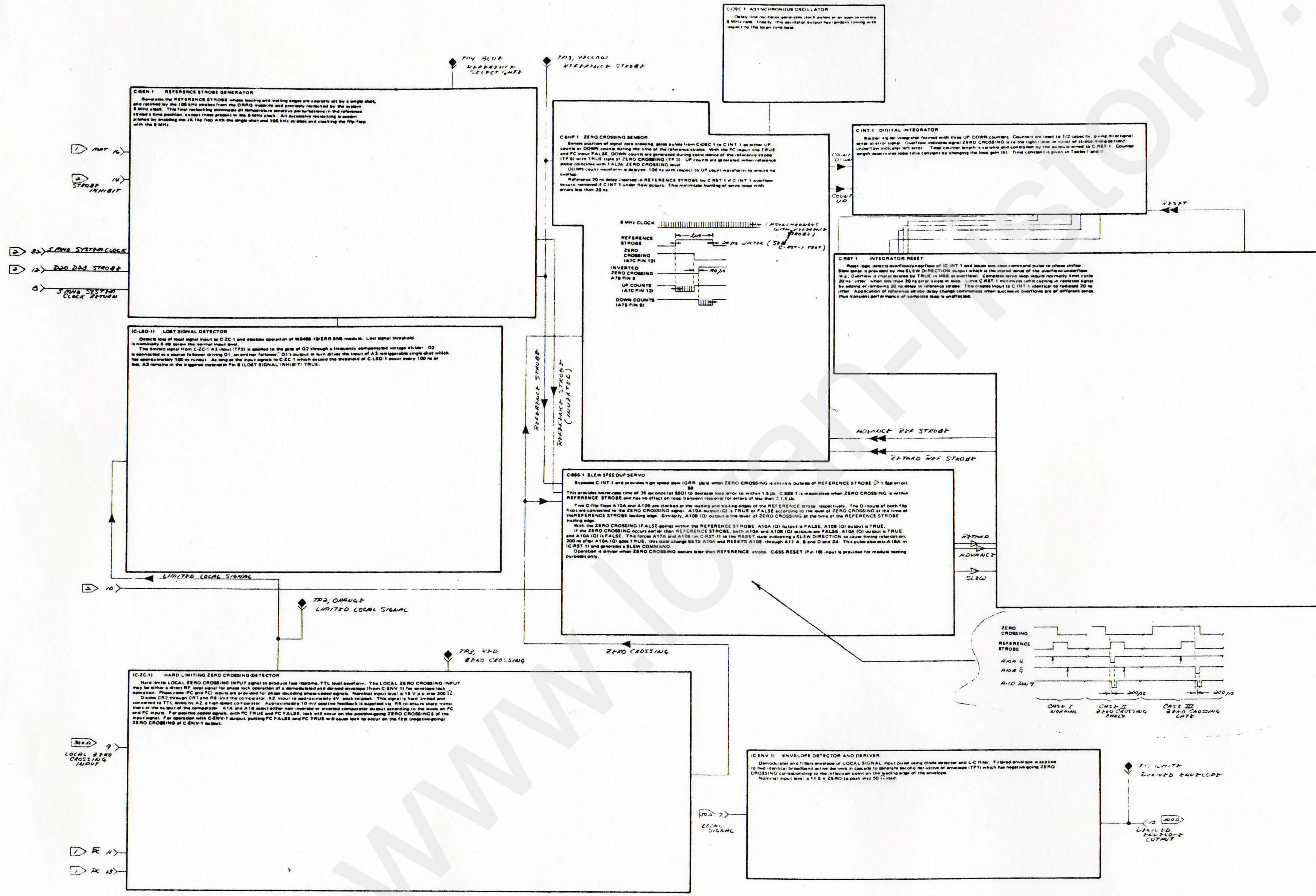
⚠1 Secondary Timing Waveforms = $(X_1\ X_2\ X_3\ X_4\ X_5) + (Y_1\ Y_2\ Y_3\ Y_4\ Y_5)$ Used as a parallel, enable waveform for the decade counters of C-CTR-1. These timing waveforms occur at the beginning of the secondary interval.

⚠2 M INT - Used as the controlling logic waveform for the MASTER/SECONDARY CODE SELECT. The M INT waveform is low during the master interval and high during the secondary interval. This is exactly the logic required to control the phase coding.

⚠3 This M INT waveform is used as a scope trigger and is provided via a front-panel BNC connection.

W0486-9/PC/MPT
Application Flow Diagram
Loran-C Simulator

W0486-9/PC/MPT 12-10-71
Supplemental Information



W0486-10/ERRSNS

This module measures the error between an input reference waveform, derived from the ORRG majority and the local radiated ZERO CROSSING (either carrier ZERO CROSSING or envelope second derivative ZERO CROSSING). The output of the module is a slew command pulse and slew direction level to the digital phase shifter, W0486-4/O SHIFT. The module realizes the subtraction and gain function (K) of a TYPE 1 servo loop symbolically represented below.

C-GEN-1 develops precise REFERENCE STROBE whose leading and trailing edges are positioned in time by data from the ORRG's. C-ZC-1 generates a hard limited ZERO CROSSING of the local radiated carrier or envelope. C-SHF-1 generates two sequential count intervals whose width is equal to the time between REFERENCE STROBE leading edge and ZERO CROSSING, and ZERO CROSSING and REFERENCE STROBE trailing edge. C-INT-1 then digitally measures and scales the magnitude of the difference in these two intervals' width. When an unbalance persists in these two intervals, C-INT-1 develops a slew command to W0486-4/O SHIFT in the direction to correct the unbalance. The complete servo loops thus maintains the radiated ZERO CROSSING positioned within 20 ns of the midpoint of the REFERENCE STROBE.

The principle feature of this module is that all measurements are made digitally; there are no analog functions (excluding the envelope deriver). This results in a system that is almost totally insensitive to temperature or line voltage fluctuations. This operation is achieved through the use of a 8 MHz clock (C-OSC-1) whose phase is random with respect to the differential intervals it is used to measure. C-INT-1 is a bipolar digital integrator (UP/DOWN counter) which performs the digital scaling function (gain K where K < 1) and acts to average the differential width measured with C-OSC-1. Accurate control of the 20 ns phase shifter is provided with relative low frequency (8 MHz) digital elements by means of the noise bias introduced by the random clock phase.

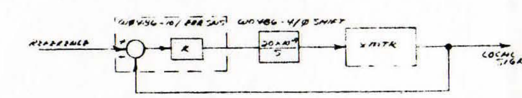


TABLE I

APPROXIMATE BASIC TIME CONSTANT (960/X) – SECONDS			
BASIC RATE	LOR A	LOR C MASTER	LOR C SECONDARY
H	29 sec	3 sec	3.5 sec
L	38 sec	4 sec	5 sec
S	48 sec	5.5 sec	6 sec
SH	56 sec	6.5 sec	7 sec
SL	74 sec	8.5 sec	9.5 sec
SS	96 sec	10.5 sec	12 sec

TABLE II. LOOP SCALE FACTOR (N)

MULTIPLY BASIC TIME CONSTANT BY	C-RST-1 INPUTS E9	E10	OR E9	E10
1	E8	E8	–	–
2	E8	E5	E5	E5
3	E8	E6	E6	E6
4	E5	E6	–	–
5	E7	E8	E7	E7
6	E7	E5	–	–
7	E7	E6	–	–

LOOP TIME CONSTANT

Loop time constant is determined both by the sampling rate (average local RF pulses per second) and by the overflow underflow count of C-INT-1

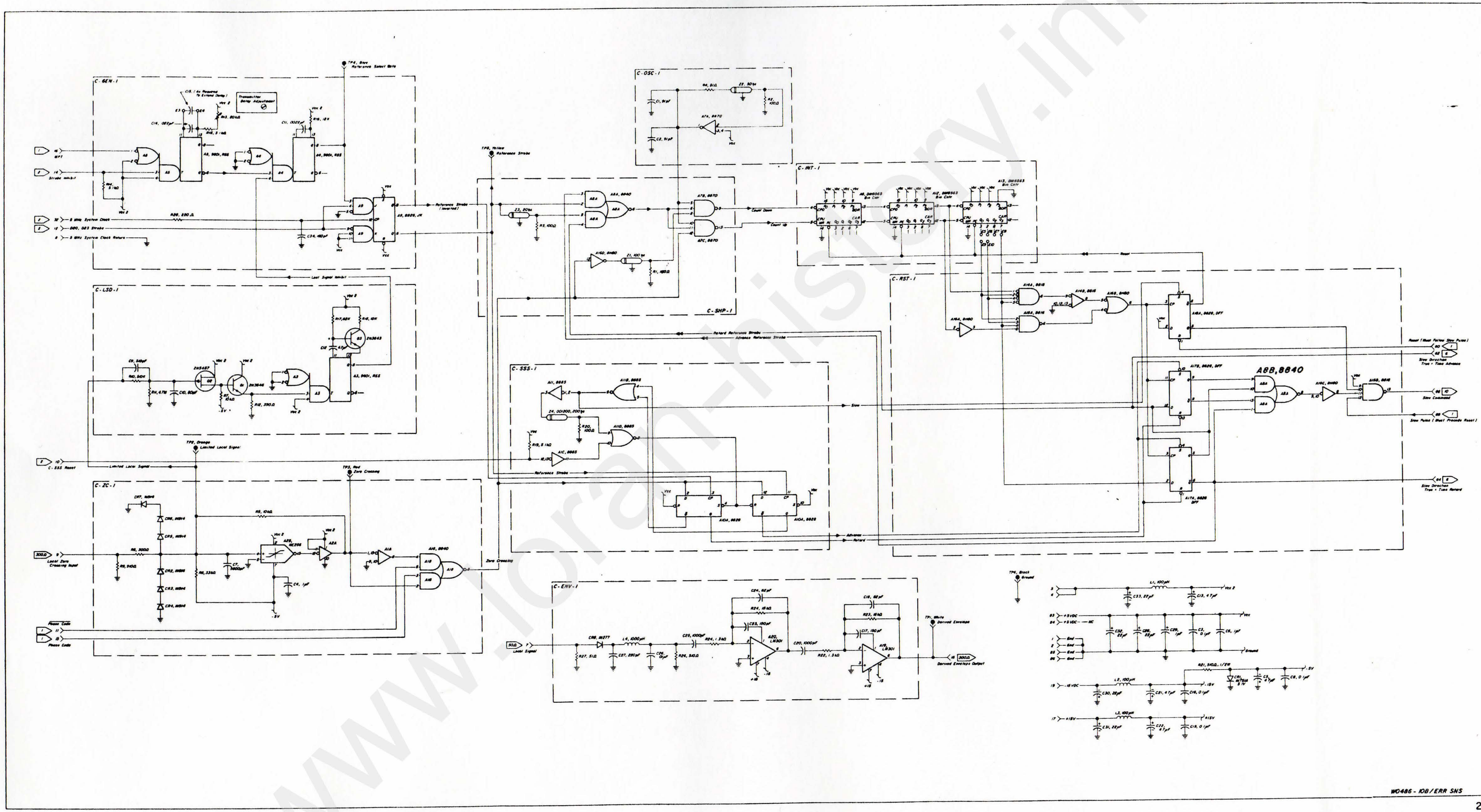
$$\text{time constant} \cong \frac{960\,N}{X}\ \text{seconds}$$

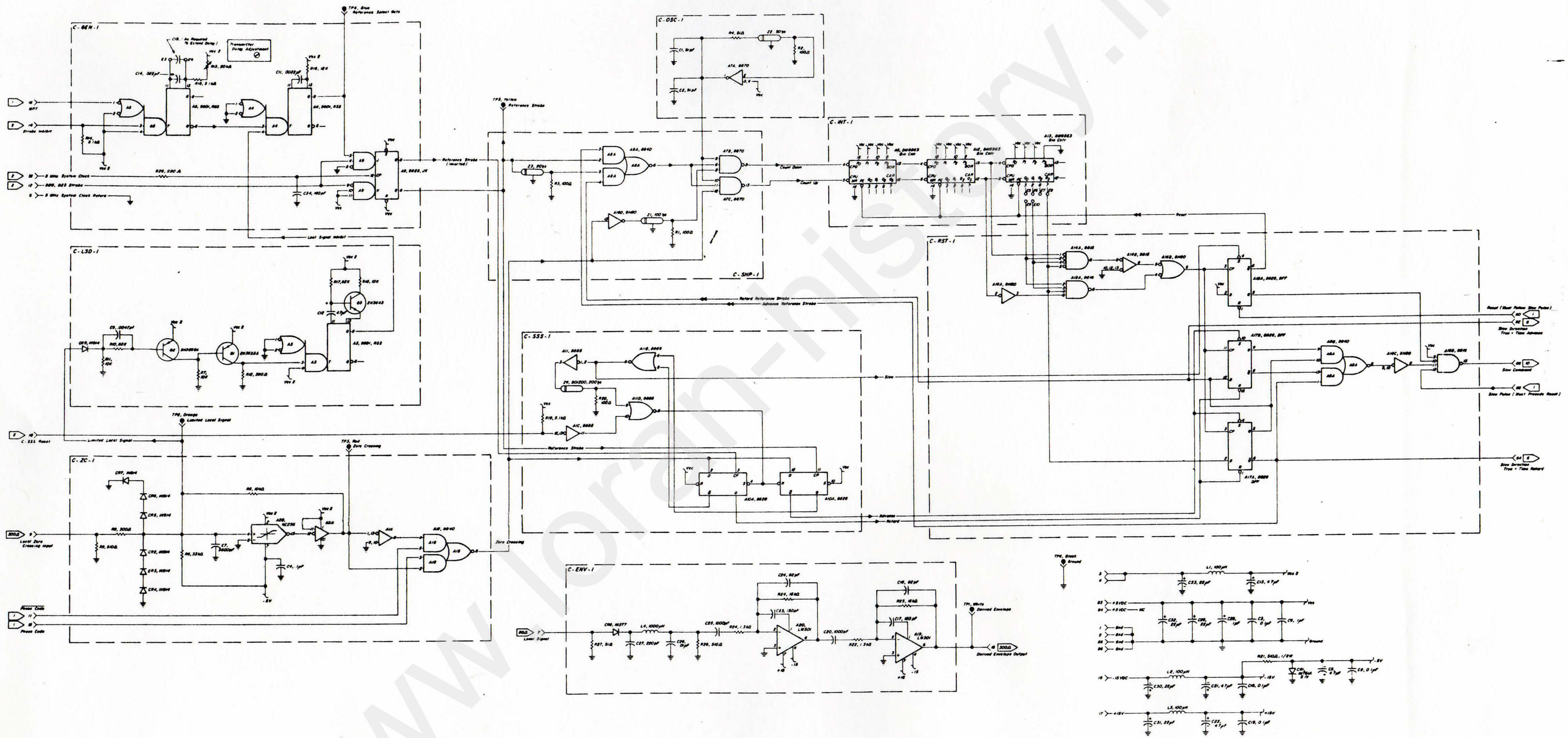
where X = sampling rate (See Table I)
N = C-INT-1 scale factor (Table II)

C-INT-1 scale factor (N) is determined by the wiring of jumpers between the four output turret terminals of C-INT-1 (E5, E6, E7, E8) and the two input turret terminals of C-RST-1 (E9, E10). These connections determine the overflow/underflow count of C-INT-1 and scale the loop again (K). When making these connections, both turret terminals E9 and E10 (A14 and A15 inputs) of C-RST-1 MUST be wired to one of the four available outputs of A13 in C-INT-1.

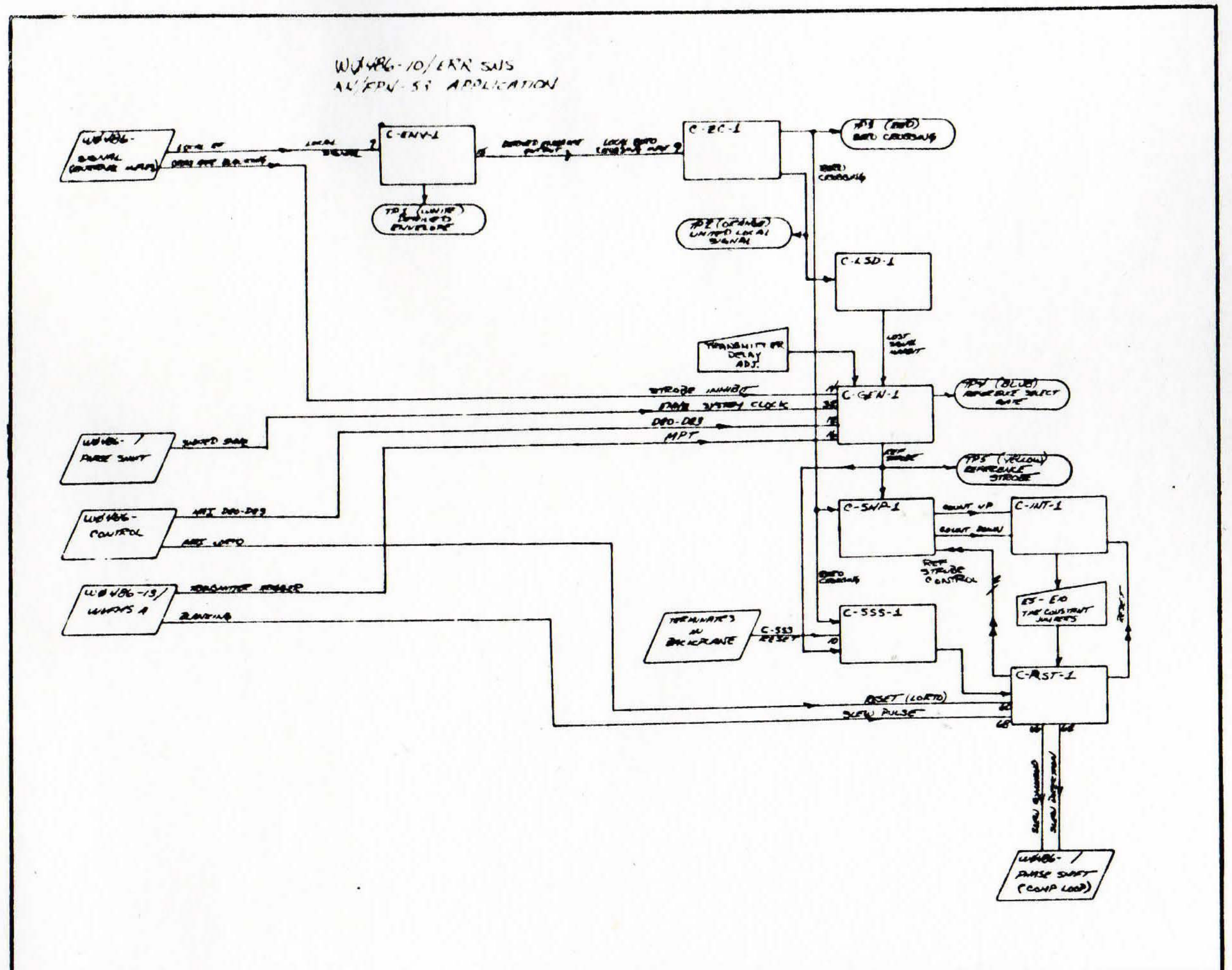
One or both input terminals of C-RST-1 may be wired to any given output of C-INT-1 (E5, E6, E7, E8), however, no two outputs of C-INT-1 may be connected together or to the same C-RST-1 input. Table II gives all possible combinations of connections, which allow N to vary from 1 to 7.

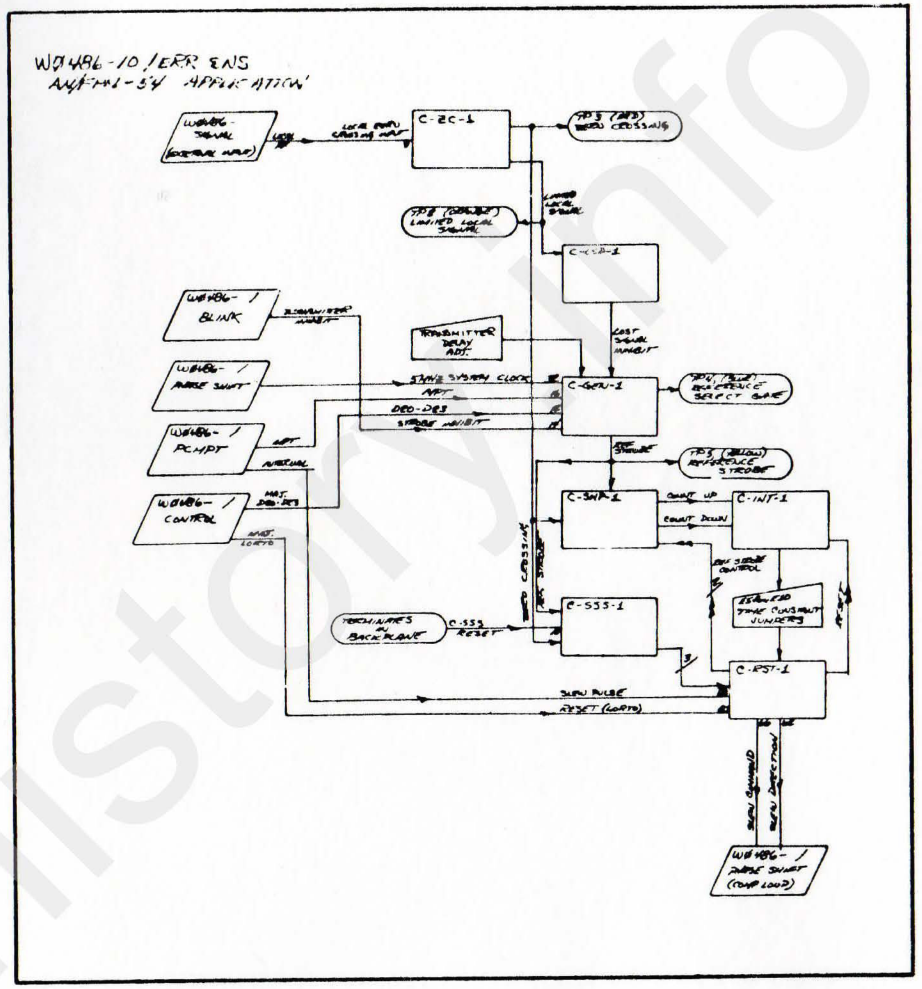
W0486-10/ERR SNS
(BLOCKED TEXT)


C-GEN-1
C-OSC-1
C-INT-1
C-SHP-1
C-LSD-1
C-RST-1
C-SSS-1
C-ZC-1
C-ENV-1
A8B, 8840
W0486-108/ERR SNS



W0486-10B (MOD)-10C/ERR SNS





SUPPLEMENTARY INFORMATION

W0486-10B/ERR SNS (POWER REQUIREMENTS BASED ON MANUFACTURES SPECIFICATIONS)

+5VDC

MFRS PREFIX	IC TYPE	MFR SUFFIX	MFR	NO USED	POWER SUPPLY: VCC PIN NO	GND PIN NO	CURRENT PER PACK MA	TOTAL CURRENT MA
U6A	9601	59X	FAIRCHILD	3	14	7	25.0	75.0
N	8840	A	SIGNETICS	2	14	7	11.0	22.0
DM	8563	—	NATIONAL	3	16	8	50.0	150.0
N	8870	A	SIGNETICS	1	14	7	17.7	17.7
N	8825	A	SIGNETICS	1	14	7	25.0	25.0
N	8828	A	SIGNETICS	3	14	7	22.0	66.0
N	8885	A	SIGNETICS	1	14	7	20.0	20.0
N	8815	A	SIGNETICS	1	14	7	16.0	16.0
N	8816	A	SIGNETICS	1	14	7	11.8	11.8
N	8880	A	SIGNETICS	1	14	7	19.0	19.0
NE	526	A	SIGNETICS	1	14	7	24.0	24.0

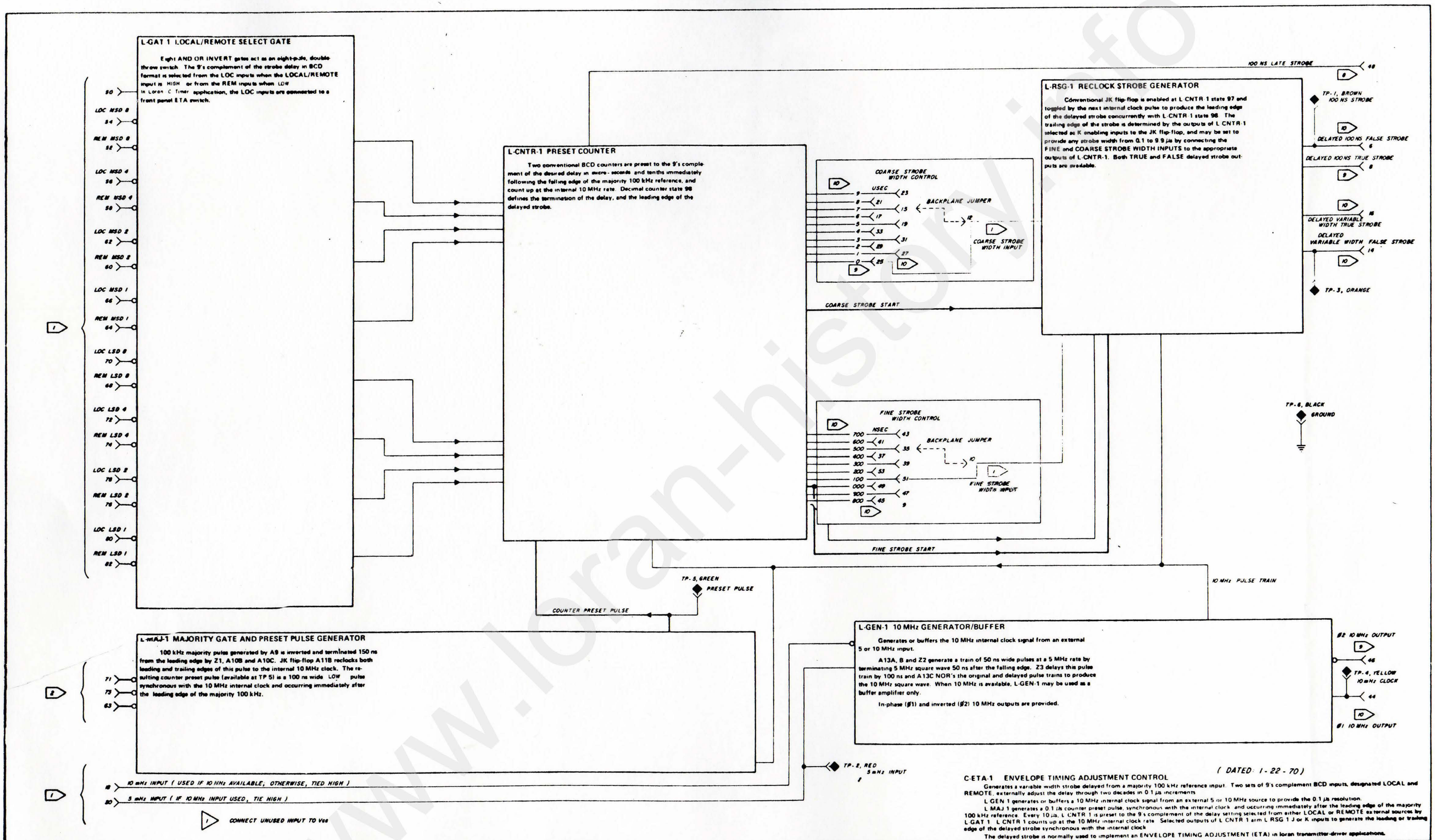
TOTAL PER BOARD 441.5

±15VDC

MFRS PREFIX	IC TYPE	MFRS SUFFIX	MFR.	NO USED	POWER SUPPLY: VCC PIN NO	GND PIN NO	CURRENT PER PACK MA	TOTAL CURRENT MA
U6E	7741	393	FAIRCHILD	1	11+ 6−	—	2.8	2.8
LM	301	AN	NATIONAL	2	7+ 4−	—	0.1	0.2

TOTAL PER BOARD 3.0MA.

SUPPLEMENTAL INFORMATION
W0486-10B/ERR SNS 12-17-71



(DATED: 1-22-70)

C-ETA-1 ENVELOPE TIMING ADJUSTMENT CONTROL

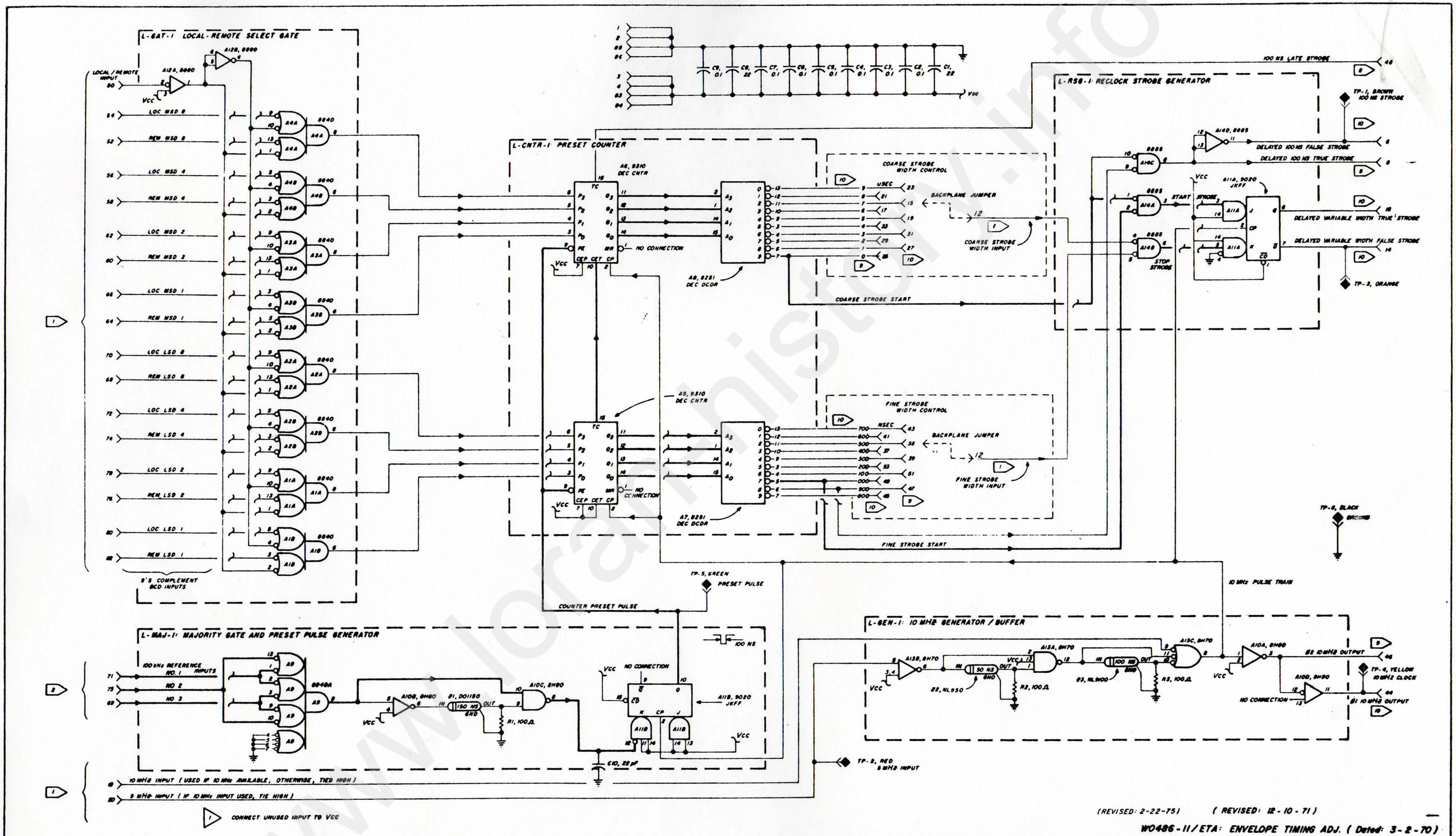
Generates a variable width strobe delayed from a majority 100 kHz reference input. Two sets of 9's complement BCD inputs, designated LOCAL and REMOTE, externally adjust the delay through two decades in 0.1 µs increments.

L GEN 1 generates or buffers a 10 MHz internal clock signal from an external 5 or 10 MHz source to provide the 0.1 µs resolution.

L MAJ 1 generates a 0.1 µs counter preset pulse, synchronous with the internal clock and occurring immediately after the leading edge of the majority 100 kHz reference. Every 10 µs, L CNTR 1 is preset to the 9's complement of the delay setting selected from either LOCAL or REMOTE external sources by L-GAT 1. L CNTR 1 counts up at the 10 MHz internal clock rate. Selected outputs of L CNTR 1 arm L RSG 1 J or K inputs to generate the leading or trailing edge of the delayed strobe synchronous with the internal clock.

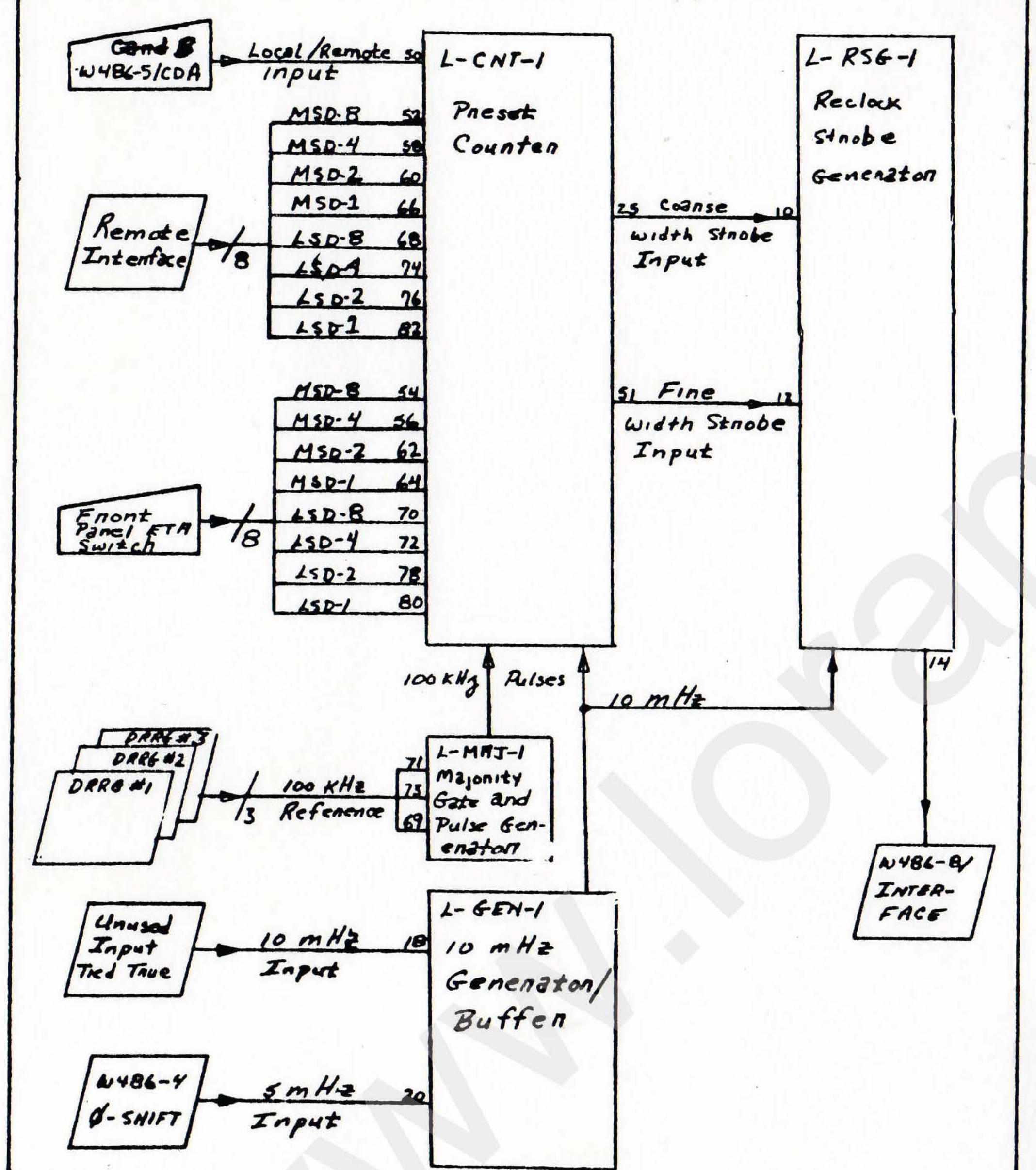
The delayed strobe is normally used to implement an ENVELOPE TIMING ADJUSTMENT (ETA) in loran transmitter-driver applications.

(REVISED 12-10-71)


L-GAT-1 LOCAL-REMOTE SELECT GATE
LOCAL / REMOTE INPUT
LOC MSD 8
REM MSD 8
LOC MSD 4
REM MSD 4
LOC MSD 2
REM MSD 2
LOC MSD 1
REM MSD 1
LOC LSD 8
REM LSD 8
LOC LSD 4
REM LSD 4
LOC LSD 2
REM LSD 2
LOC LSD 1
REM LSD 1
9'S COMPLEMENT BCD INPUTS
L-CNTR-1 PRESET COUNTER
A6, 9310 DEC CNTR
A8, 9301 DEC DCDR
A9, 9310 DEC CNTR
A7, 9301 DEC DCDR
NO CONNECTION
COARSE STROBE WIDTH CONTROL
BACKPLANE JUMPER
COARSE STROBE WIDTH INPUT
COARSE STROBE START
FINE STROBE WIDTH CONTROL
FINE STROBE WIDTH INPUT
FINE STROBE START
L-RSG-1 RECLOCK STROBE GENERATOR
100 NS LATE STROBE
TP-1, BROWN 100 NS STROBE
DELAYED 100NS FALSE STROBE
DELAYED 100 NS TRUE STROBE
DELAYED VARIABLE WIDTH TRUE STROBE
DELAYED VARIABLE WIDTH FALSE STROBE
TP-3, ORANGE
START
STOP STROBE
TP-6, BLACK GROUND
TP-5, GREEN PRESET PULSE
COUNTER PRESET PULSE
10 MHz PULSE TRAIN
L-MAJ-1 MAJORITY GATE AND PRESET PULSE GENERATOR
100 kHz REFERENCE INPUTS
NO. 1
NO 2
NO 3
C10, 22 pF
L-GEN-1: 10 MHz GENERATOR / BUFFER
82 10 MHz OUTPUT
TP-4, YELLOW 10 MHz CLOCK
81 10 MHz OUTPUT
NO CONNECTION
TP-2, RED 5 MHz INPUT
10 MHz INPUT (USED IF 10 MHz AVAILABLE, OTHERWISE, TIED HIGH)
5 MHz INPUT (IF 10 MHz INPUT USED, TIE HIGH)
CONNECT UNUSED INPUT TO Vcc
(REVISED: 2-22-75)
(REVISED: 12-10-71)
W0486-II/ETA: ENVELOPE TIMING ADJ. (Dated: 3-2-70)

W486-11/ETA APPLICATION FLOW DIAGRAM

LORAN-C TIMER

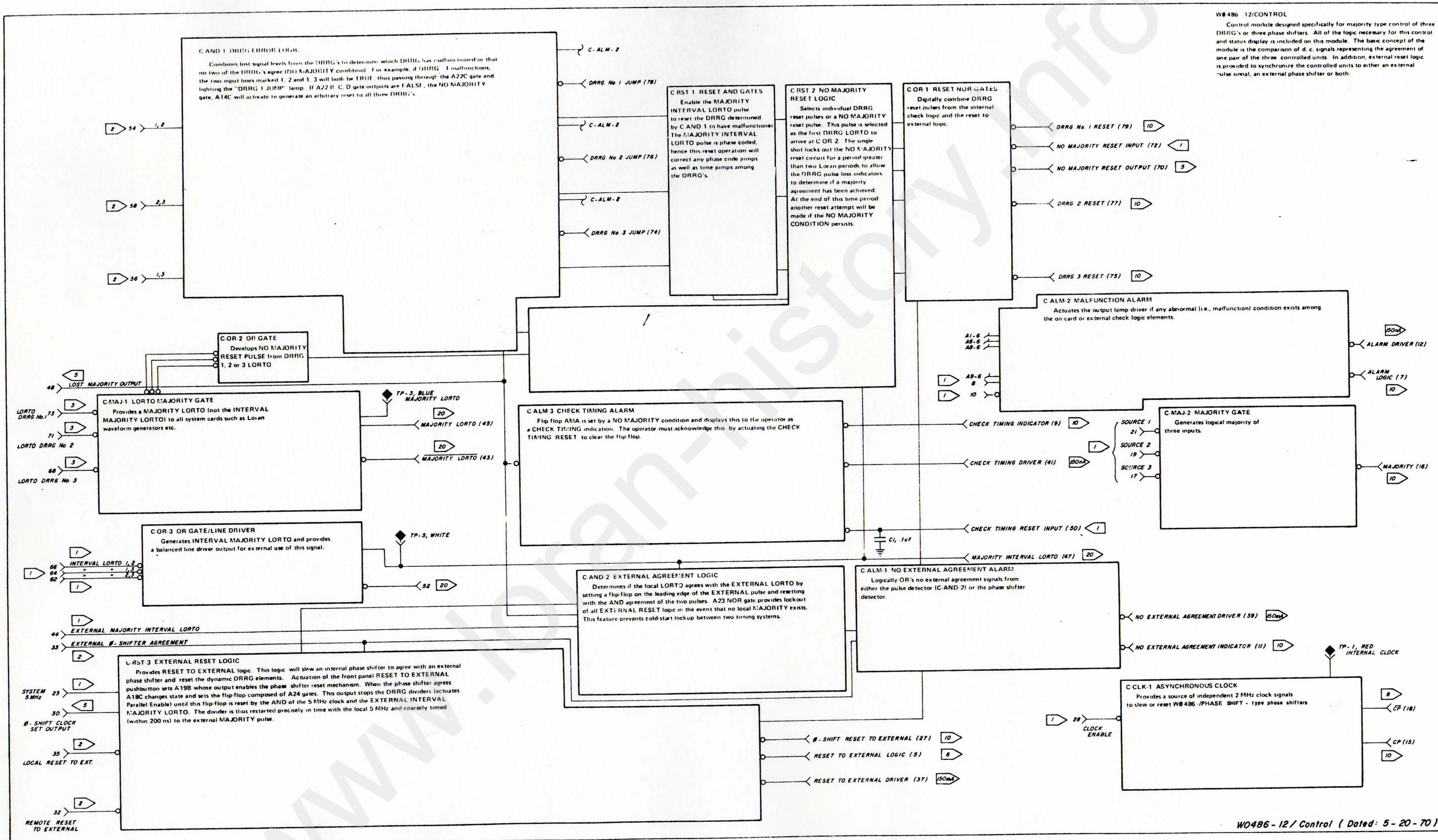


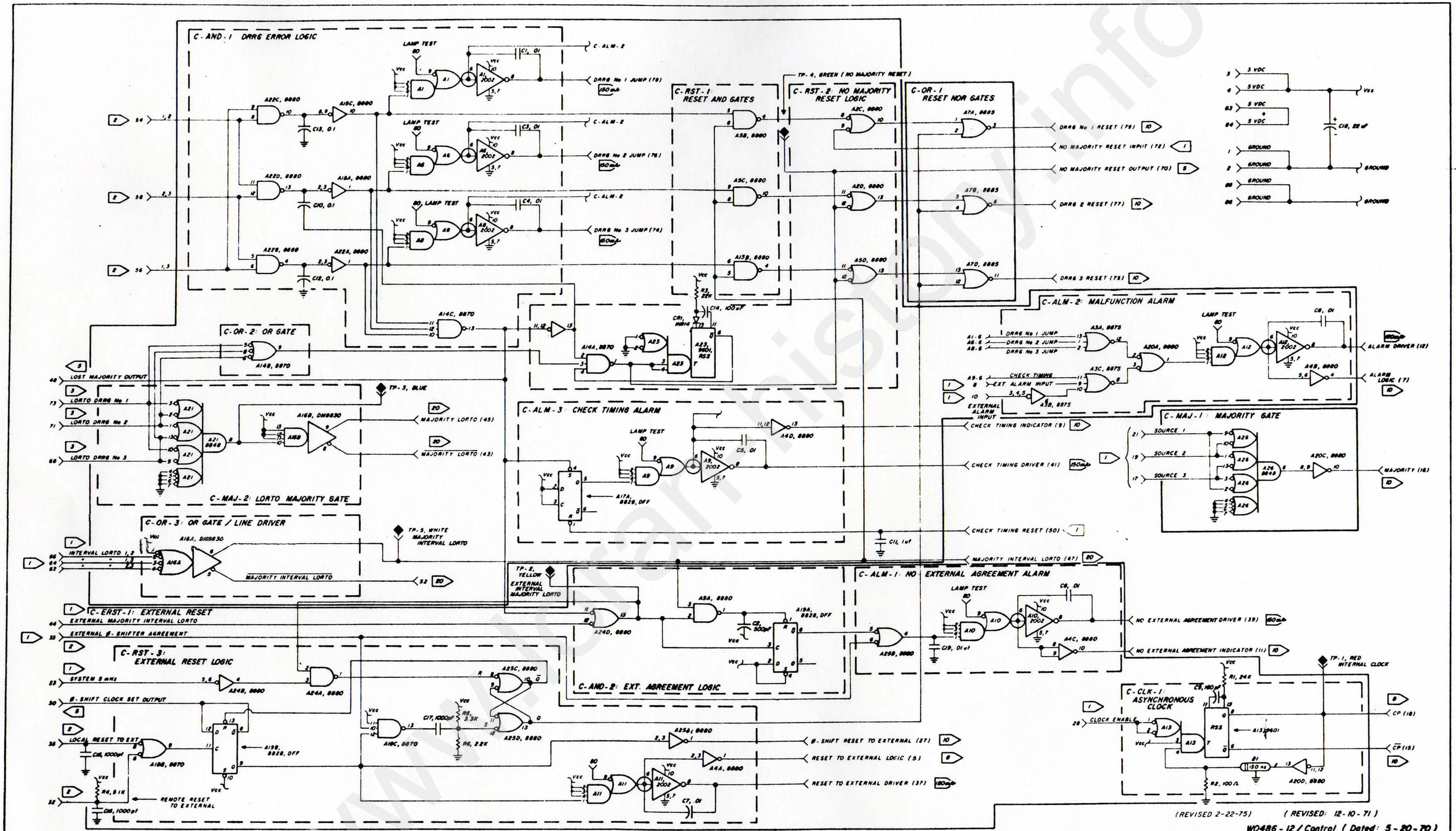
WO-486-11/ETA (POWER REQUIREMENTS BASED ON MANUFACTURERS SPECIFICATIONS)

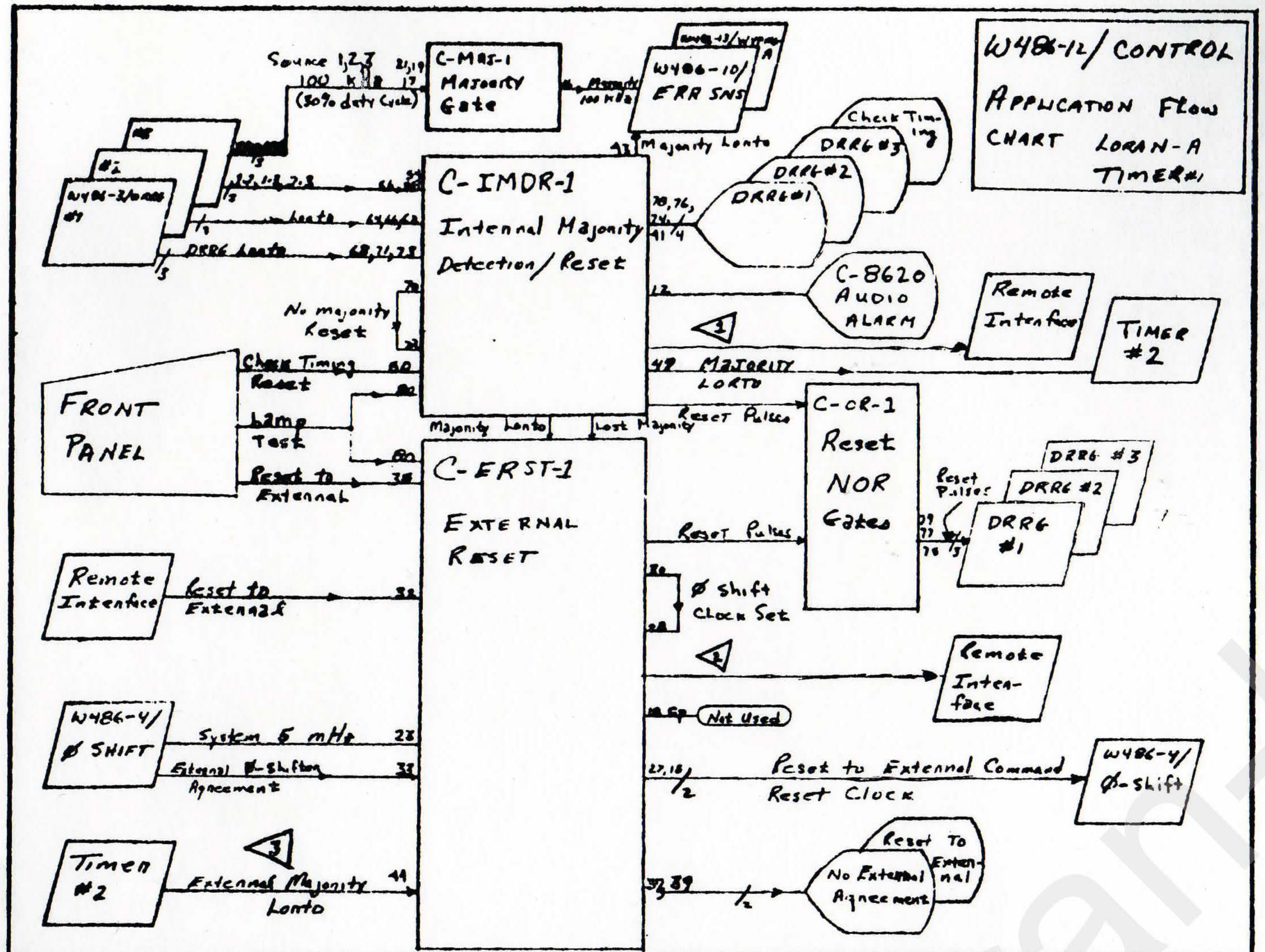
MFRS PREFIX	IC TYPE	MFRS SUFFIX	MFR	NO USED	POWER SUPPLY: Vcc PIN #	GND PIN #	CURRENT PER PACK	TOTAL CUR.
N	8840	A	SIGNETICS	4	14	7	11,0	44,0
U6B	9310	59X	FAIRCHILD	2	16	8	70.0	140
N	8251	B	SIGNETICS	2	16	8	25.7	51,4
N	8848	A	SIGNETICS	1	14	7	8.0	8.0
N	8H80	A	SIGNETICS	1	14	7	26.0	26.0
U7B	9020	59X	FAIRCHILD	1	16	8	28.0	28.0
N	8880	A	SIGNETICS	1	14	7	14.0	14.0
N	8H70	A	SIGNETICS	1	14	7	26.0	26.0
N	8885	A	SIGNETICS	1	14	7	28.4	28.4

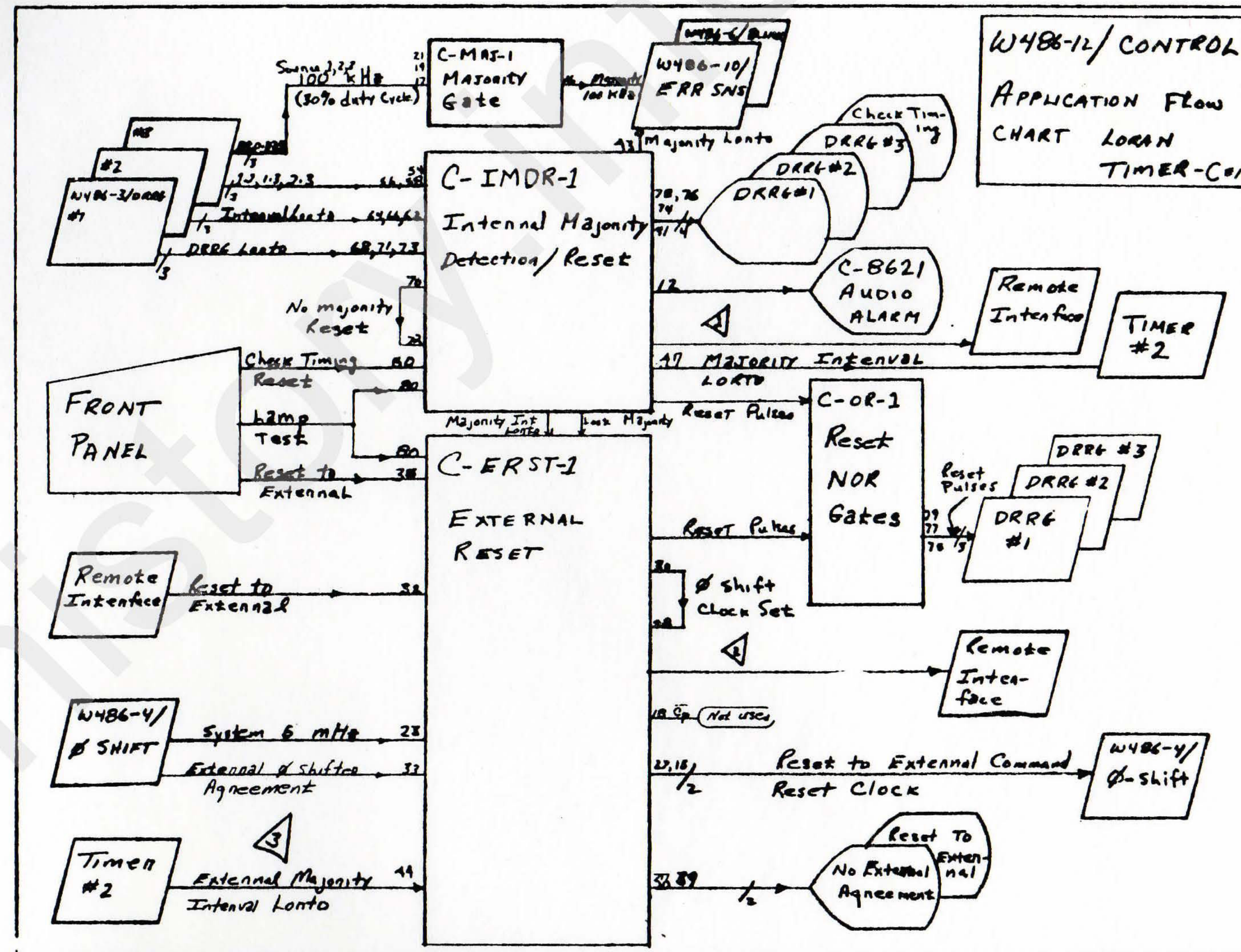
TOTAL PER BOARD 365.8

WO486-11/ETA Envelope Timing Adj.
Supplemental Information
12/10/71


W0486 12/CONTROL
Control module designed specifically for majority type control of three DRRG's or three phase shifters. All of the logic necessary for this control and status display is included on this module. The basic concept of the module is the comparison of d. c. signals representing the agreement of one pair of the three controlled units. In addition, external reset logic is provided to synchronize the controlled units to either an external pulse signal, an external phase shifter or both.
C AND 1 DRRG ERROR LOGIC
Combines lost signal levels from the DRRG's to determine which DRRG has malfunctioned or that no two of the DRRG's agree (NO MAJORITY condition). For example, if DRRG 1 malfunctions, the two input lines marked 1, 2 and 1, 3 will both be TRUE, thus passing through the A22C gate and lighting the "DRRG 1 JUMP" lamp. If A22 B, C, D gate outputs are FALSE, the NO MAJORITY gate, A14C will activate to generate an arbitrary reset to all three DRRG's.
C RST 1 RESET AND GATES
Enable the MAJORITY INTERVAL LORTO pulse to reset the DRRG determined by C AND 1 to have malfunctioned. The MAJORITY INTERVAL LORTO pulse is phase coded, hence this reset operation will correct any phase code jumps as well as time jumps among the DRRG's.
C RST 2 NO MAJORITY RESET LOGIC
Selects individual DRRG reset pulses or a NO MAJORITY reset pulse. This pulse is selected as the first DRRG LORTO to arrive at C OR 2. The single shot locks out the NO MAJORITY reset circuit for a period greater than two Loran periods to allow the DRRG pulse loss indicators to determine if a majority agreement has been achieved. At the end of this time period another reset attempt will be made if the NO MAJORITY CONDITION persists.
C OR 1 RESET NOR GATES
Digitally combine DRRG reset pulses from the internal check logic and the reset to external logic.
C-ALM-2
DRRG No 1 JUMP (78)
C-ALM-2
DRRG No 2 JUMP (76)
C-ALM-2
DRRG No 3 JUMP (74)
DRRG No. 1 RESET (79)
NO MAJORITY RESET INPUT (72)
NO MAJORITY RESET OUTPUT (70)
DRRG 2 RESET (77)
DRRG 3 RESET (75)
2 54 1,2
2 58 2,3
2 56 1,3
C ALM 2 MALFUNCTION ALARM
Actuates the output lamp driver if any abnormal (i.e., malfunction) condition exists among the on card or external check logic elements.
A1-6
A8-6
A8-6
A9-6
8
10
150mA
ALARM DRIVER (12)
ALARM LOGIC (7)
C OR 2 OR GATE
Develops NO MAJORITY RESET PULSE from DRRG 1, 2 or 3 LORTO
5
LOST MAJORITY OUTPUT
48
C MAJ 1 LORTO MAJORITY GATE
Provides a MAJORITY LORTO (not the INTERVAL MAJORITY LORTO) to all system cards such as Loran waveform generators etc.
LORTO DRRG No.1 73
71
LORTO DRRG No 2
68
LORTO DRRG No 3
TP-3, BLUE MAJORITY LORTO
MAJORITY LORTO (45)
MAJORITY LORTO (43)
C ALM 3 CHECK TIMING ALARM
Flip flop AMA is set by a NO MAJORITY condition and displays this to the operator as a CHECK TIMING indication. The operator must acknowledge this by actuating the CHECK TIMING RESET to clear the flip flop.
CHECK TIMING INDICATOR (9)
CHECK TIMING DRIVER (41)
CHECK TIMING RESET INPUT (50)
C1, .1uf
MAJORITY INTERVAL LORTO (47)
C MAJ 2 MAJORITY GATE
Generates logical majority of three inputs.
SOURCE 1 21
SOURCE 2 19
SOURCE 3 17
MAJORITY (16)
C OR 3 OR GATE/LINE DRIVER
Generates INTERVAL MAJORITY LORTO and provides a balanced line driver output for external use of this signal.
TP-5, WHITE
INTERVAL LORTO 1,2
66
64
62
1,3
2,3
52
C AND 2 EXTERNAL AGREEMENT LOGIC
Determines if the local LORTO agrees with the EXTERNAL LORTO by setting a flip-flop on the leading edge of the EXTERNAL pulse and resetting with the AND agreement of the two pulses. A23 NOR gate provides lockout of all EXTERNAL RESET logic in the event that no local MAJORITY exists. This feature prevents cold-start lockup between two timing systems.
C ALM 1 NO EXTERNAL AGREEMENT ALARM
Logically OR's no external agreement signals from either the pulse detector (C-AND-2) or the phase shifter detector.
NO EXTERNAL AGREEMENT DRIVER (39)
NO EXTERNAL AGREEMENT INDICATOR (11)
44 EXTERNAL MAJORITY INTERVAL LORTO
33 EXTERNAL Ø-SHIFTER AGREEMENT
C RST 3 EXTERNAL RESET LOGIC
Provides RESET TO EXTERNAL logic. This logic will slew an internal phase shifter to agree with an external phase shifter and reset the dynamic DRRG elements. Actuation of the front panel RESET TO EXTERNAL pushbutton sets A19B whose output enables the phase shifter reset mechanism. When the phase shifter agrees A18C changes state and sets the flip-flop composed of A24 gates. This output stops the DRRG dividers (actuates Parallel Enable) until this flip-flop is reset by the AND of the 5 MHz clock and the EXTERNAL INTERVAL MAJORITY LORTO. The divider is thus restarted precisely in time with the local 5 MHz and coarsely timed (within 200 ns) to the external MAJORITY pulse.
SYSTEM 5 MHz 23
30
Ø-SHIFT CLOCK SET OUTPUT
35
LOCAL RESET TO EXT.
32
REMOTE RESET TO EXTERNAL
Ø-SHIFT RESET TO EXTERNAL (27)
RESET TO EXTERNAL LOGIC (5)
RESET TO EXTERNAL DRIVER (37)
TP-1, RED INTERNAL CLOCK
C CLK 1 ASYNCHRONOUS CLOCK
Provides a source of independent 2 MHz clock signals to slew or reset W0486-/PHASE SHIFT - type phase shifters
28 CLOCK ENABLE
CP (18)
CP (15)
W0486-12/Control (Dated: 5-20-70)


C-AND-1 DRRG ERROR LOGIC
C-RST-1 RESET AND GATES
C-RST-2 NO MAJORITY RESET LOGIC
C-OR-1 RESET NOR GATES
C-OR-2 OR GATE
C-ALM-2 MALFUNCTION ALARM
C-ALM-3 CHECK TIMING ALARM
C-MAJ-1 MAJORITY GATE
C-MAJ-2 LORTO MAJORITY GATE
C-OR-3 OR GATE / LINE DRIVER
C-ERST-1 EXTERNAL RESET
C-AND-2 EXT. AGREEMENT LOGIC
C-ALM-1 NO EXTERNAL AGREEMENT ALARM
C-RST-3 EXTERNAL RESET LOGIC
C-CLK-1 ASYNCHRONOUS CLOCK
(REVISED 2-22-75)
(REVISED: 12-10-71)
W0486-12/Control (Dated: 5-20-70)





F·AG NOTES LORAN-A TIMER

1. Two malfunction indications are provided.
   1. Check Timing (9)
   2. Malfunction Alarm (7)
2. Two malfunction indications are provided
   1. Reset to External Armed (5)
   2. No External Agreement (11)
3. External Majority LORTO check pulse may be any FALSE 200 ns pulse which is delayed from Interval majority LORTO by 40 ± 5 ns.

CONTROL BOARD W0486-12A/ CONTROL (POWER REQUIREMENTS BASED ON MANUFACTURER'S SPEC)

MFRS PREFIX	IC TYPE PER DRWG	MFRS SUFFIX	NO USED	MFR	POWER SUPPLY Vcc PIN #	GND PIN #	CURRENT PKG	TOTAL CUR.
HGF	2002	9XX	7	FAIRCHILD	10	5	30.0	210.0
N	8880	A	8	SIGNETICS	14	7	14.0	112.0
N	8875	A	1	SIGNETICS	14	7	21.0	21.0
N	8885	A	1	SIGNETICS	14	7	28.4	28.4
U6A	9601	59X	2	FAIRCHILD	14	7	25.0	50.0
N	8870	A	2	SIGNETICS	4	11	17.7	35.4
DM	8830	-	1	NATIONAL	14	7	36.0	36.0
N	8828	A	2	SIGNETICS	14	7	22.0	44.0
N	8878	A	2	SIGNETICS	14	7	8.0	16.0

TOTAL PER BOARD 552.8 MA

FLAG NOTES LORAN-C TIMER

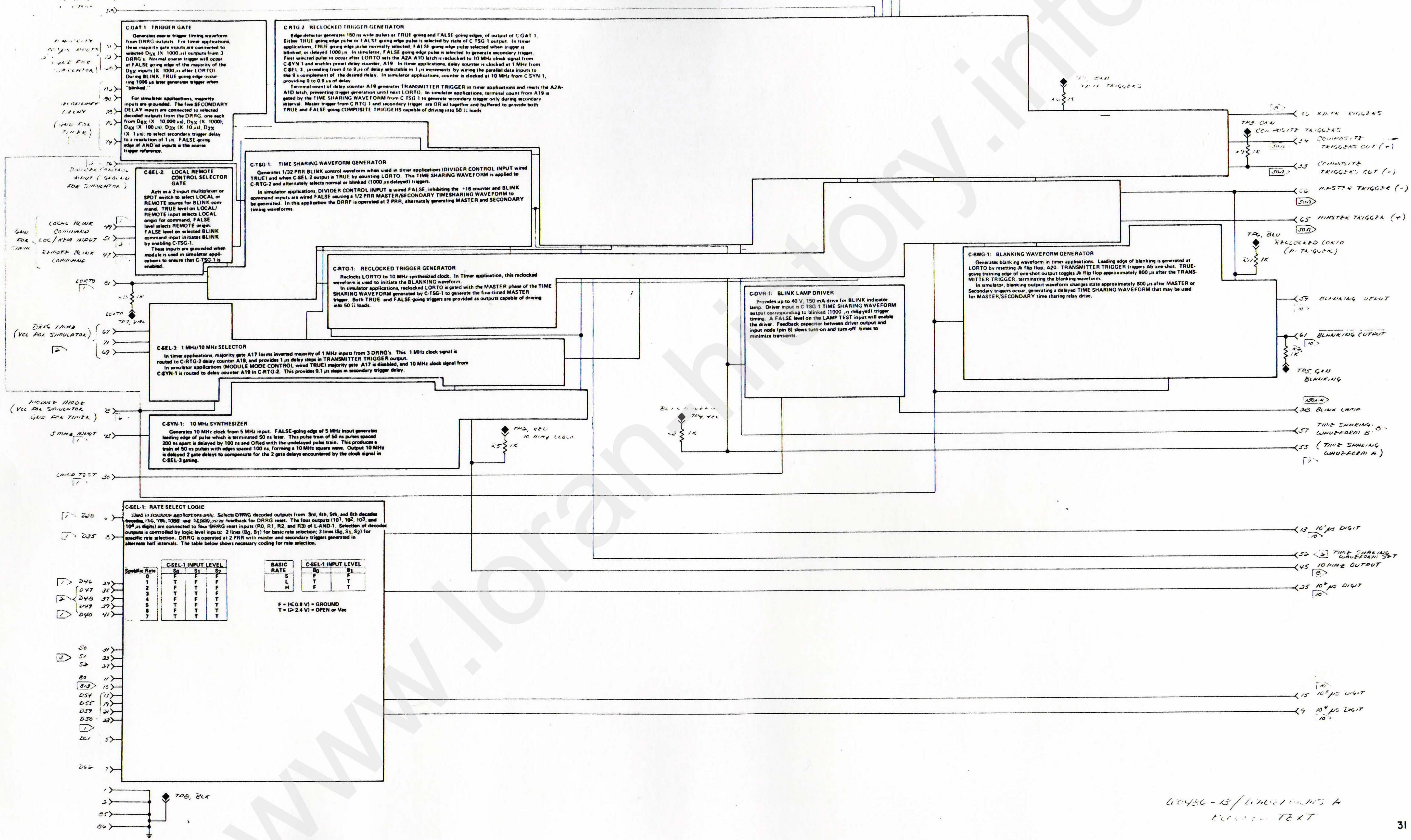
1. Two malfunction indications are provided.
   1. Check Timing (9)
   2. Malfunction Alarm (7)
2. Two malfunction indications are provided.
   1. Reset to External Armed (5)
   2. No External Agreement (11)
3. External Majority Interval LORTO check pulse may be any FALSE 200 ns pulse which is delayed from Interval majority Interval LORTO by 40 ± 5. ns.

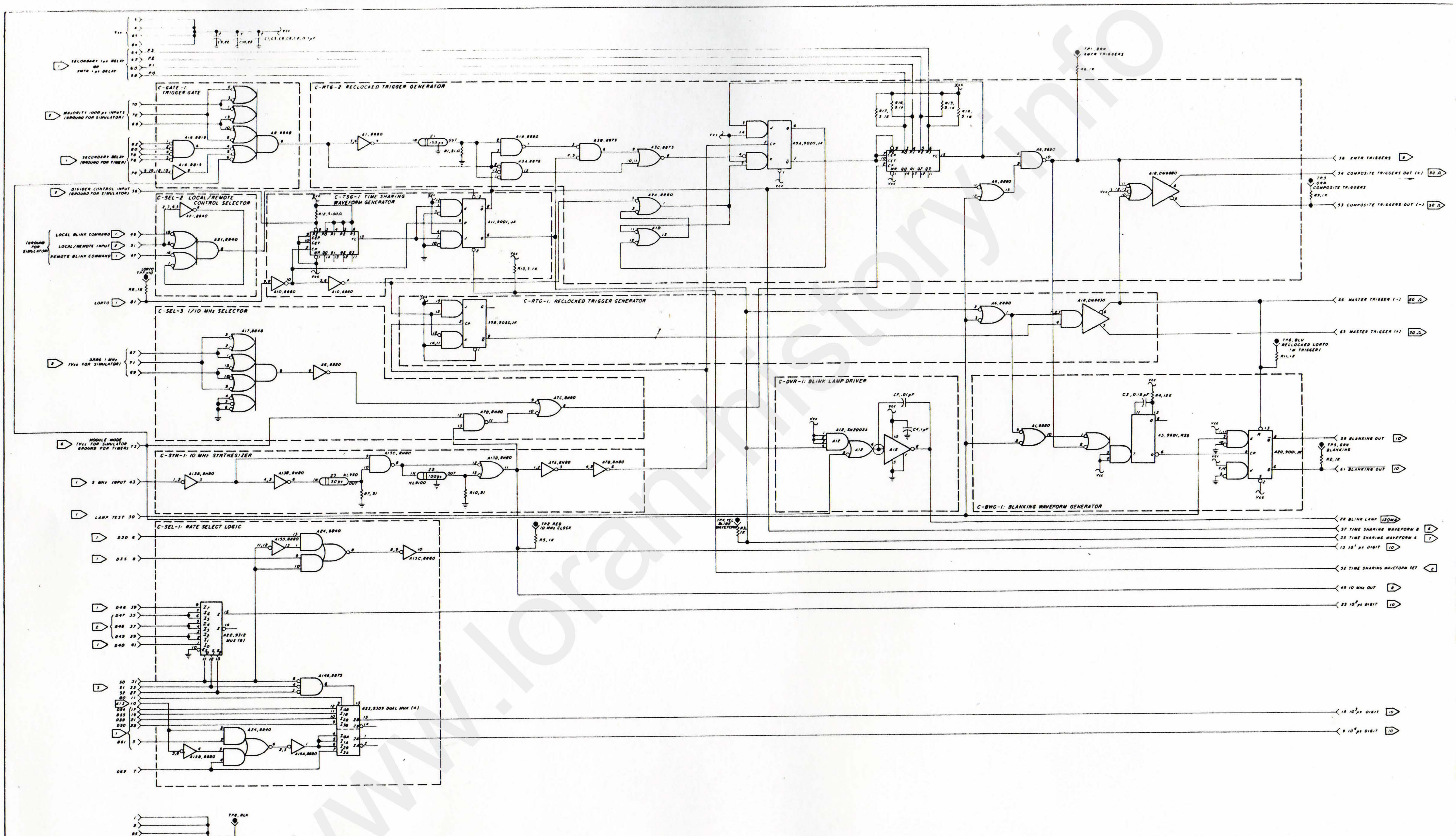
W0486-12/Control 12-10-71
Supplemental Information

W0486-13/WAVEFORMS A

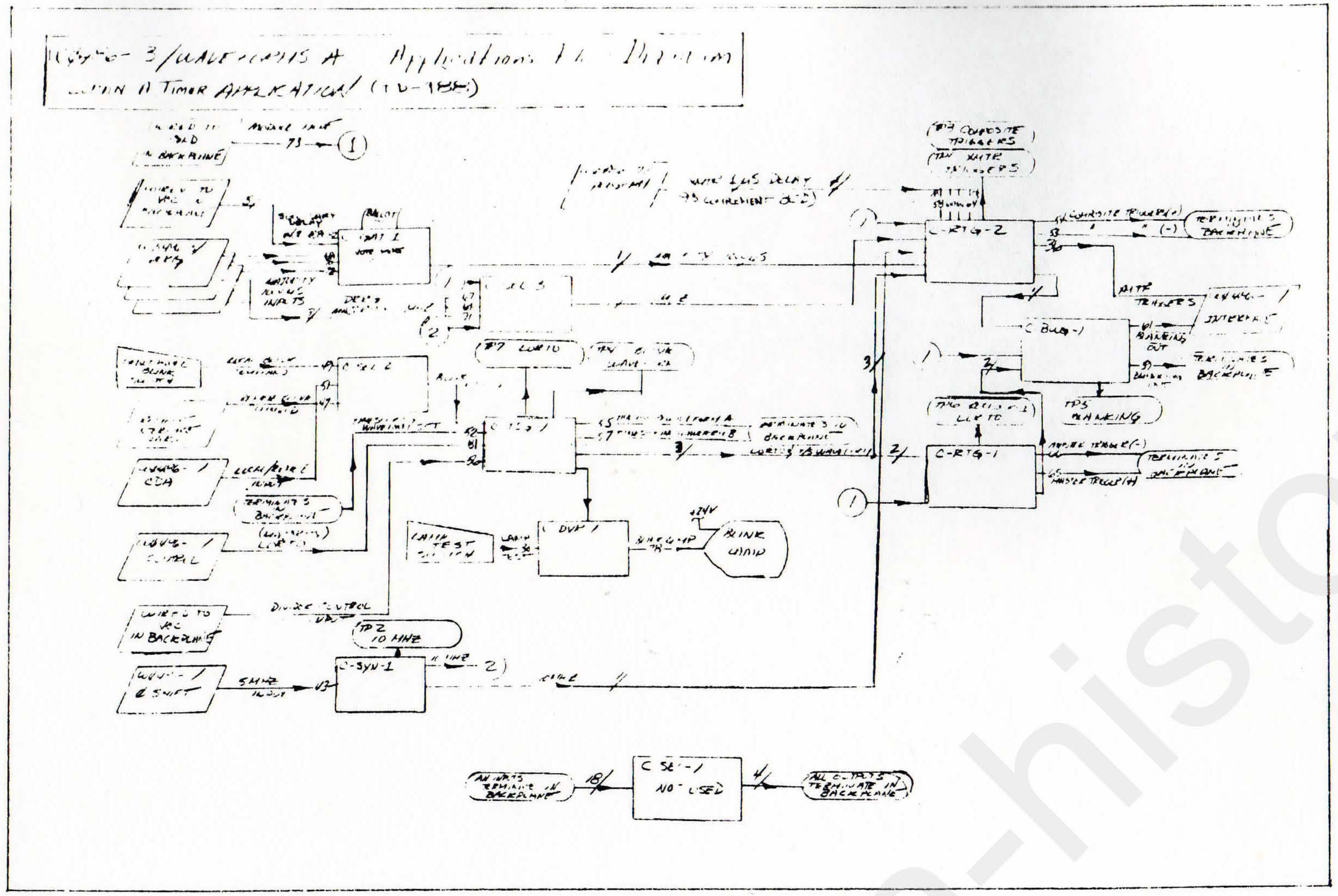
Generates Loran A signal format (BLANKING, TRANSMITTER TRIGGER and BLINK) from majority of decoded outputs of three W0486-3/DRRG modules in timer applications. TRANSMITTER trigger may be delayed in 1 μs steps over a range of 0 to 9 μs from the internal trigger reference. When a local path compensation loop is used, TRANSMITTER TRIGGER timing may be adjusted to maximize the correction range of the compensation loop.

In simulator applications, module generates both master and secondary triggers. Master-secondary delay may be varied in 100 ns increments. A delayed BLANKING waveform is provided for master/secondary time sharing. Logic is provided to decode 5 input lines to determine W0486-3/DRRG feedback and set all Loran-A PRR's.





W0486-13 / WAVEFORMS A SCHEMATIC



W0486-13/WVFMS-A (POWER REQUIREMENTS BASED ON MANUFACTURERS SPEC.)

MFRS PREFIX	IC TYPE	MFRS SUFFIX	MFR	NO USED	SUPPLY POWER VCC PIN #	GND PIN #	CURRENT PER PACK	TOTAL CURRENT
U7B	9312	59X	FAIRCHILD	1	16	8	27.0	27.0
N	8870	A	SIGNETICS	2	14	7	11.0	22.0
N	8875	A	SIGNETICS	2	14	7	21.0	42.0
U6B	9309	59X	FAIRCHILD	1	16	8	30.0	30.0
N	8880	A	SIGNETICS	5	14	7	14.0	70.0
N	8848	A	SIGNETICS	2	14	7	8.0	16.0
N	8815	A	SIGNETICS	1	14	7	16.0	16.0
U6A	9020	59X	FAIRCHILD	1	16	8	28.0	28.0
U6B	9310	59X	FAIRCHILD	1	16	8	70.0	70.0
U7B	9316	59X	FAIRCHILD	1	16	8	70.0	70.0
U6B	9001	59X	FAIRCHILD	2	14	7	14.0	28.0
U6A	9601	59X	FAIRCHILD	1	14	7	25.0	25.0
H6F	2002	9XX	FAIRCHILD	1	10	5	30.0	30.0
N	8H80	A	SIGNETICS	2	14	7	26.0	52.0
DM	8830	N	NATIONAL	1	14	7	36.0	36.0

TOTAL PER BOARD 532 MA

W0486-13/WVFMS-A 12-10-71

Supplemental Information

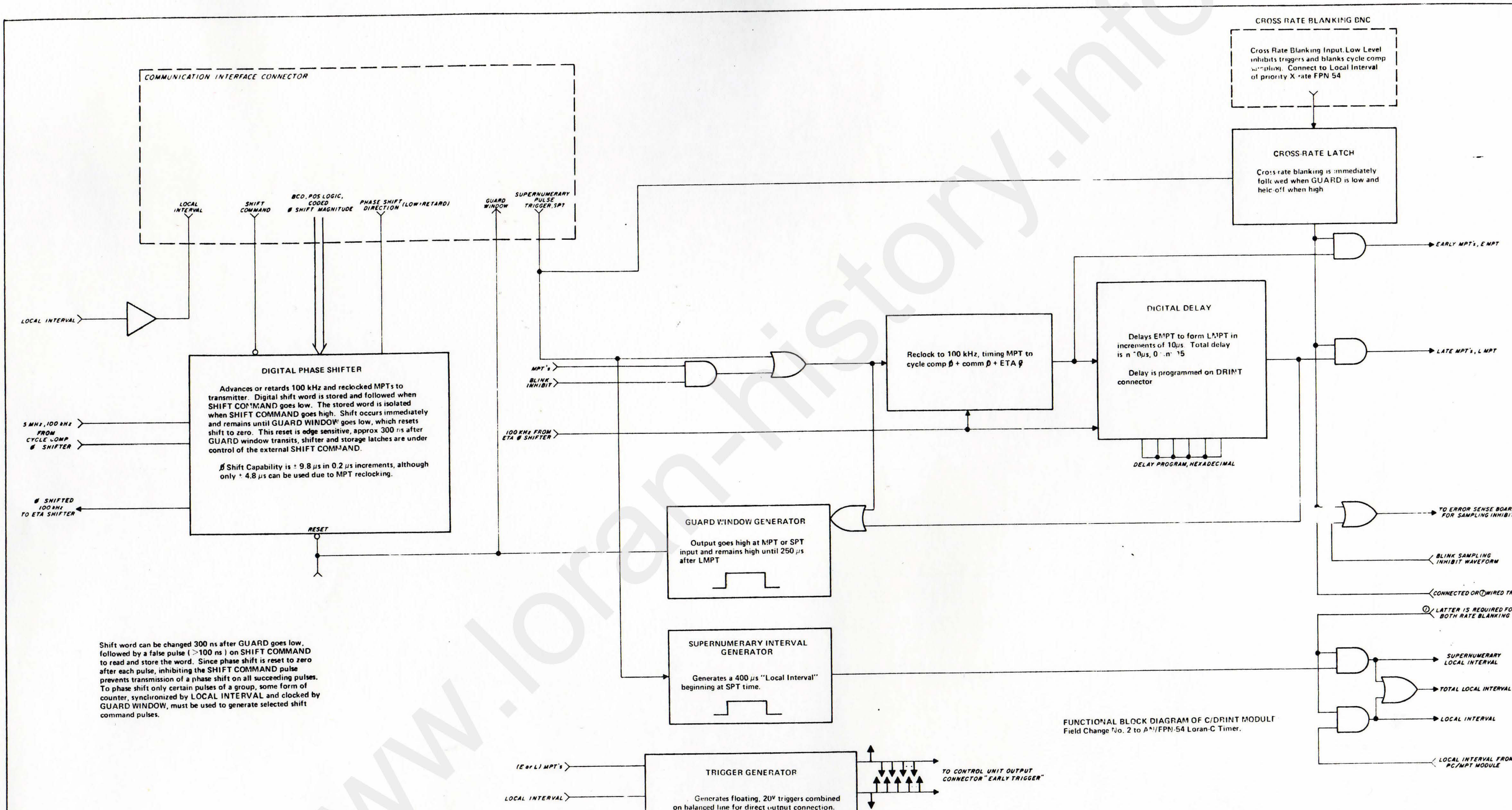
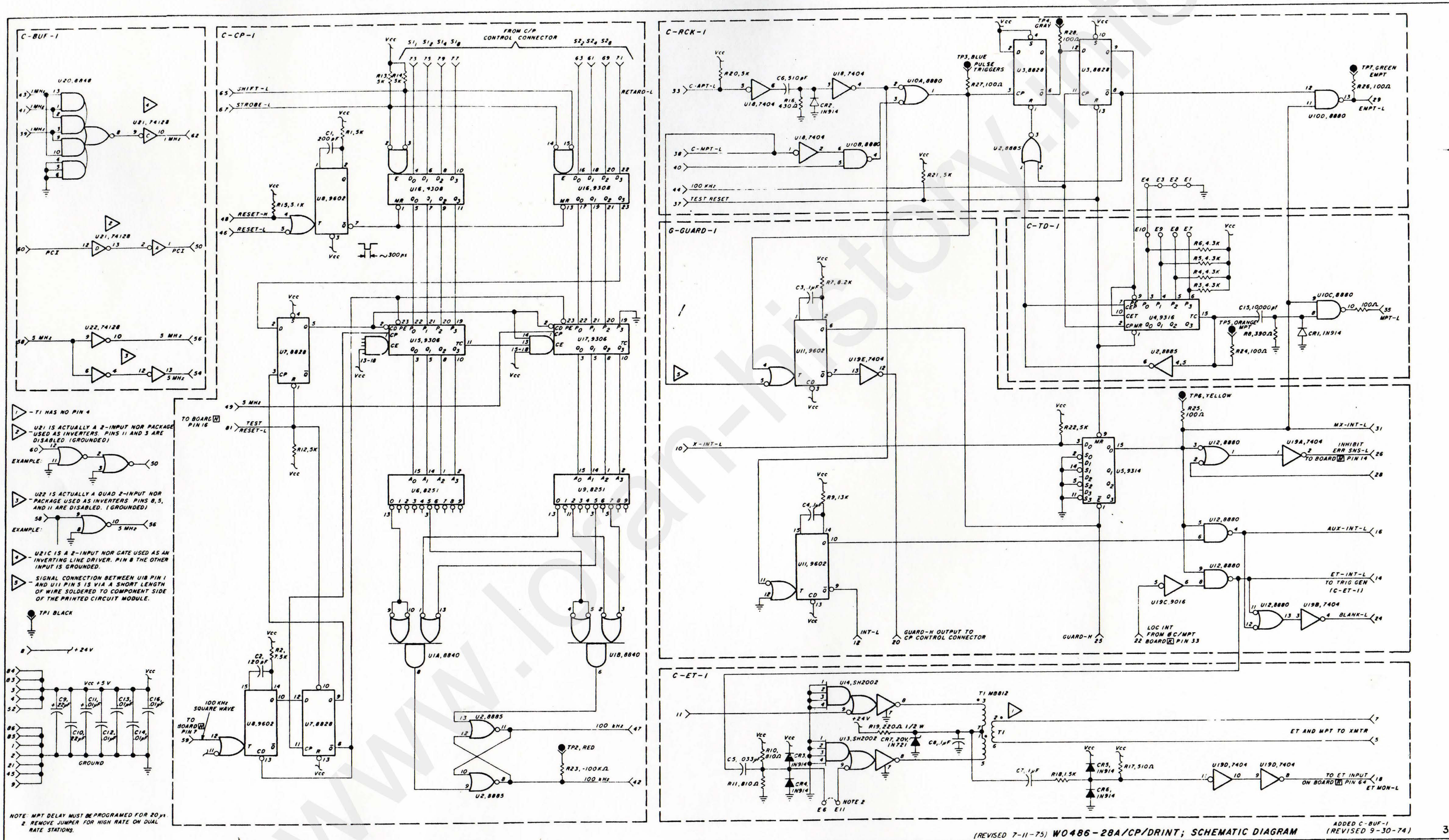
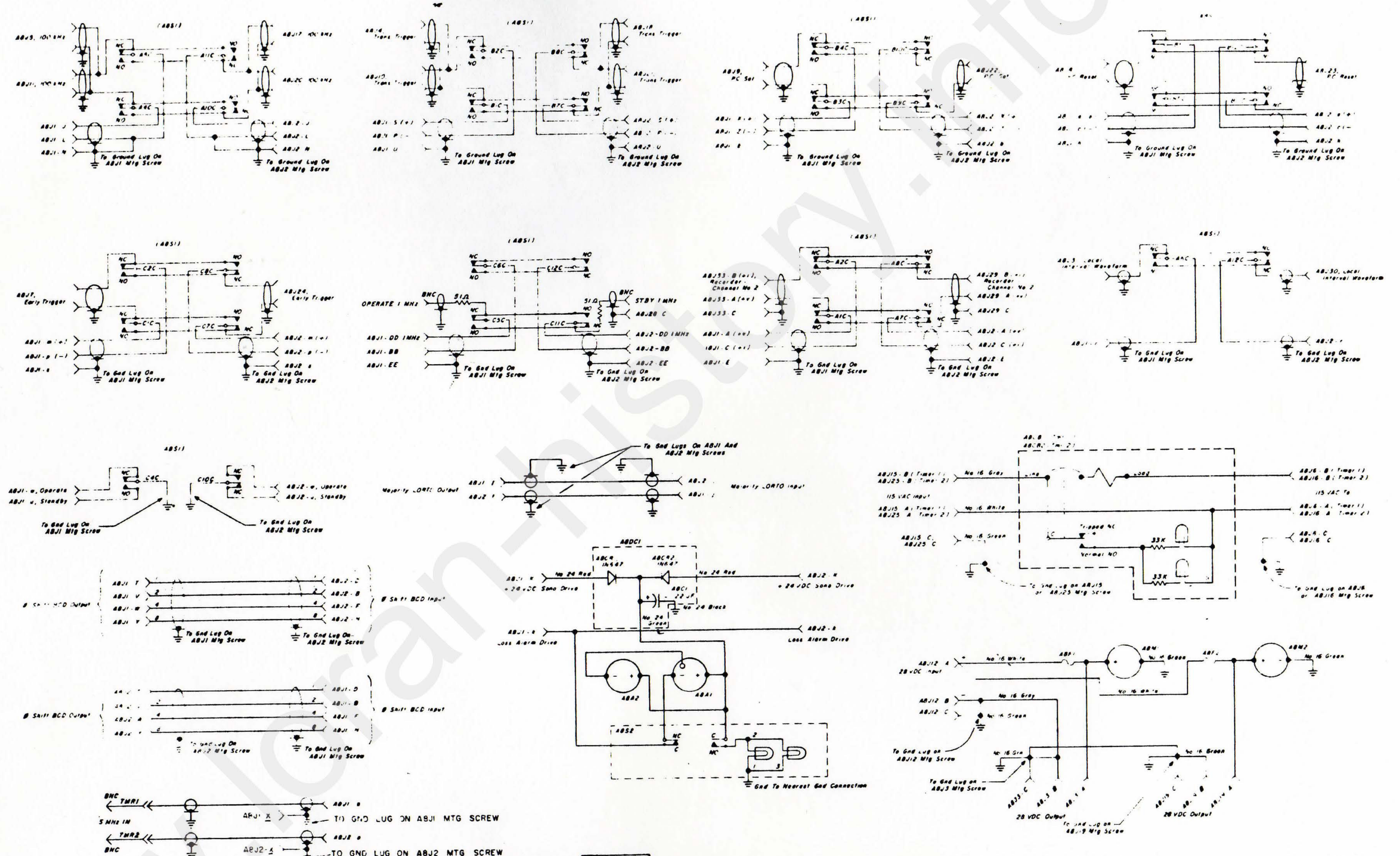


Figure 5-3
DRINT, Functional Block Diagram

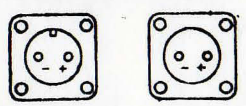


C-BUF-1
C-CP-1
C-RCK-1
G-GUARD-1
C-TD-1
C-ET-1
FROM C/P CONTROL CONNECTOR
1 - T1 HAS NO PIN 4
2 - U21 IS ACTUALLY A 2-INPUT NOR PACKAGE USED AS INVERTERS. PINS 11 AND 3 ARE DISABLED (GROUNDED)
EXAMPLE:
3 - U22 IS ACTUALLY A QUAD 2-INPUT NOR PACKAGE USED AS INVERTERS. PINS 8, 5, AND 11 ARE DISABLED. (GROUNDED)
EXAMPLE:
4 - U21C IS A 2-INPUT NOR GATE USED AS AN INVERTING LINE DRIVER. PIN 8 THE OTHER INPUT IS GROUNDED.
5 - SIGNAL CONNECTION BETWEEN U18 PIN 1 AND U11 PIN 5 IS VIA A SHORT LENGTH OF WIRE SOLDERED TO COMPONENT SIDE OF THE PRINTED CIRCUIT MODULE.
TP1 BLACK
+24V
Vcc +5 V
GROUND
NOTE: MPT DELAY MUST BE PROGRAMED FOR 20 μs.
2. REMOVE JUMPER FOR HIGH RATE ON DUAL RATE STATIONS.
(REVISED 7-11-75) W0486-28A/CP/DRINT; SCHEMATIC DIAGRAM
ADDED C-BUF-1 (REVISED 9-30-74)

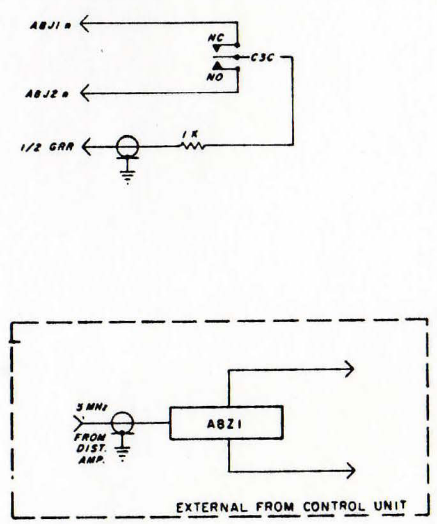


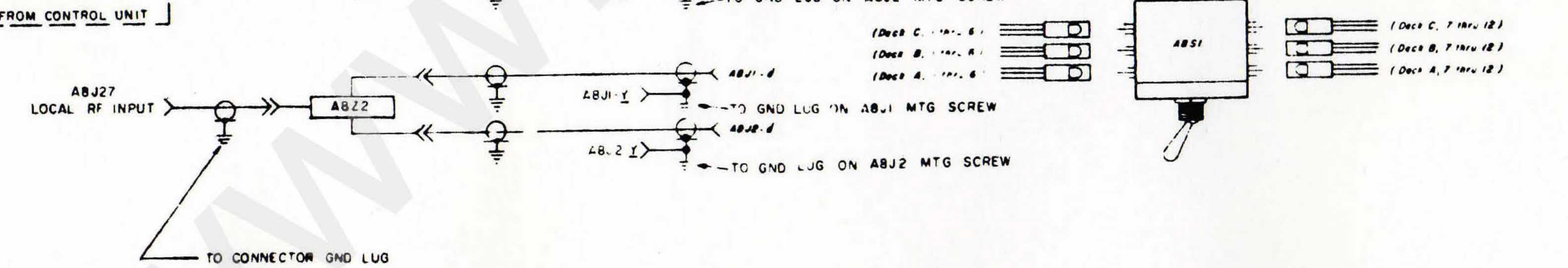
NOTES:

1. ALL CONNECTIONS FROM SWITCH A8S1 TO BACK PANEL SHALL BE MADE WITH TYPE E TEFLON, ALUMINIZED MYLAR SHIELDED; NO. 24 TWISTED PAIR WITH NO. 24 DRAIN WIRE.
2. ALL NO. 24 AND NO. 16 WIRE USED FOR RUNS AND JUMPERS SHALL BE TYPE E TEFLON INSULATED.
3. NEGATIVE TERMINALS ON METERS A8M1 AND A8M2 SHALL BE CONNECTED TO NEAREST AVAILABLE GROUND CONNECTIONS.
4. WIRE TWIN-AX CONNECTORS (VIEW FROM REAR OF CONTROL PANEL) AS FOLLOWS:

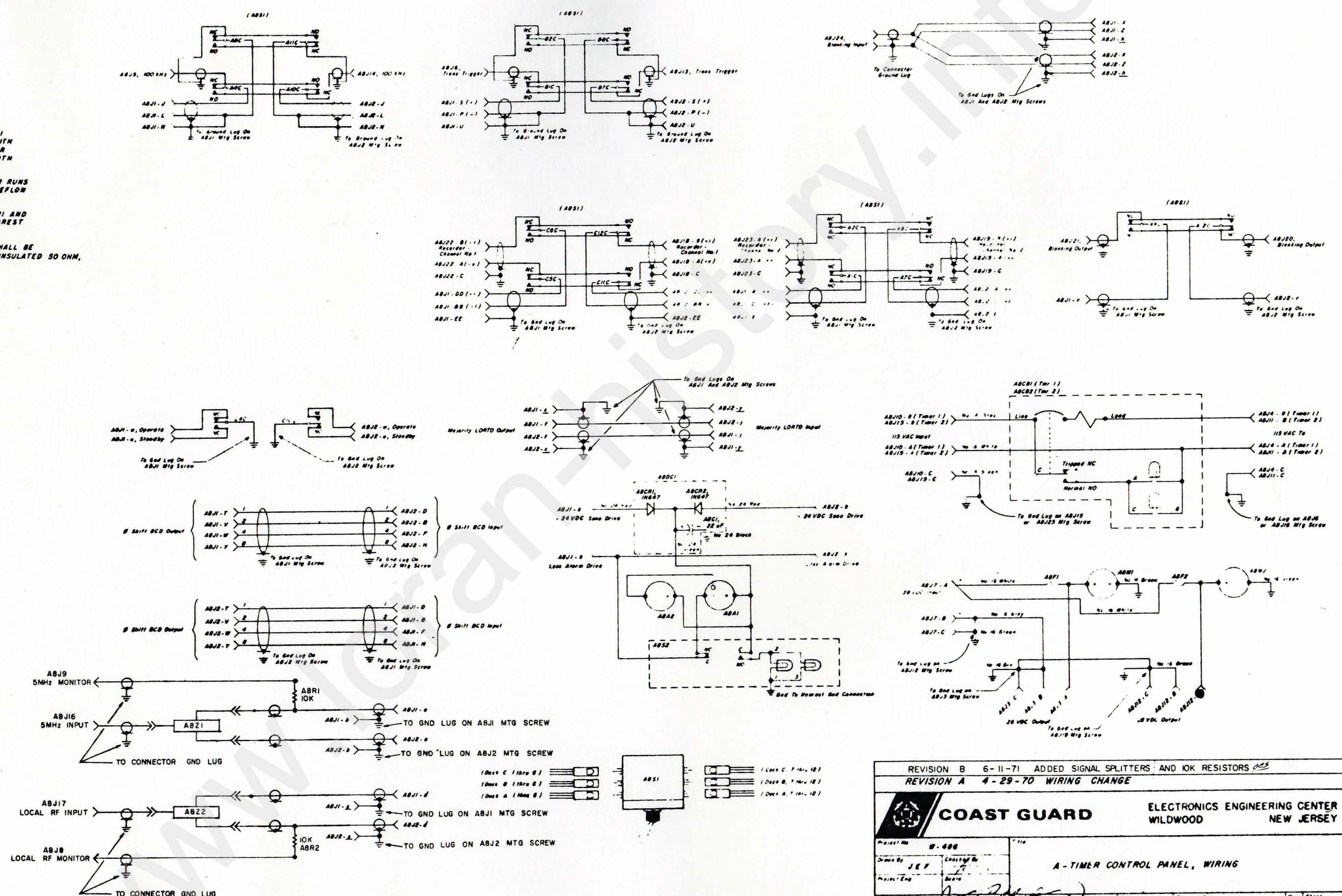


5. PARALLEL CONNECTIONS BETWEEN A8J5 - A8J11, A8J17 - A8J20, A8J4 - A8J10, AND A8J18 - A8J21 SHALL BE MADE ON THE WIRING SIDE OF THESE CONNECTORS.
6. 5 MHZ AND LOCAL RF CONNECTIONS SHALL BE MADE USING RG-178B/U TEFLON INSULATED, 50 OHM, MINIATURE COAXIAL CABLE.





REVISION A 6-11-71 ADDED SIGNAL SPLITTERS AND 10K RESISTORS CCS				
COAST GUARD	ELECTRONICS ENGINEERING CENTER WILDWOOD NEW JERSEY			
Project No W-486	Title C-TIMER CONTROL PANEL, WIRING			
Drawn By J.E.F.	Checked By			
Project Eng	Scale			
Approved By [signature] COMMANDING OFFICER USCG	Date MAR. 9, '70	Drawing No 486-C-133	Rev A	Sheet 1 of 1



NOTES:

1. ALL CONNECTIONS FROM SWITCH A8S1 TO BACK PANEL SHALL BE MADE WITH TYPE E TEFLON, ALUMINIZED MYLAR SHIELDED, NO 24 TWISTED PAIR WITH NO 24 DRAIN WIRE

2. ALL NO 24 AND NO 16 WIRE USED FOR RUNS AND JUMPERS SHALL BE TYPE E TEFLON INSULATED

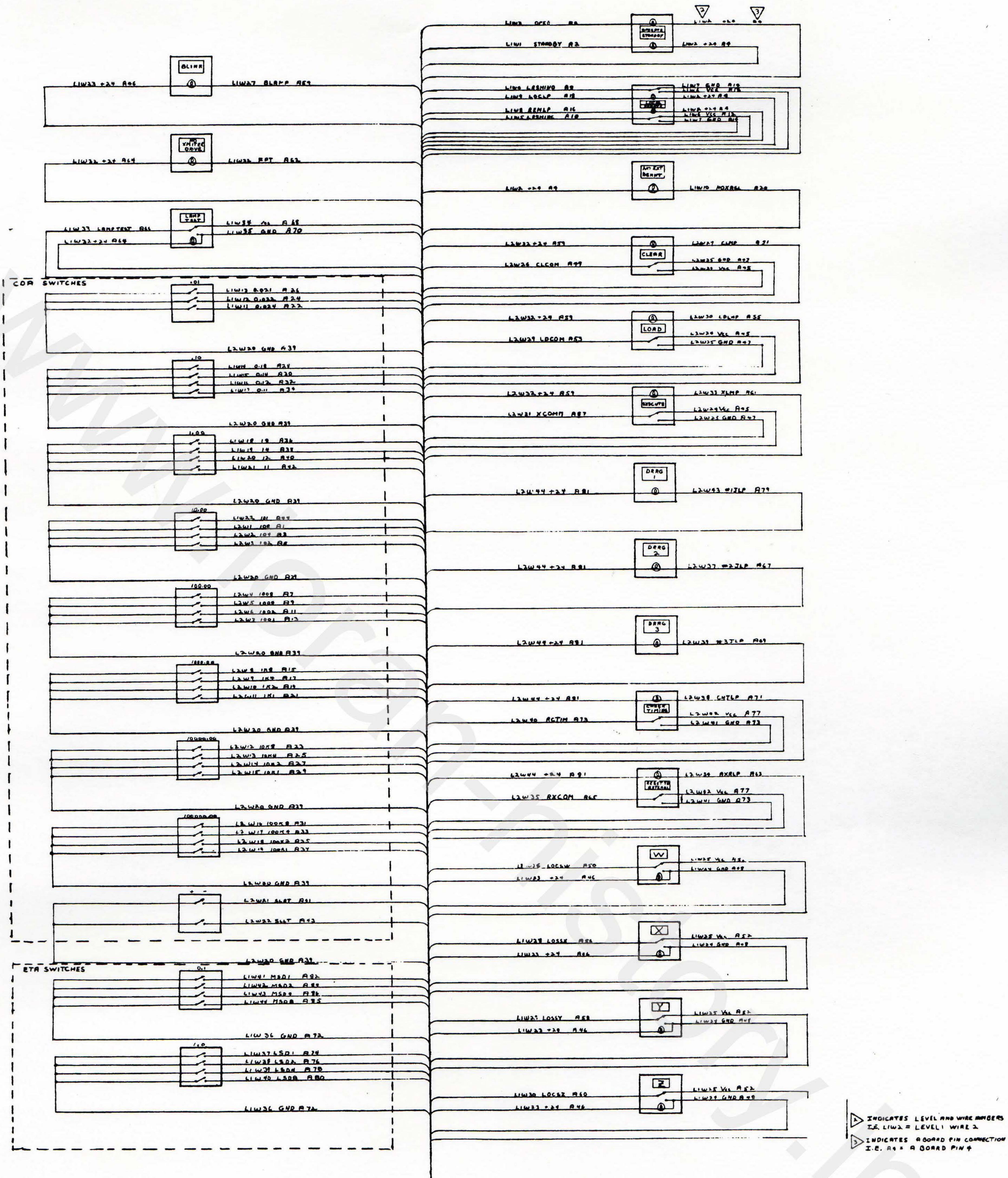
3. NEGATIVE TERMINALS ON METERS A8M1 AND A8M2 SHALL BE CONNECTED TO NEAREST AVAILABLE GROUND CONNECTIONS

4. 5 MHZ AND LOCAL RF CONNECTIONS SHALL BE MADE USING RG-178B/U, TEFLON INSULATED 50 OHM, MINIATURE COAXIAL CABLE

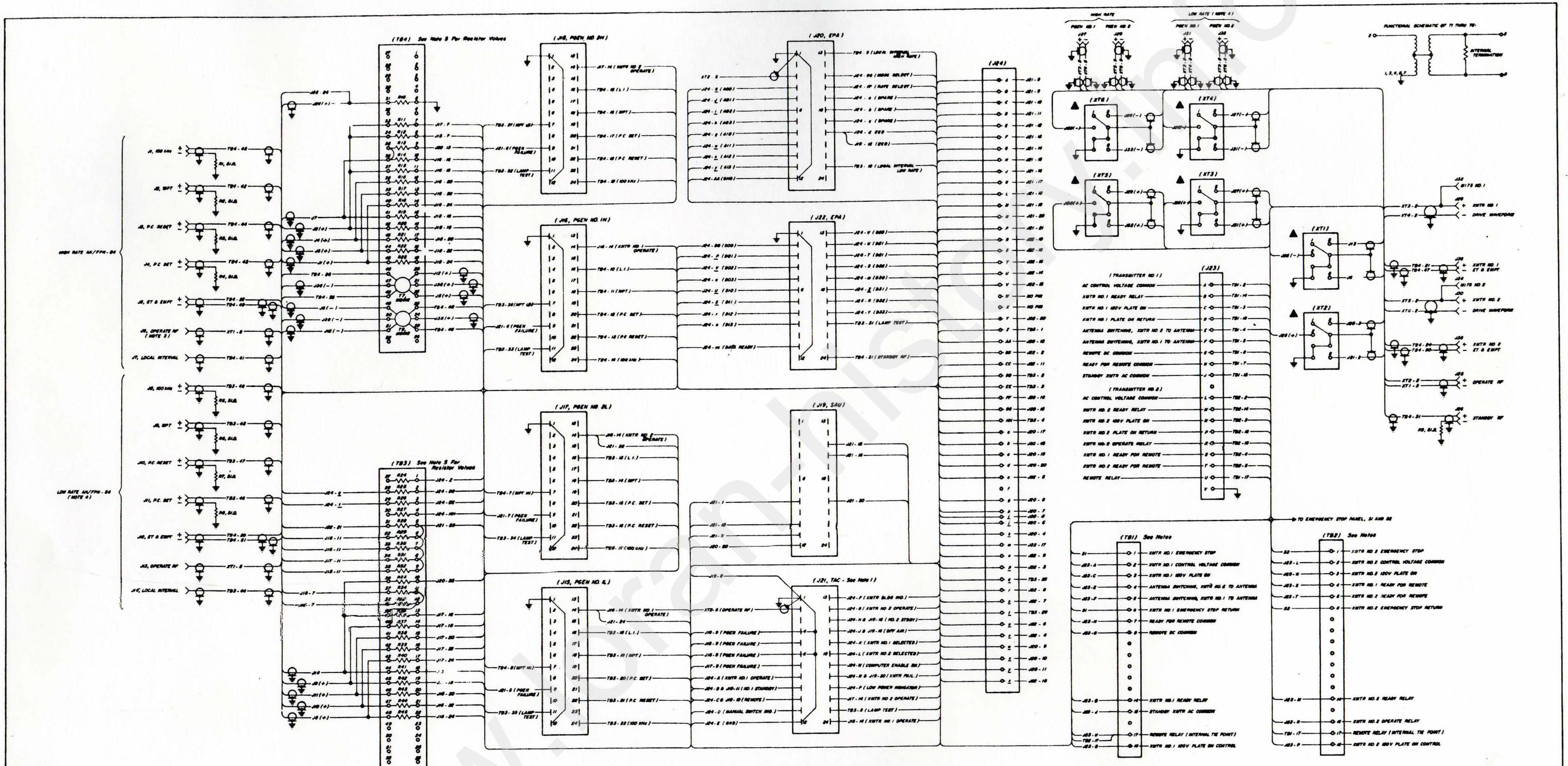
REVISION B	6-11-71 ADDED SIGNAL SPLITTERS AND 10K RESISTORS
REVISION A	4-29-70 WIRING CHANGE

COAST GUARD — ELECTRONICS ENGINEERING CENTER, WILDWOOD, NEW JERSEY

Project No: W-486	Title: A-TIMER CONTROL PANEL, WIRING		
Drawn By: J.E.F	Checked By		
Project Eng	Scale		
Approved By: COMMANDING OFFICER USCG	Date: MAR. 9, '70	Drawing No: 486-C-130	Rev: B — Sheet 1 of 1



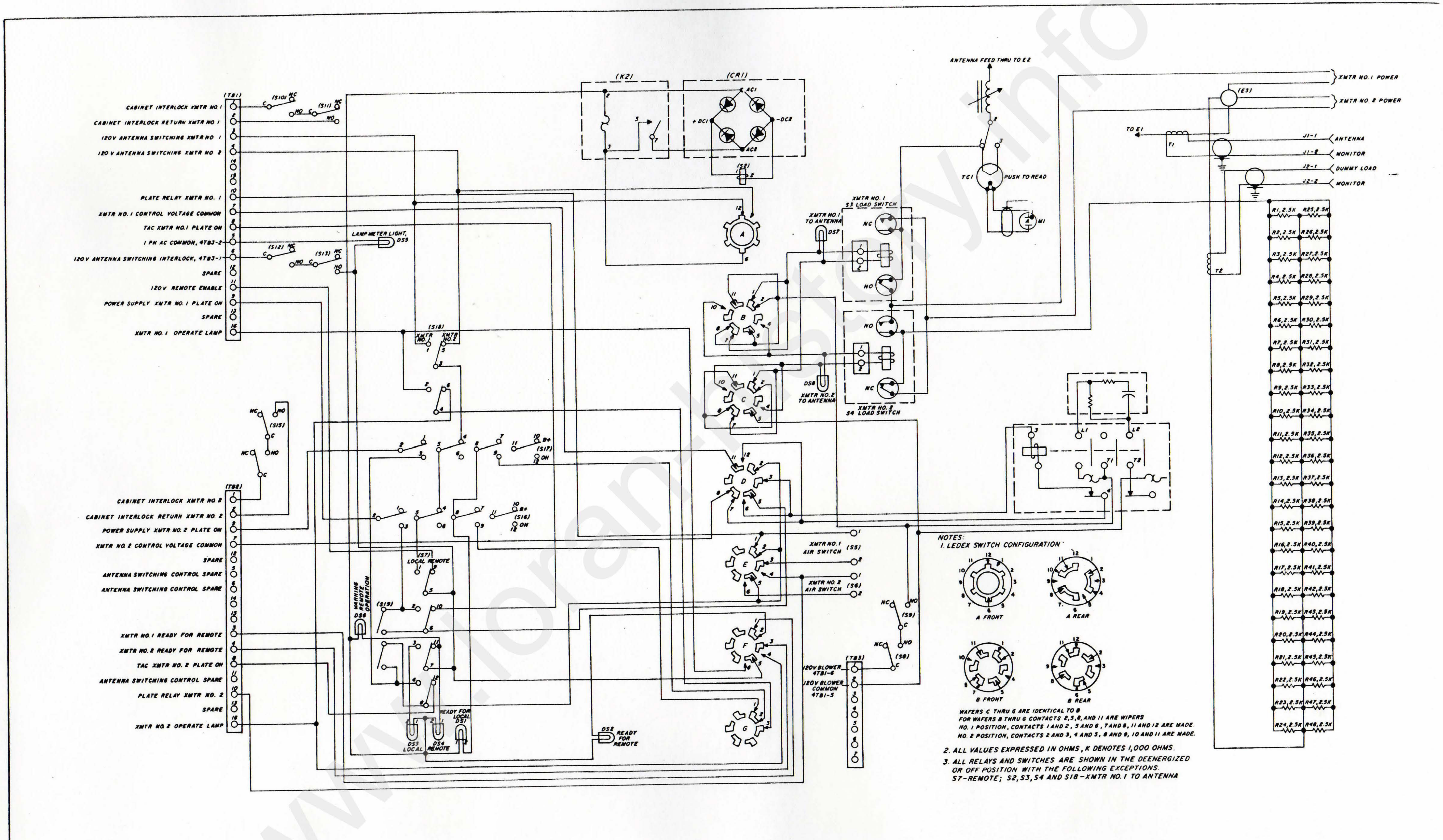
TD-989
FRONT PANEL WIRING DIAGRAM



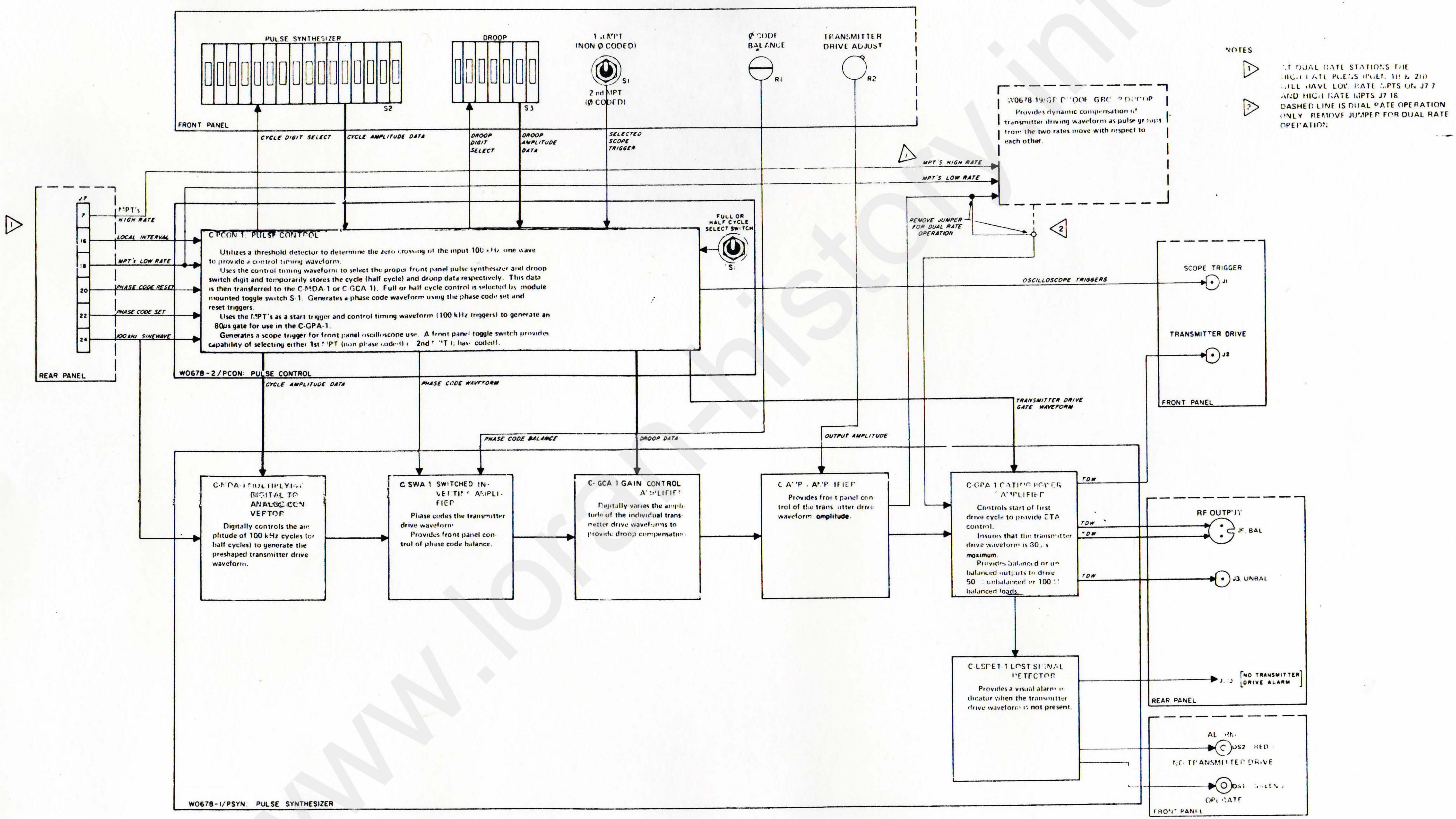
NOTES:

1. FOR DUAL-RATE OPERATION, REMOVE JUMPER WIRES J21-1 TO J21-4 AND J21-1 TO J21-6.
2. FOR SINGLE RATE OPERATION, TERMINATE WITH 80 Ω.
3. AT SINGLE RATE STATIONS USE LOW RATE PORTS.
4. R1-10 AND R24-27 = 51Ω
   R11, 12, 15 - 17, 20 - 22, 34, 36, 37 - 39, AND 42 - 44 = 680Ω
   R13, 14, 19, 29 - 33, 40, AND 42 - 44 = 180Ω
   R18, 23, 40, AND 45 = 75Ω
5. FOR USE WITH THE AN/FPN-39 TRANSMITTER, CONNECT JUMPERS AS INDICATED: TB1-8 TO TB1-17, TB1-14 TO TB1-15, TB1-14 TO TB2-14, TB2-5 TO TB2-16
6. FOR USE WITH THE AN/FPN-42 TRANSMITTER, CONNECT JUMPER FROM TB1-8 TO TB1-17
7. FOR USE WITH THE AN/FPN-44 TRANSMITTER, CONNECT JUMPERS AS INDICATED: TB1-5 TO TB2-7, TB1-6 TO TB1-18, TB1-18 TO TB2-18, TB2-6 TO TB2-16

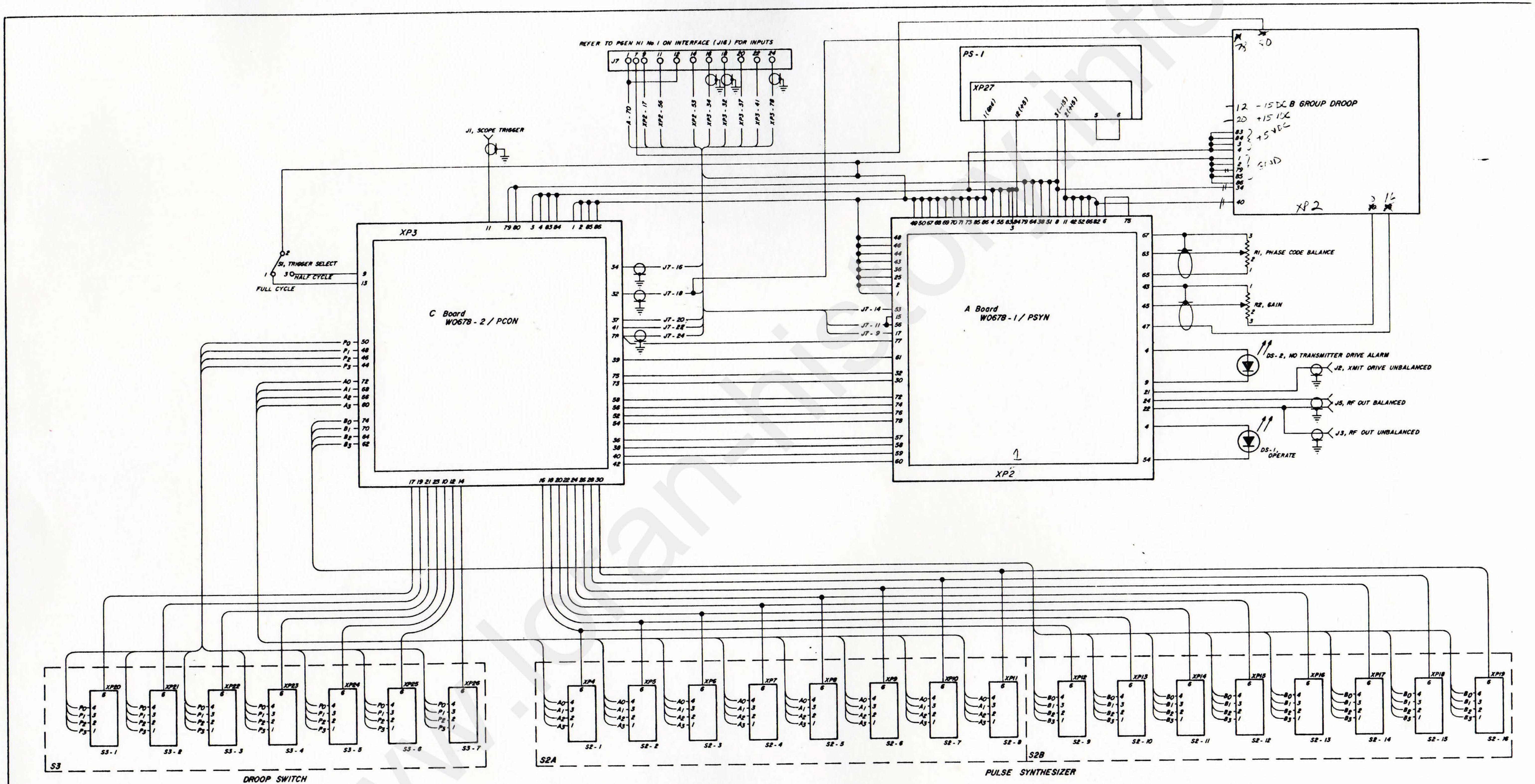
TCS INTERFACE UNIT; WIRING DIAGRAM



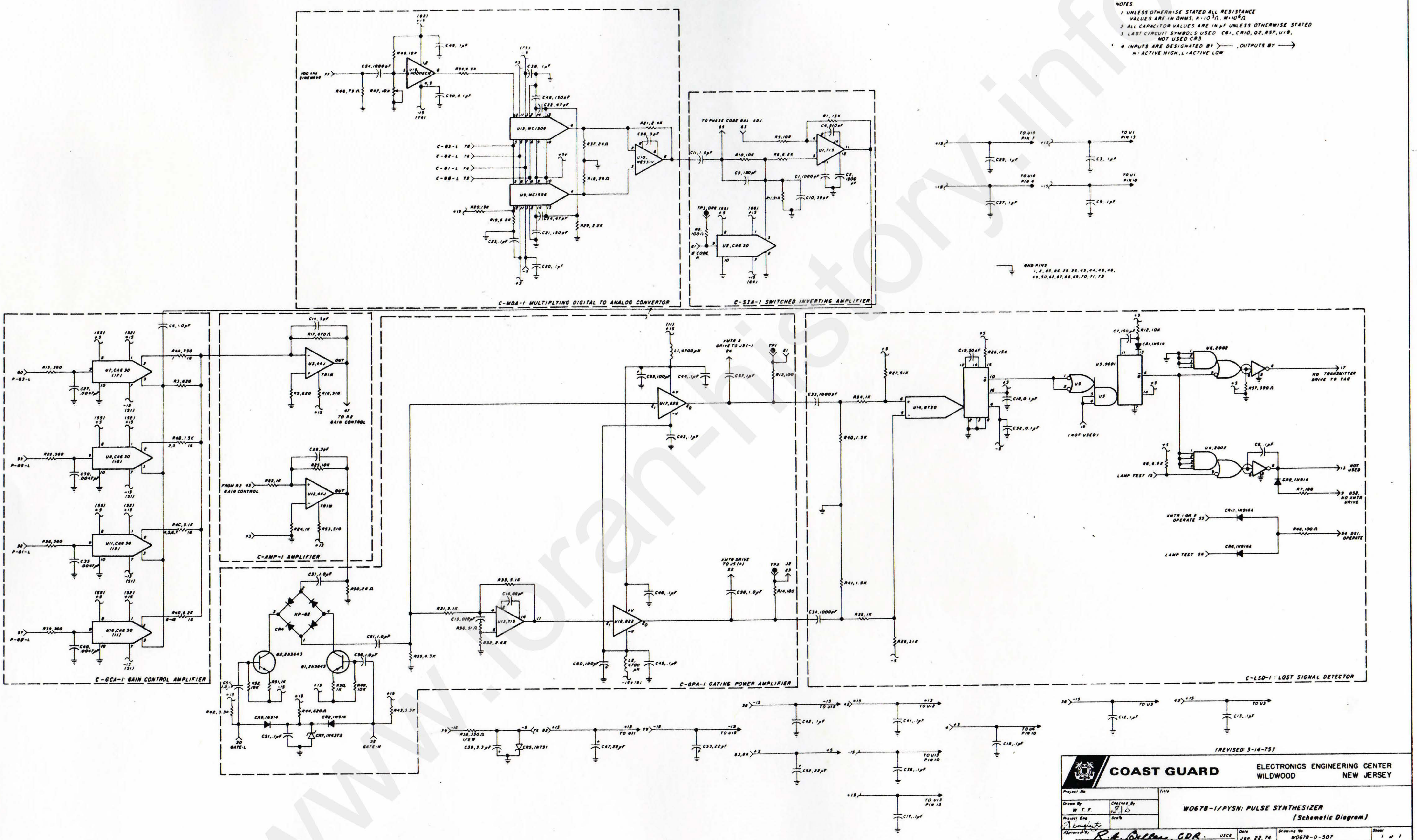
ANTENNA COUPLER CU-807/FPN-42 WIRING DIAGRAM

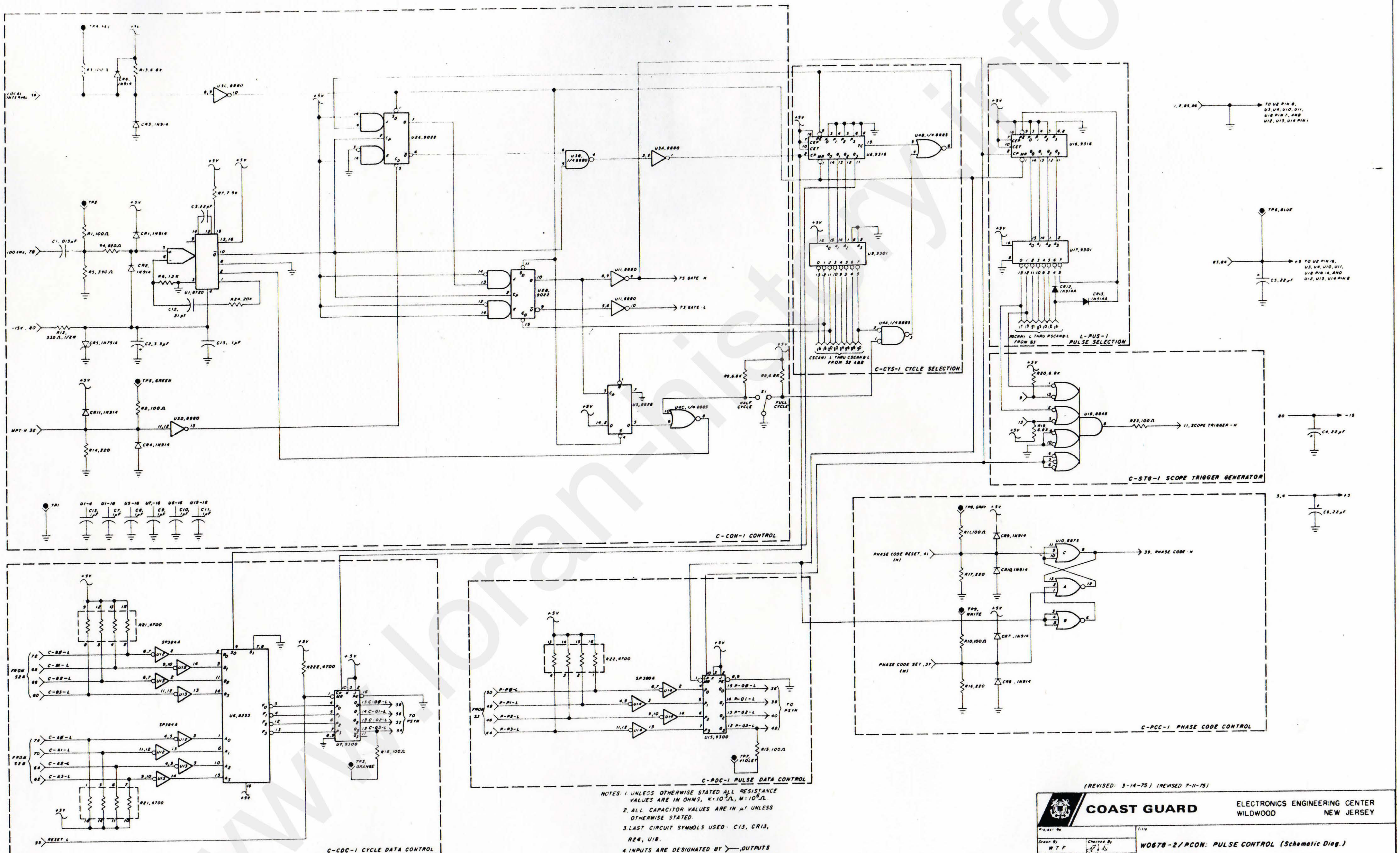


PULSE SYNTHESIZER
S2
DROOP
S3
1st MPT (NON Ø CODED)
S1
2nd MPT (Ø CODED)
Ø CODE BALANCE
R1
TRANSMITTER DRIVE ADJUST
R2
FRONT PANEL
CYCLE DIGIT SELECT
CYCLE AMPLITUDE DATA
DROOP DIGIT SELECT
DROOP AMPLITUDE DATA
SELECTED SCOPE TRIGGER
NOTES
DASHED LINE IS DUAL RATE OPERATION ONLY. REMOVE JUMPER FOR DUAL RATE OPERATION.
Provides dynamic compensation of transmitter driving waveform as pulse groups from the two rates move with respect to each other.
MPT'S HIGH RATE
MPT'S LOW RATE
REMOVE JUMPER FOR DUAL RATE OPERATION
J7
MPT's HIGH RATE
LOCAL INTERVAL
MPT's LOW RATE
PHASE CODE RESET
PHASE CODE SET
100 kHz SINEWAVE
REAR PANEL
FULL OR HALF CYCLE SELECT SWITCH
C-PCON-1 PULSE CONTROL
Utilizes a threshold detector to determine the zero crossing of the input 100 kHz sine wave to provide a control timing waveform.
Uses the control timing waveform to select the proper front panel pulse synthesizer and droop switch digit and temporarily stores the cycle (half cycle) and droop data respectively. This data is then transferred to the C-MDA-1 or C-GCA-1. Full or half cycle control is selected by module mounted toggle switch S-1. Generates a phase code waveform using the phase code set and reset triggers.
Uses the MPT's as a start trigger and control timing waveform (100 kHz triggers) to generate an 80μs gate for use in the C-GPA-1.
Generates a scope trigger for front panel oscilloscope use. A front panel toggle switch provides capability of selecting either 1st MPT (non phase coded) or 2nd MPT (phase coded).
W0678-2/PCON: PULSE CONTROL
OSCILLOSCOPE TRIGGERS
SCOPE TRIGGER
J1
TRANSMITTER DRIVE
J2
FRONT PANEL
CYCLE AMPLITUDE DATA
PHASE CODE WAVEFORM
TRANSMITTER DRIVE GATE WAVEFORM
PHASE CODE BALANCE
DROOP DATA
OUTPUT AMPLITUDE
C-SWA-1 SWITCHED INVERTING AMPLIFIER
Phase codes the transmitter drive waveform.
Provides front panel control of phase code balance.
C-GCA-1 GAIN CONTROL AMPLIFIER
Digitally varies the amplitude of the individual transmitter drive waveforms to provide droop compensation.
Provides front panel control of the transmitter drive waveform amplitude.
Controls start of first drive cycle to provide ETA control.
Insures that the transmitter drive waveform is 80μs maximum.
TDW
RF OUTPUT
J5, BAL
J3, UNBAL
Digitally controls the amplitude of 100 kHz cycles (or half cycles) to generate the preshaped transmitter drive waveform.
Provides a visual alarm indicator when the transmitter drive waveform is not present.
NO TRANSMITTER DRIVE ALARM
REAR PANEL
NO TRANSMITTER DRIVE
FRONT PANEL
W0678-1/PSYN: PULSE SYNTHESIZER



PULSE GENERATOR WIRING DIAGRAM

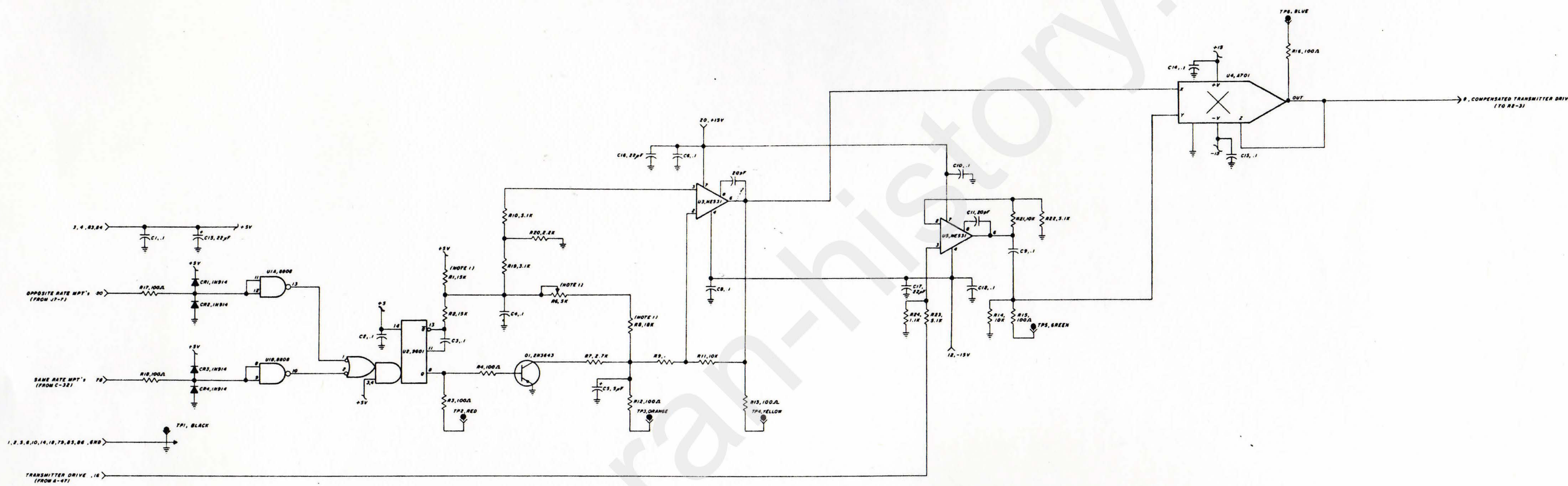

NOTES
1 UNLESS OTHERWISE STATED ALL RESISTANCE VALUES ARE IN OHMS, K=10³Ω, M=10⁶Ω
2 ALL CAPACITOR VALUES ARE IN μF UNLESS OTHERWISE STATED
3 LAST CIRCUIT SYMBOLS USED C61, CR10, Q2, R57, U19, NOT USED CR3
4 INPUTS ARE DESIGNATED BY >—, OUTPUTS BY —> H=ACTIVE HIGH, L=ACTIVE LOW
C-MDA-1 MULTIPLYING DIGITAL TO ANALOG CONVERTOR
C-SIA-1 SWITCHED INVERTING AMPLIFIER
C-GCA-1 GAIN CONTROL AMPLIFIER
C-AMP-1 AMPLIFIER
C-GPA-1 GATING POWER AMPLIFIER
C-LSD-1 LOST SIGNAL DETECTOR
(REVISED 3-14-75)
COAST GUARD
ELECTRONICS ENGINEERING CENTER
WILDWOOD NEW JERSEY
W0678-1/PYSN: PULSE SYNTHESIZER
(Schematic Diagram)
COMMANDING OFFICER
JAN 22, 74
W0678-D-507



NOTES: 1. UNLESS OTHERWISE STATED ALL RESISTANCE VALUES ARE IN OHMS, $K = 10^3\Omega$, $M = 10^6\Omega$.
2. ALL CAPACITOR VALUES ARE IN µf UNLESS OTHERWISE STATED.
3. LAST CIRCUIT SYMBOLS USED: C13, CR13, R24, U18.
4. INPUTS ARE DESIGNATED BY >—, OUTPUTS ARE DESIGNATED BY —>. H = ACTIVE HIGH, L = ACTIVE LOW.

(REVISED: 3-14-75) (REVISED 7-11-75)

COAST GUARD	ELECTRONICS ENGINEERING CENTER WILDWOOD NEW JERSEY	
Project No	Title: W0678-2/PCON: PULSE CONTROL (Schematic Diag.)	
Drawn By: W T F	Checked By:	
Project Eng	Scale	
Approved By: R A Bullen CDR, COMMANDING OFFICER USCG	Date: JAN 17, 74	Drawing No: W0678-D-508 — Sheet 1 of 1



NOTES:

1. AS ORIGINALLY DESIGNED
   R1 WAS A 20KΩ POT, R5 WAS 20KΩ POT
   R6 WAS 20KΩ POT, AND R8 WAS 2.1KΩ FIXED
   VALUES AS SHOWN REPRESENT AS INSTALLED
   W0678-19/GR DROOP BOARDS AT LORSTA NANTUCKET AN/FPN-42
2. ALL CAPACITOR VALUES ARE µF UNLESS STATED OTHERWISE
3. UNLESS OTHERWISE STATED ALL RESISTANCE VALUES ARE IN OHMS, $K = 10^3 \Omega$, $M = 10^6 \Omega$.
4. LAST CIRCUIT SYMBOLS USED; C17, CR4, Q1, R24, U5.
   SYMBOL NOT USED; R5.
5. INPUTS ARE DESIGNATED BY ≻— ; OUTPUTS BY →

(REVISED 3-20-75)

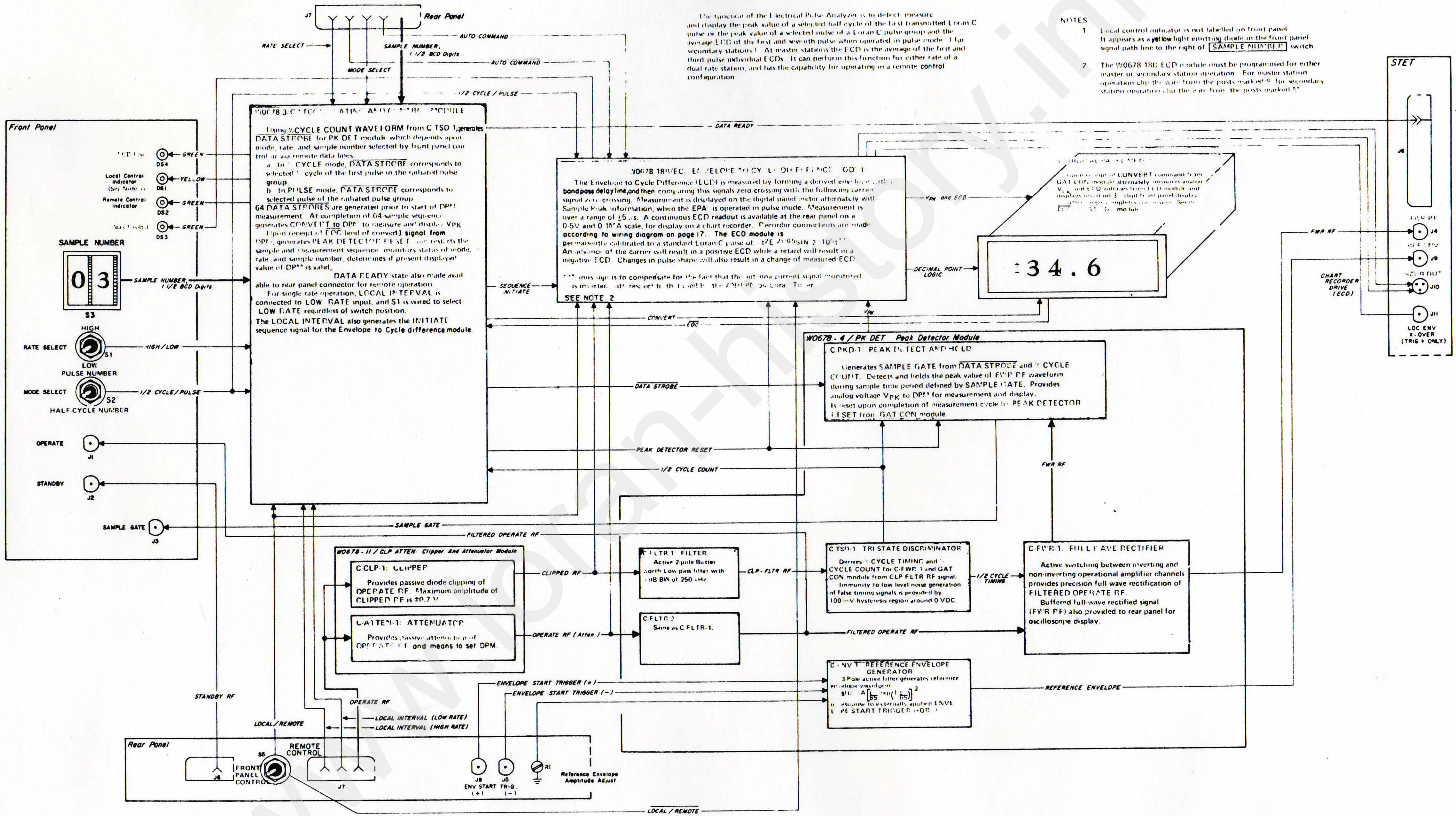
COAST GUARD		ELECTRONICS ENGINEERING CENTER WILDWOOD NEW JERSEY		
Project No W0638		Title FIGURE 2 W0678-19/GR DROOP		
Drawn By W. T. F.	Checked By			
Project Eng	Scale			
Approved By USCG COMMANDING OFFICER		Date 10-31-74	Drawing No	Sheet 1 of 1

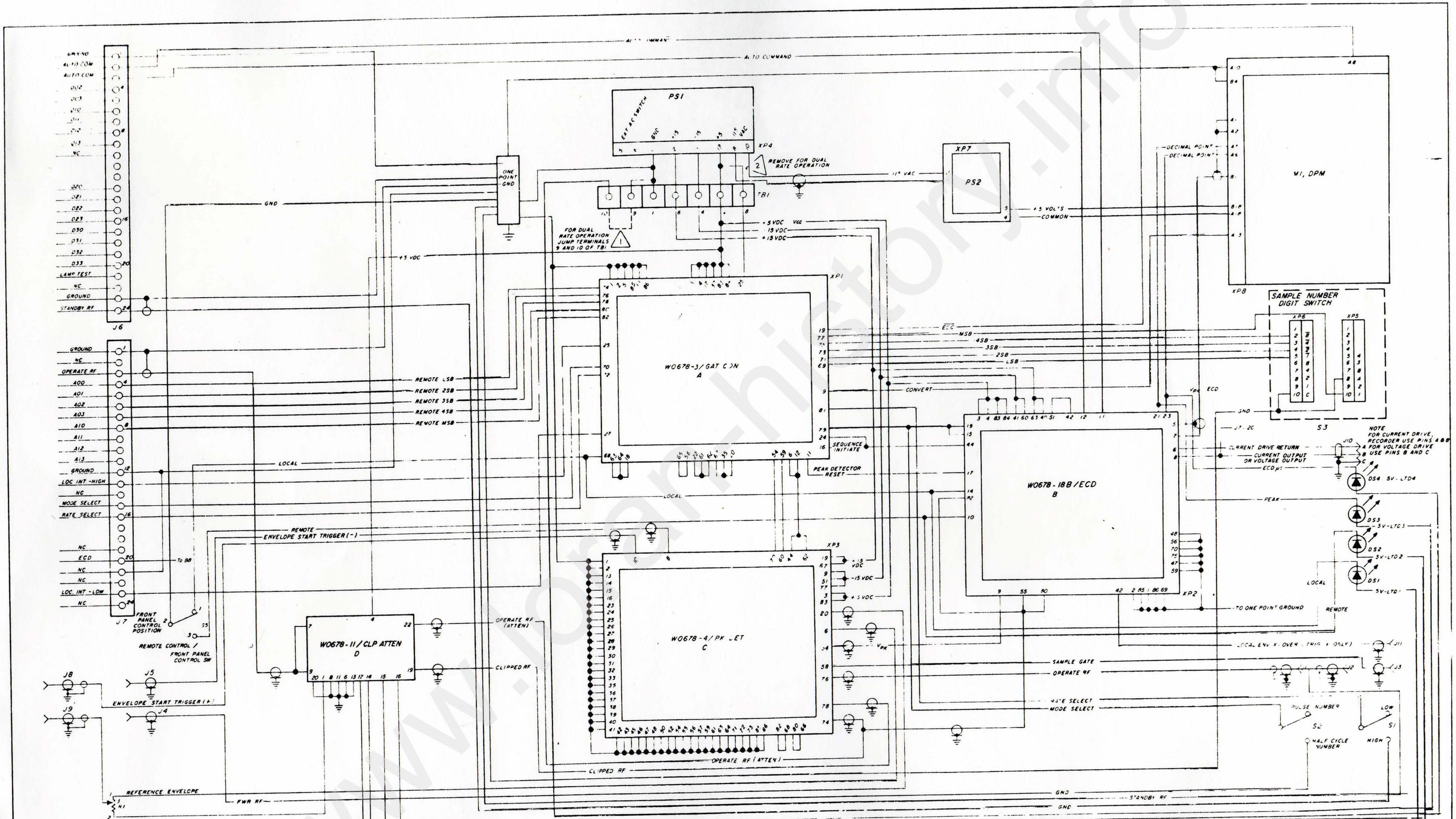
The function of the Electrical Pulse Analyzer is to detect, measure and display the peak value of a selected half cycle of the first transmitted Loran C pulse or the peak value of a selected pulse of a Loran C pulse group and the average ECD of the first and seventh pulse when operated in pulse mode. (for secondary stations.) At master stations the ECD is the average of the first and third pulse individual ECDs. It can perform this function for either rate of a dual rate station, and has the capability for operating in a remote control configuration.

NOTES

1. Local control indicator is not labelled on front panel. It appears as a **yellow** light emitting diode in the front panel signal path line to the right of SAMPLE NUMBER switch.

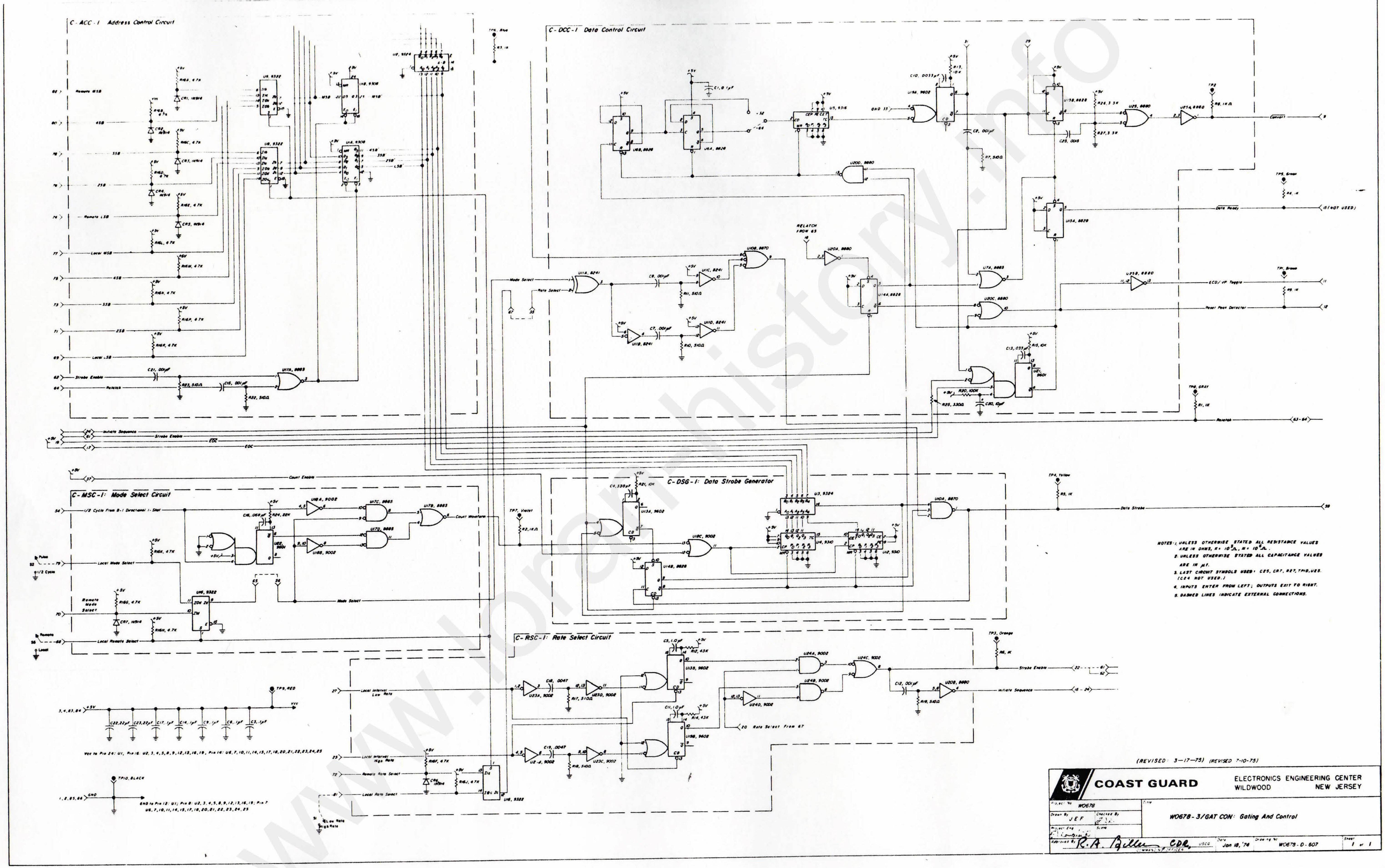
2. The W0678 18B ECD module must be programmed for either master or secondary station operation. For master station operation clip the wire from the posts marked S. For secondary station operation clip the wire from the posts marked M.

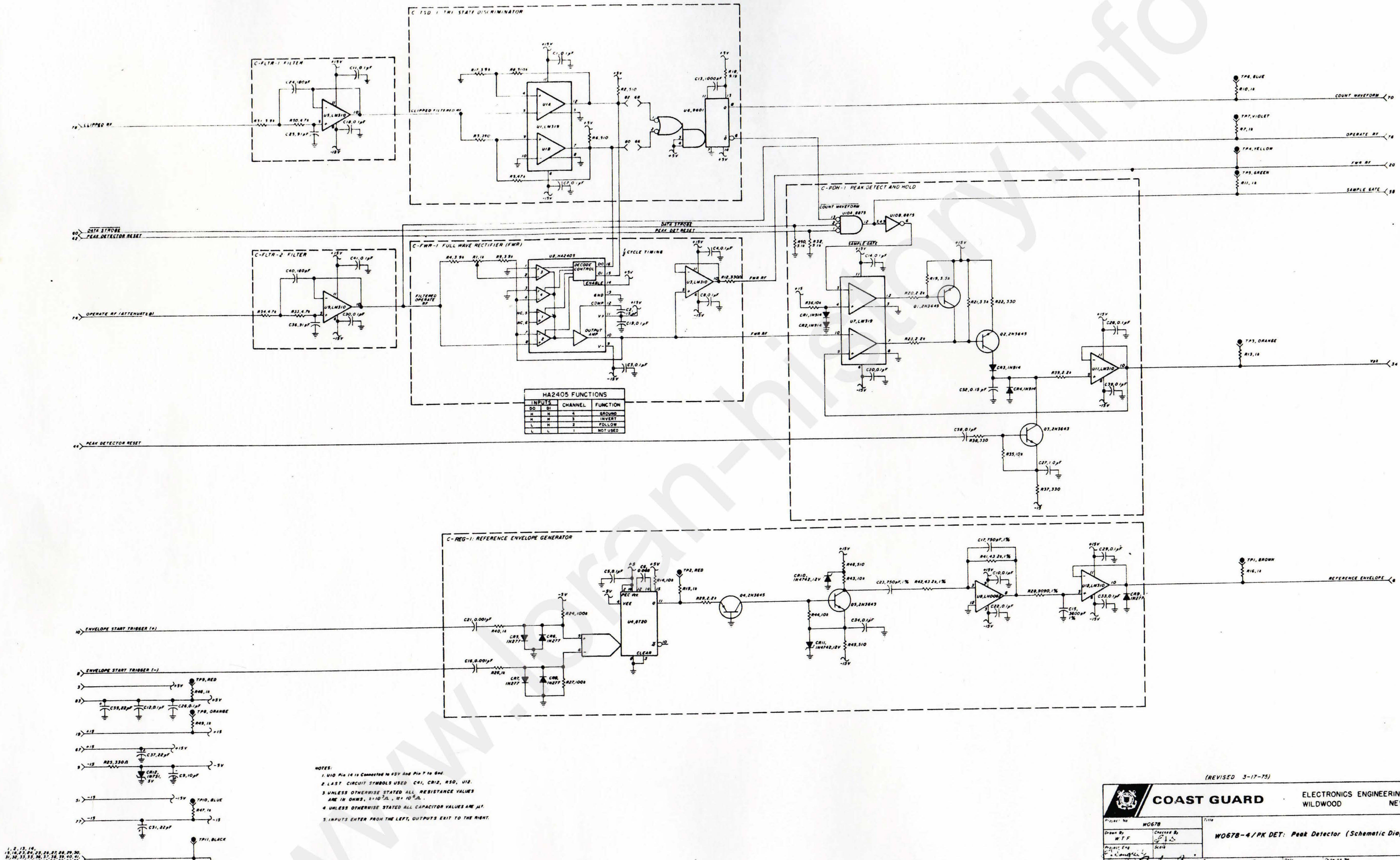




ELECTRICAL PULSE ANALYZER WIRING DIAGRAM

(REVISED 7-11-75)


C-ACC-1 Address Control Circuit
C-DCC-1 Data Control Circuit
C-MSC-1: Mode Select Circuit
C-DSG-1: Data Strobe Generator
C-RSC-1: Rate Select Circuit
Initiate Sequence
Strobe Enable
EOC
Count Enable
Data Strobe
Data Ready
Reset Peak Detector
Mode Select
Rate Select
Local Mode Select
Local Remote Select
Local Interval Low Rate
Local Interval High Rate
Remote Rate Select
Local Rate Select
Rate Select From 67
NOTES: 1. UNLESS OTHERWISE STATED ALL RESISTANCE VALUES ARE IN OHMS, K = $10^3 \Omega$, M = $10^6 \Omega$.
2. UNLESS OTHERWISE STATED ALL CAPACITANCE VALUES ARE IN µf.
3. LAST CIRCUIT SYMBOLS USED: C25, CR7, R27, TP10, U25. (C24 NOT USED.)
4. INPUTS ENTER FROM LEFT; OUTPUTS EXIT TO RIGHT.
5. DASHED LINES INDICATE EXTERNAL CONNECTIONS.
(REVISED: 3-17-75) (REVISED 7-10-75)
COAST GUARD
ELECTRONICS ENGINEERING CENTER
WILDWOOD NEW JERSEY
Project No W0678
Drawn By JEF
Checked By
Project Eng
Scale
Title
W0678-3/GAT CON: Gating And Control
Approved By R.A. Biller, CDR, USCG
COMMANDING OFFICER
Date Jan 18, '74
Drawing No W0678-D-607
Sheet 1 of 1



HA2405 FUNCTIONS			
INPUTS		CHANNEL	FUNCTION
DO	DI		
H	H	4	GROUND
H	H	3	INVERT
L	H	2	FOLLOW
L	L	1	NOT USED

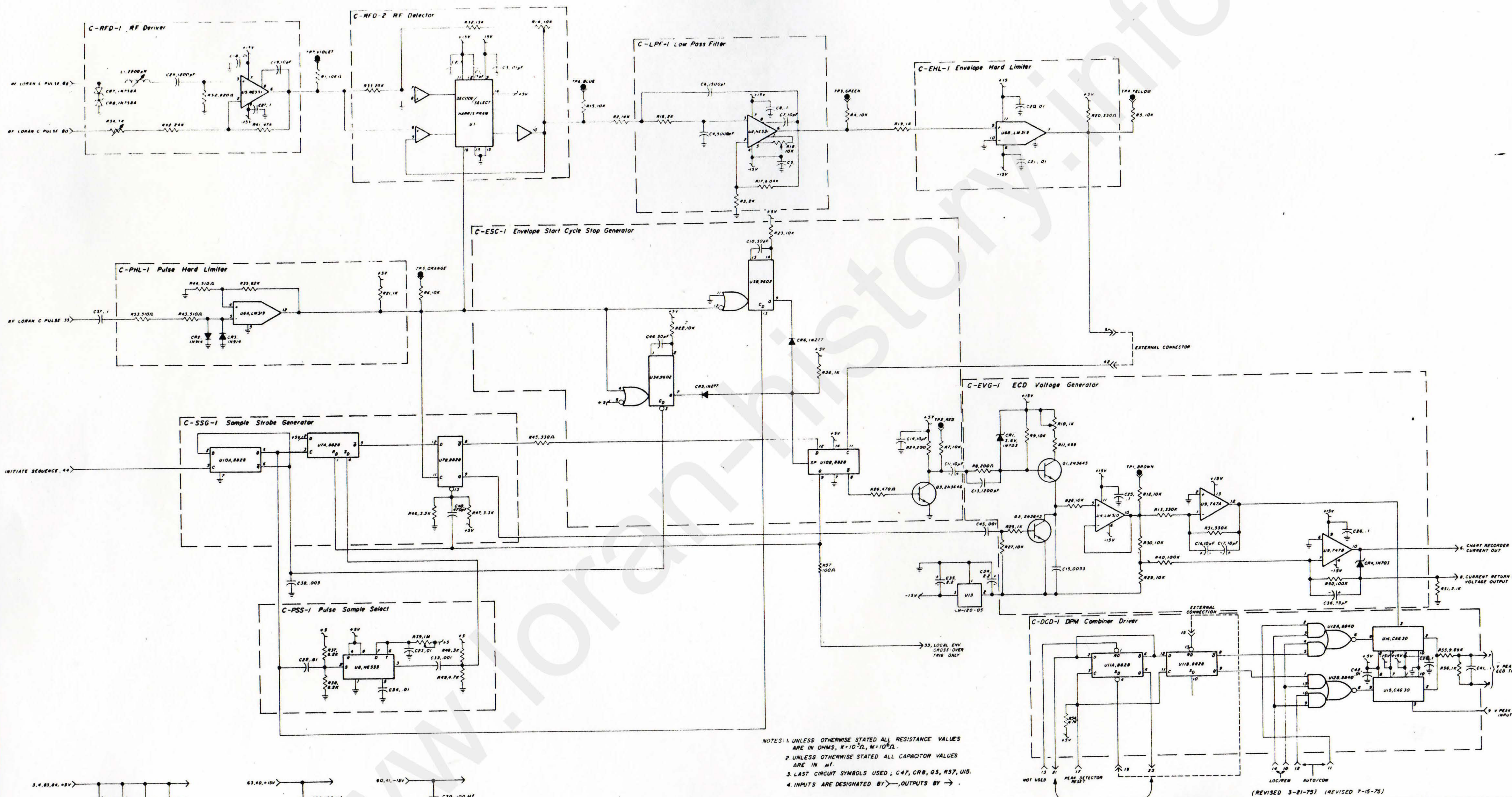
NOTES:

1. U10 Pin 14 is Connected to +5V And Pin 7 to Gnd.
2. LAST CIRCUIT SYMBOLS USED C41, CR12, R50, U12.
3. UNLESS OTHERWISE STATED ALL RESISTANCE VALUES ARE IN OHMS, $k = 10^3 \Omega$, $M = 10^6 \Omega$.
4. UNLESS OTHERWISE STATED ALL CAPACITOR VALUES ARE µF.
5. INPUTS ENTER FROM THE LEFT, OUTPUTS EXIT TO THE RIGHT.

(REVISED 3-17-75)

COAST GUARD — ELECTRONICS ENGINEERING CENTER, WILDWOOD, NEW JERSEY

Project No	W0678
Drawn By	W T F
Checked By	FJS
Project Eng	F. Dougherty
Scale	
Title	W0678-4/PK DET: Peak Detector (Schematic Diag.)
Approved By	R.A. Biller, CDR., USCG, COMMANDING OFFICER
Date	NOV. 25, 73
Drawing No	W0678-D-608
Sheet	1 of 1



NOTES: 1. UNLESS OTHERWISE STATED ALL RESISTANCE VALUES ARE IN OHMS, $K = 10^3 \Omega$, $M = 10^6 \Omega$.
2. UNLESS OTHERWISE STATED ALL CAPACITOR VALUES ARE IN µf.
3. LAST CIRCUIT SYMBOLS USED ; C47, CR8, Q3, R57, U15.
4. INPUTS ARE DESIGNATED BY ≻—, OUTPUTS BY →.

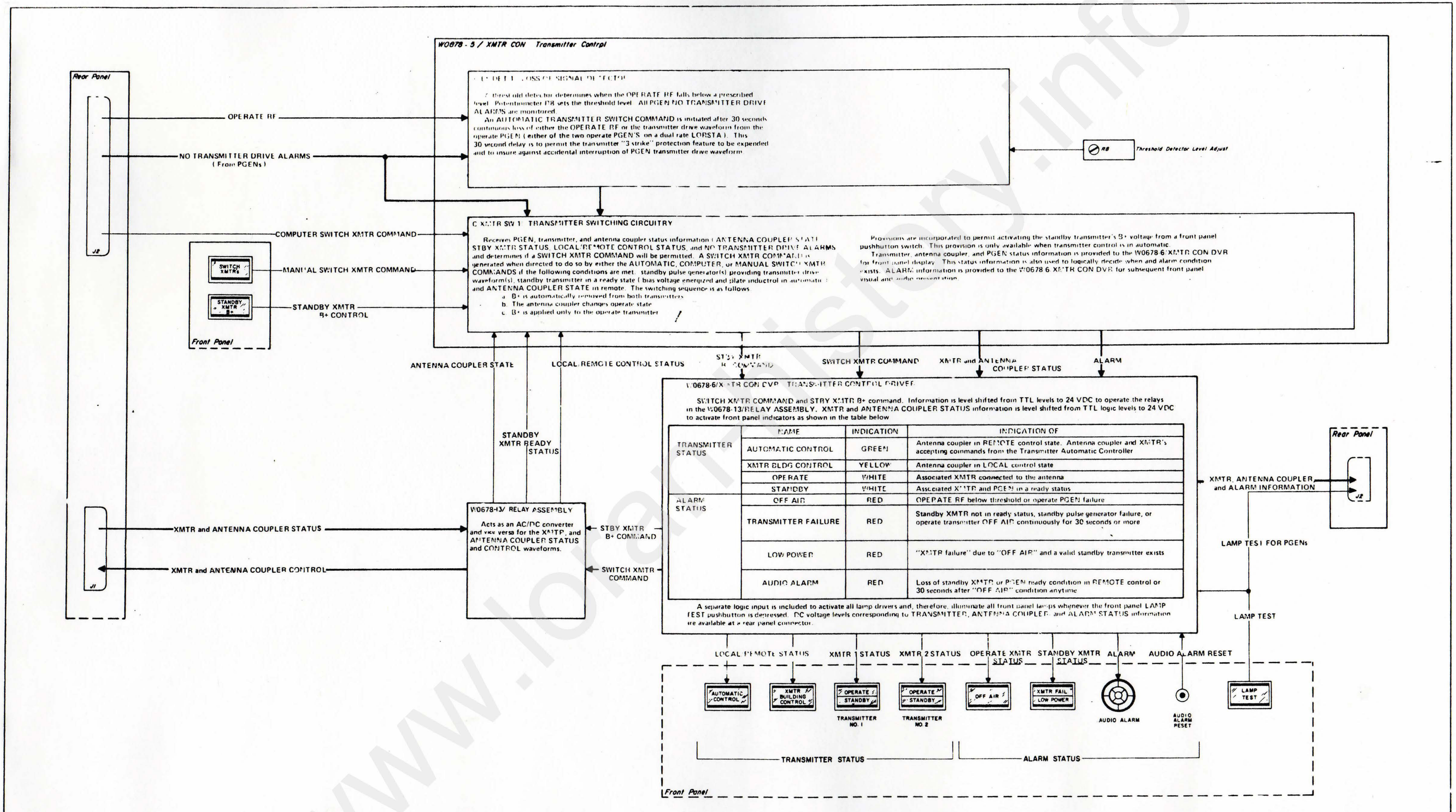
(REVISED 3-21-75) (REVISED 7-15-75)

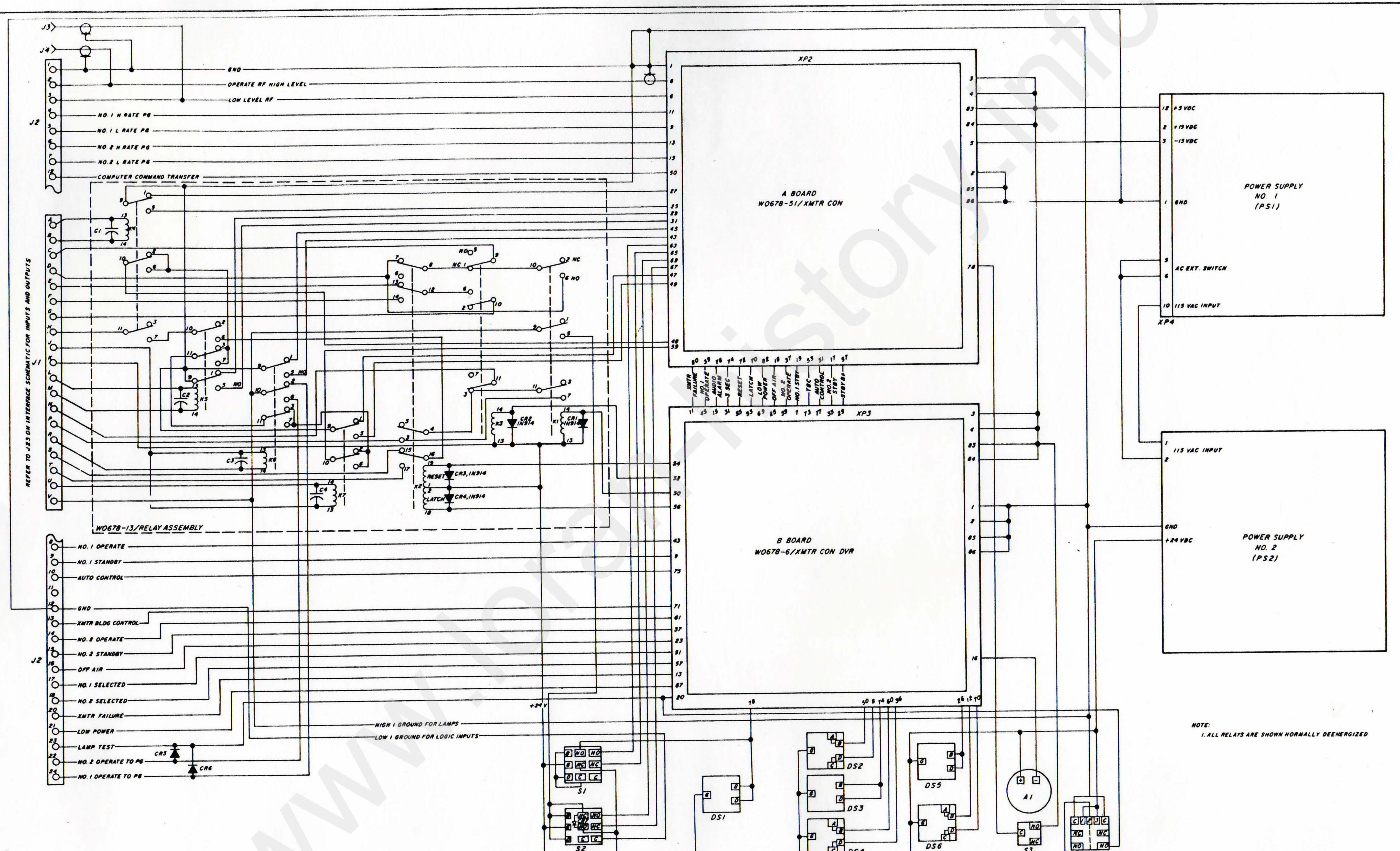
COAST GUARD

ELECTRONICS ENGINEERING CENTER
WILDWOOD NEW JERSEY

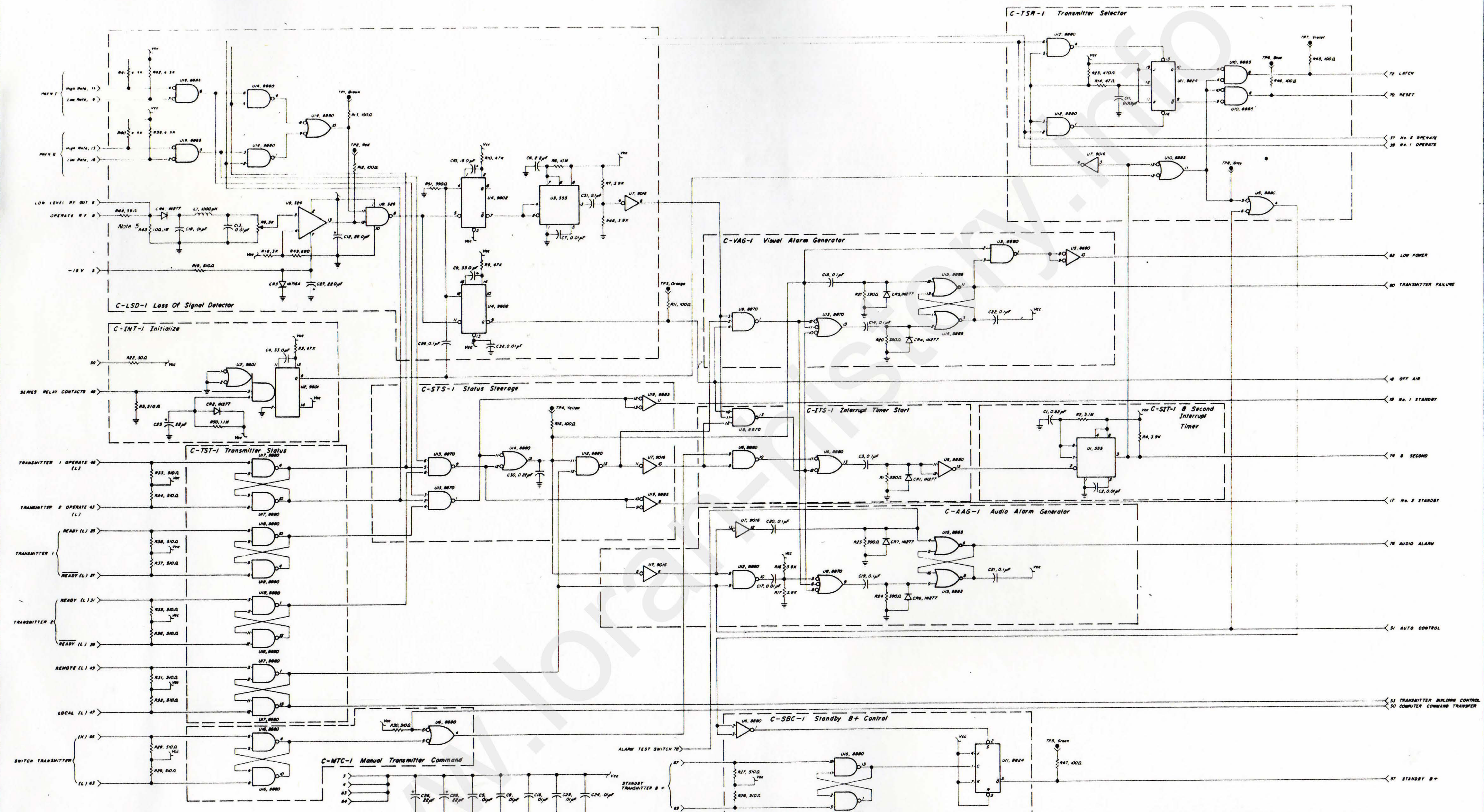
Project No		Title
Drawn By: W T F	Checked By	W0678-18B/ECD: ENVELOPE CYCLE DIFFERENCE (SCHEMATIC DIAGRAM)
Project Eng	Scale	

Approved By: USCG COMMANDING OFFICER	Date: 6-4-74	Drawing No: W0678-D-609	Sheet: 1 of 1


Rear Panel
J2
J1
OPERATE RF
NO TRANSMITTER DRIVE ALARMS
(From PGENs)
COMPUTER SWITCH XMTR COMMAND
MANUAL SWITCH XMTR COMMAND
STANDBY XMTR B+ CONTROL
SWITCH XMTRs
STANDBY XMTR B+
Front Panel
W0678-5 / XMTR CON Transmitter Control
LOSS OF SIGNAL DETECTOR
A threshold detector determines when the OPERATE RF falls below a prescribed level. Potentiometer R8 sets the threshold level. All PGEN NO TRANSMITTER DRIVE ALARMS are monitored.
An AUTOMATIC TRANSMITTER SWITCH COMMAND is initiated after 30 seconds continuous loss of either the OPERATE RF or the transmitter drive waveform from the operate PGEN (either of the two operate PGEN'S on a dual rate LORSTA). This 30 second delay is to permit the transmitter "3 strike" protection feature to be expended and to insure against accidental interruption of PGEN transmitter drive waveform.
R8
Threshold Detector Level Adjust
C XMTR SW 1 TRANSMITTER SWITCHING CIRCUITRY
Receives PGEN, transmitter, and antenna coupler status information (ANTENNA COUPLER STATE, STBY XMTR STATUS, LOCAL/REMOTE CONTROL STATUS, and NO TRANSMITTER DRIVE ALARMS and determines if a SWITCH XMTR COMMAND will be permitted. A SWITCH XMTR COMMAND is generated when directed to do so by either the AUTOMATIC, COMPUTER, or MANUAL SWITCH XMTR COMMANDS if the following conditions are met: standby pulse generator(s) providing transmitter drive waveform(s), standby transmitter in a ready state (bias voltage energized and plate inductrol in automatic) and ANTENNA COUPLER STATE in remote. The switching sequence is as follows:
a. B+ is automatically removed from both transmitters
b. The antenna coupler changes operate state
c. B+ is applied only to the operate transmitter
Provisions are incorporated to permit activating the standby transmitter's B+ voltage from a front panel pushbutton switch. This provision is only available when transmitter control is in automatic.
Transmitter, antenna coupler, and PGEN status information is provided to the W0678-6/XMTR CON DVR for front panel display. This status information is also used to logically decide when and alarm condition exists. ALARM information is provided to the W0678-6 XMTR CON DVR for subsequent front panel visual and audio presentation.
ANTENNA COUPLER STATE
LOCAL/REMOTE CONTROL STATUS
STBY XMTR B+ COMMAND
SWITCH XMTR COMMAND
XMTR and ANTENNA COUPLER STATUS
ALARM
STANDBY XMTR READY STATUS
W0678-13/ RELAY ASSEMBLY
Acts as an AC/DC converter and vice versa for the XMTR, and ANTENNA COUPLER STATUS and CONTROL waveforms.
XMTR and ANTENNA COUPLER STATUS
XMTR and ANTENNA COUPLER CONTROL
STBY XMTR B+ COMMAND
SWITCH XMTR COMMAND
W0678-6/XMTR CON DVR TRANSMITTER CONTROL DRIVER
SWITCH XMTR COMMAND and STBY XMTR B+ command. Information is level shifted from TTL levels to 24 VDC to operate the relays in the W0678-13/RELAY ASSEMBLY. XMTR and ANTENNA COUPLER STATUS information is level shifted from TTL logic levels to 24 VDC to activate front panel indicators as shown in the table below
	NAME	INDICATION	INDICATION OF
TRANSMITTER STATUS	AUTOMATIC CONTROL	GREEN	Antenna coupler in REMOTE control state. Antenna coupler and XMTR's accepting commands from the Transmitter Automatic Controller
	XMTR BLDG CONTROL	YELLOW	Antenna coupler in LOCAL control state
	OPERATE	WHITE	Associated XMTR connected to the antenna
	STANDBY	WHITE	Associated XMTR and PGEN in a ready status
ALARM STATUS	OFF AIR	RED	OPERATE RF below threshold or operate PGEN failure
	TRANSMITTER FAILURE	RED	Standby XMTR not in ready status, standby pulse generator failure, or operate transmitter OFF AIR continuously for 30 seconds or more
	LOW POWER	RED	"XMTR failure" due to "OFF AIR" and a valid standby transmitter exists
	AUDIO ALARM	RED	Loss of standby XMTR or PGEN ready condition in REMOTE control or 30 seconds after "OFF AIR" condition anytime
A separate logic input is included to activate all lamp drivers and, therefore, illuminate all front panel lamps whenever the front panel LAMP TEST pushbutton is depressed. DC voltage levels corresponding to TRANSMITTER, ANTENNA COUPLER, and ALARM STATUS information are available at a rear panel connector.
Rear Panel
J2
XMTR, ANTENNA COUPLER and ALARM INFORMATION
LAMP TEST FOR PGENs
LAMP TEST
LOCAL/REMOTE STATUS
XMTR 1 STATUS
XMTR 2 STATUS
OPERATE XMTR STATUS
STANDBY XMTR STATUS
ALARM
AUDIO ALARM RESET
AUTOMATIC CONTROL
XMTR BUILDING CONTROL
OPERATE STANDBY
TRANSMITTER NO. 1
OPERATE STANDBY
TRANSMITTER NO. 2
OFF AIR
XMTR FAIL LOW POWER
AUDIO ALARM
AUDIO ALARM RESET
LAMP TEST
TRANSMITTER STATUS
ALARM STATUS
Front Panel



TRANSMITTER AUTO CONTROLLER WIRING DIAGRAM



NOTES UNLESS OTHERWISE DESIGNATED, ALL RESISTANCE VALUES ARE IN OHMS, $K = 10^3\Omega$, $M = 10^6\Omega$.

2. UNLESS OTHERWISE DESIGNATED, ALL CAPACITOR VALUES ARE μf.

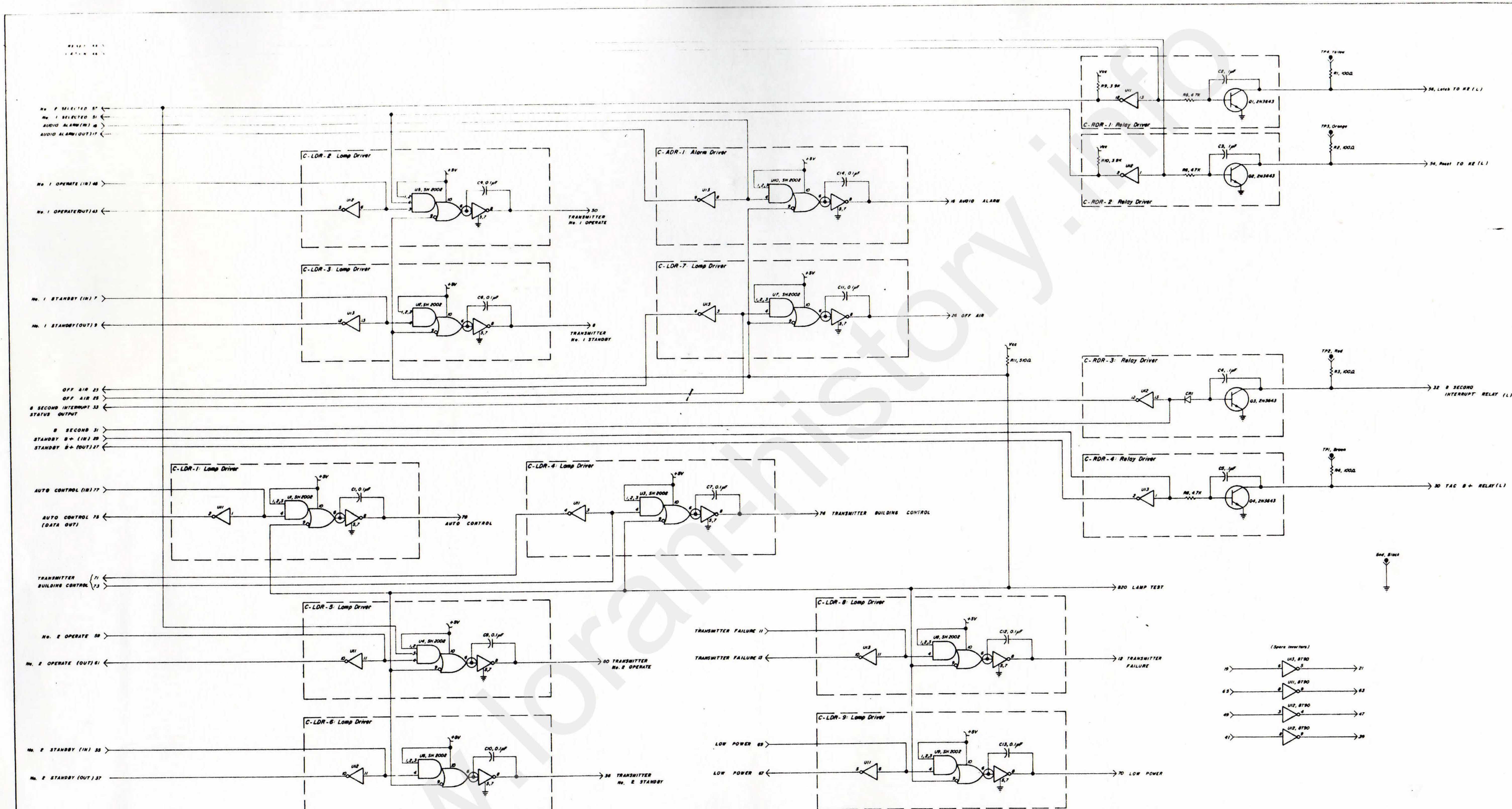
3. LAST CIRCUIT SYMBOLS USED C32, CR8, R50, U19

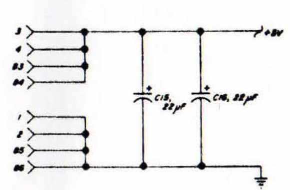
4. INPUTS ENTER FROM LEFT; OUTPUTS EXIT TO RIGHT.

5. R43 and R44 to be raised off of board.

(REVISED 3-19-75) (REVISED 7-10-75)

COAST GUARD		ELECTRONICS ENGINEERING CENTER WILDWOOD NEW JERSEY		
Project No W0678		Title W0678-5/XMTR CON: Automatic Controller (Schematic Diag.)		
Drawn By J.E.F.	Checked By			
Project Eng	Scale			
Approved By R. A. Bulley CDR USCG COMMANDING OFFICER		Date Dec. 10, '73	Drawing No W0678-D-407	Sheet 1 of 1





NOTES: 1. INPUTS ARE DESIGNATED BY ≻—; OUTPUTS BY →.
2. ALL OUTPUTS ON RIGHT GO TO FRONT PANEL.
3. ALL OUTPUTS ON LEFT GO TO INTERFACE.
4. UNLESS OTHERWISE DESIGNATED ALL RESISTANCE VALUES ARE IN OHMS, $K = 10^3 \Omega$, $M = 10^6 \Omega$.
5. ALL CAPACITORS ARE IN μfd.
6. LAST CIRCUIT SYMBOLS USED — C16, Q4, R11, U13.
7. (L) INDICATES ACTIVE LOW.

(REVISED 3-16-75) (REVISED 7-11-75)

COAST GUARD ELECTRONICS ENGINEERING CENTER WILDWOOD NEW JERSEY

Project No W0678		Title W0678-6/XMTR CON DVR: Transmitter Control Driver
Drawn By J.E.F.	Checked By [signature]	
Project Eng [signature]	Scale	
Approved By R. A. Biller CDR. USCG COMMANDING OFFICER	Date Feb 1, '74	Drawing No W0678-D-408 — Sheet 1 of 1

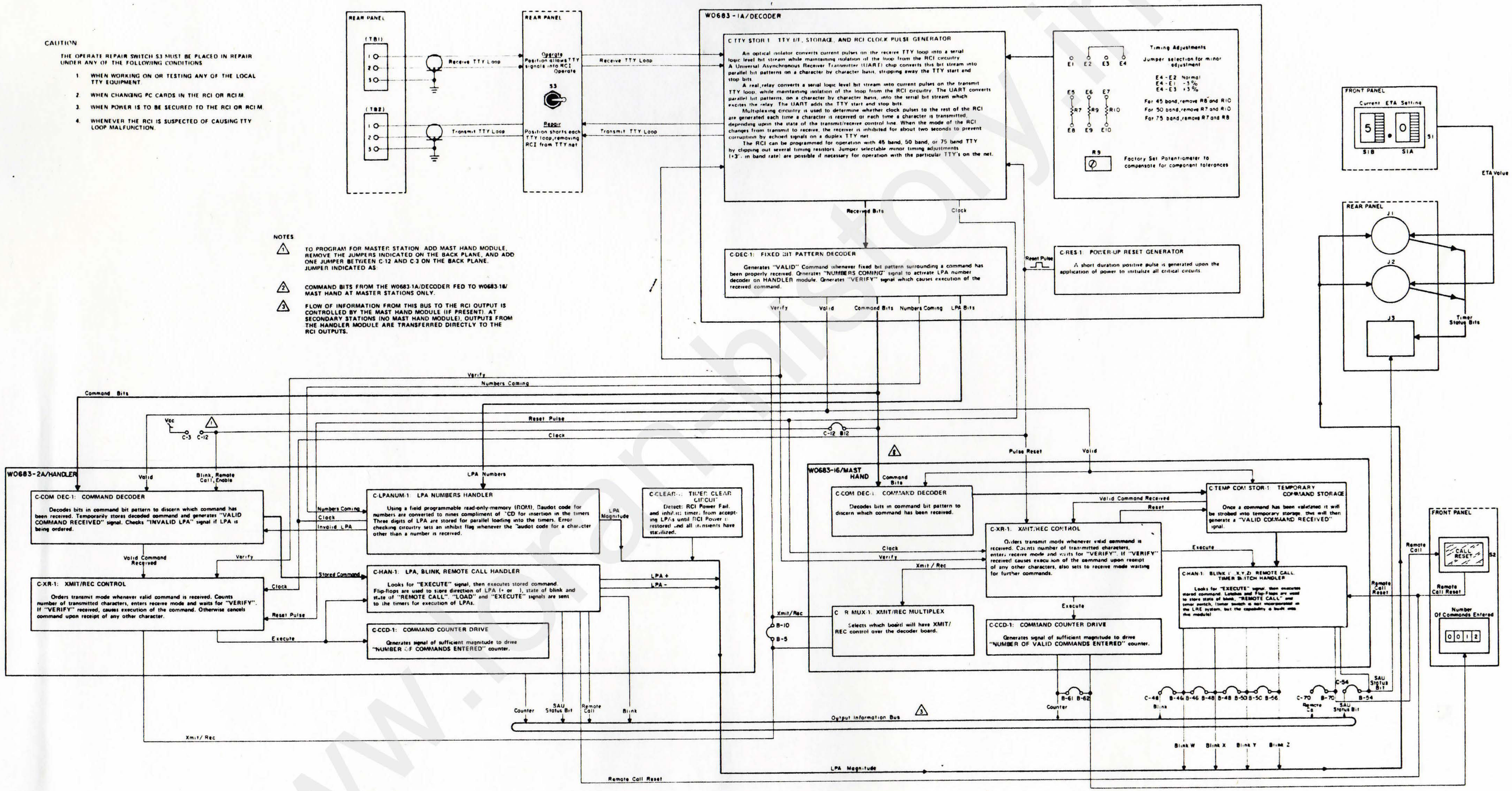
CAUTION

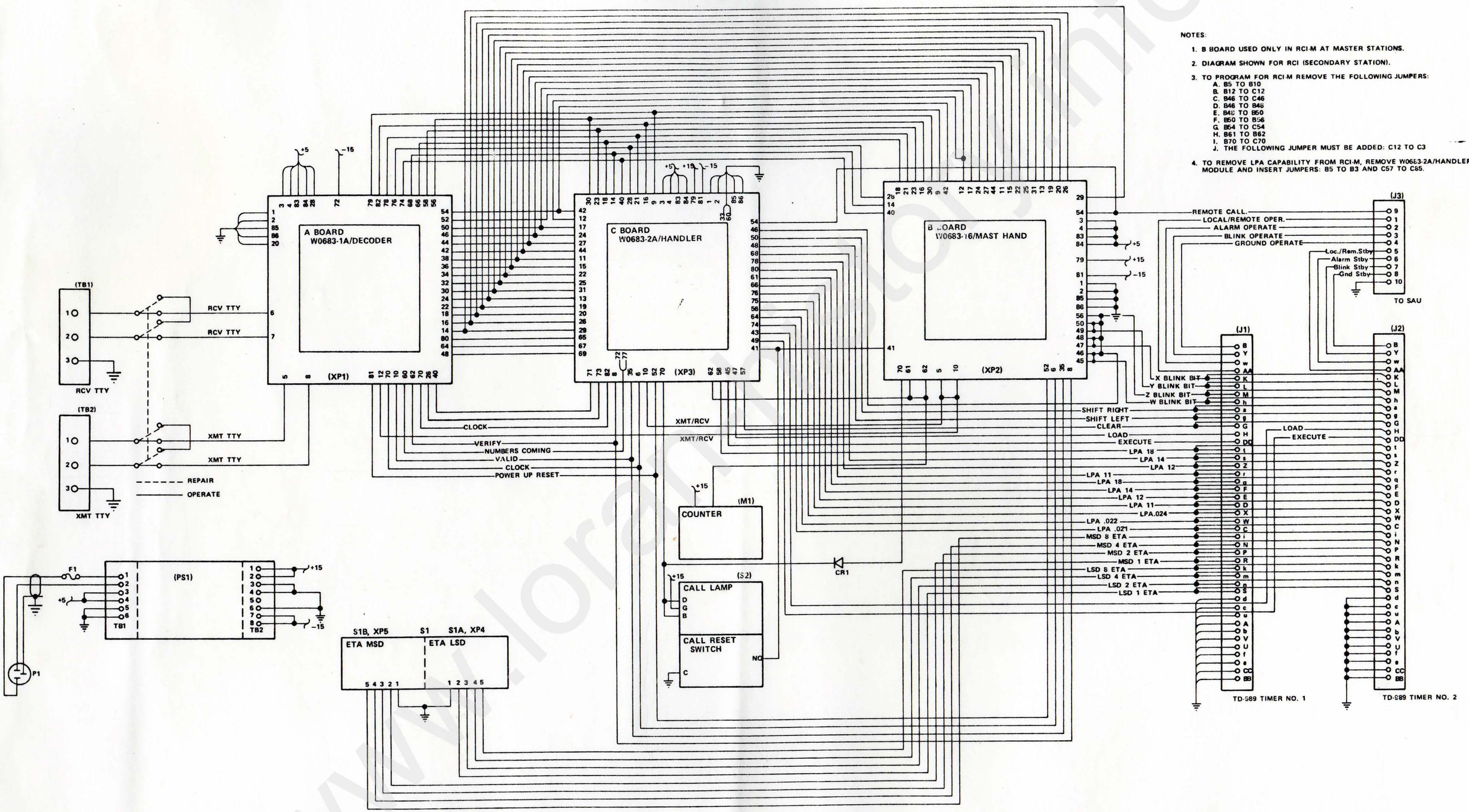
THE OPERATE REPAIR SWITCH S3 MUST BE PLACED IN REPAIR UNDER ANY OF THE FOLLOWING CONDITIONS

1. WHEN WORKING ON OR TESTING ANY OF THE LOCAL TTY EQUIPMENT
2. WHEN CHANGING PC CARDS IN THE RCI OR RCIM.
3. WHEN POWER IS TO BE SECURED TO THE RCI OR RCIM.
4. WHENEVER THE RCI IS SUSPECTED OF CAUSING TTY LOOP MALFUNCTION.

NOTES

1. TO PROGRAM FOR MASTER STATION ADD MAST HAND MODULE, REMOVE THE JUMPERS INDICATED ON THE BACK PLANE, AND ADD ONE JUMPER BETWEEN C-12 AND C-3 ON THE BACK PLANE. JUMPER INDICATED AS:
2. COMMAND BITS FROM THE W0683-1A/DECODER FED TO W0683-16/ MAST HAND AT MASTER STATIONS ONLY.
3. FLOW OF INFORMATION FROM THIS BUS TO THE RCI OUTPUT IS CONTROLLED BY THE MAST HAND MODULE (IF PRESENT). AT SECONDARY STATIONS (NO MAST HAND MODULE), OUTPUTS FROM THE HANDLER MODULE ARE TRANSFERRED DIRECTLY TO THE RCI OUTPUTS.

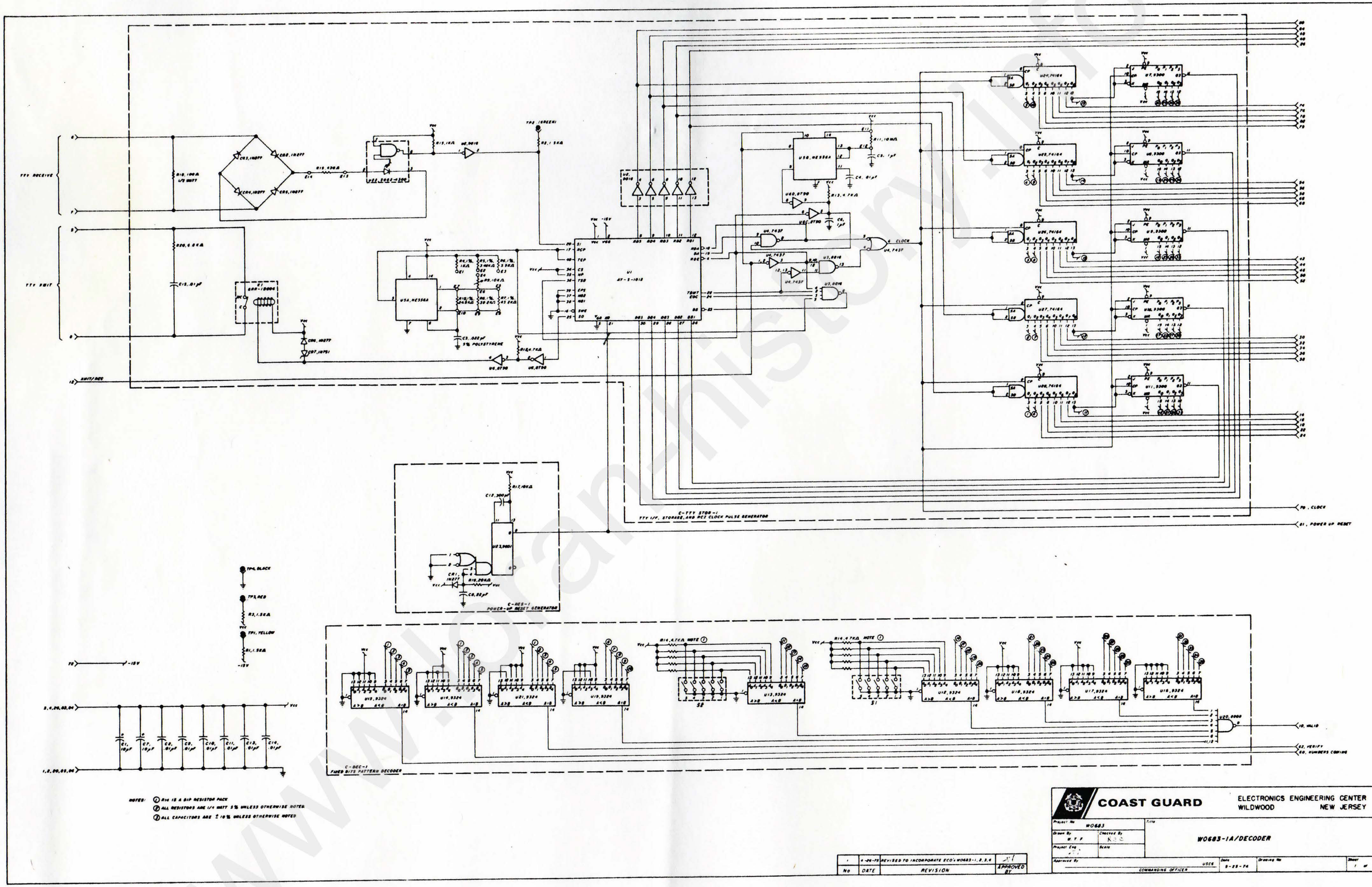


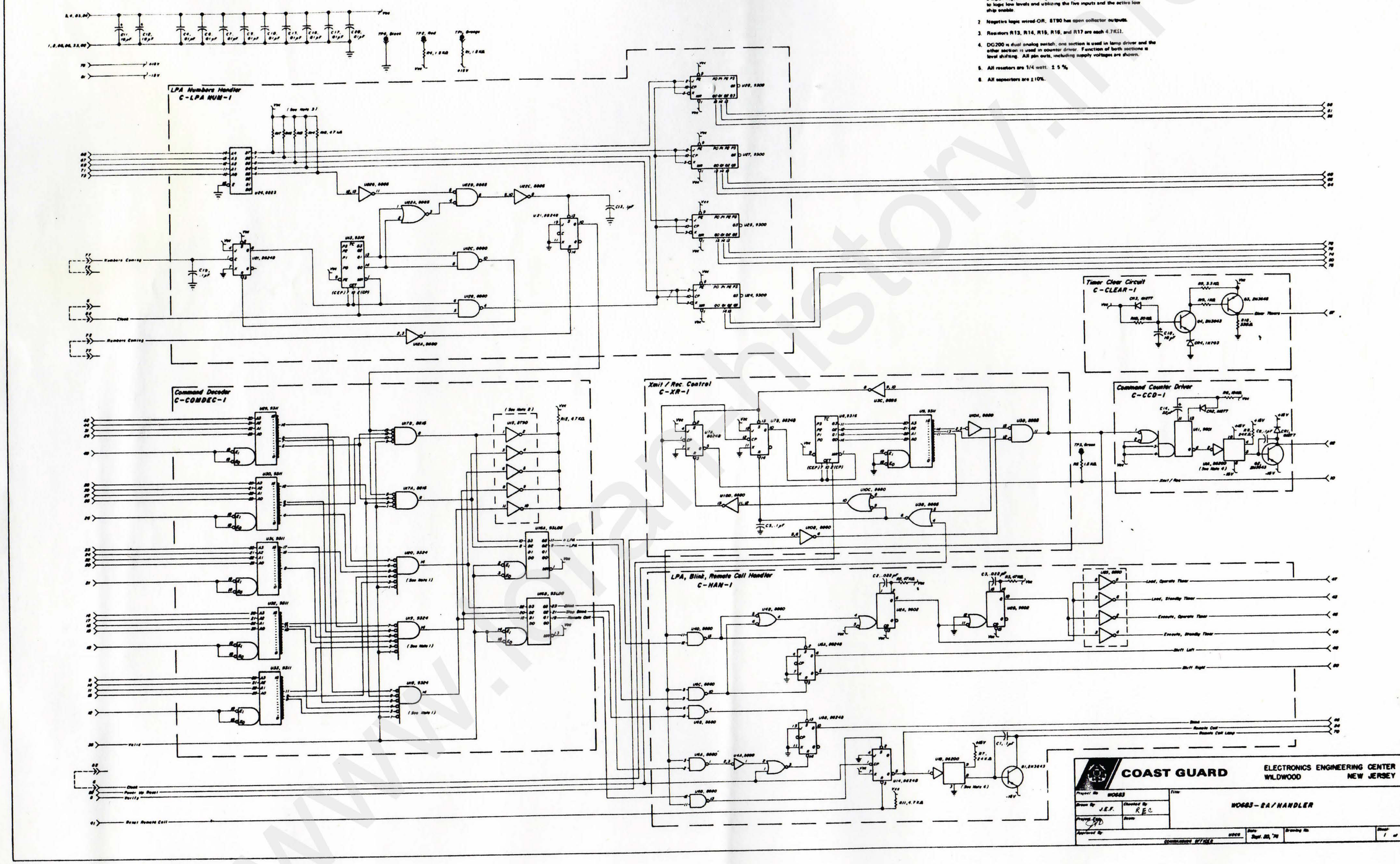


NOTES:

1. B BOARD USED ONLY IN RCI-M AT MASTER STATIONS.
2. DIAGRAM SHOWN FOR RCI (SECONDARY STATION).
3. TO PROGRAM FOR RCI-M REMOVE THE FOLLOWING JUMPERS:
   A. B5 TO B10
   B. B12 TO C12
   C. B46 TO C46
   D. B46 TO B48
   E. B48 TO B50
   F. B50 TO B56
   G. B54 TO C54
   H. B61 TO B62
   I. B70 TO C70
   J. THE FOLLOWING JUMPER MUST BE ADDED: C12 TO C3
4. TO REMOVE LPA CAPABILITY FROM RCI-M, REMOVE W0683-2A/HANDLER MODULE AND INSERT JUMPERS: B5 TO B3 AND C57 TO C85.

REMOTE CONTROL INTERFACE; WIRING DIAGRAM


TTY RECEIVE
TTY XMIT
C-TTY STOR-1
TTY I/F, STORAGE, AND PCI CLOCK PULSE GENERATOR
C-RES-1
POWER-UP RESET GENERATOR
C-DEC-1
FIXED BITS PATTERN DECODER
70, CLOCK
61, POWER UP RESET
10, VALID
62, VERIFY
60, NUMBERS COMING
NOTES: (1) R14 IS A DIP RESISTOR PACK
(2) ALL RESISTORS ARE 1/4 WATT 5% UNLESS OTHERWISE NOTED
(3) ALL CAPACITORS ARE ± 10% UNLESS OTHERWISE NOTED
1 | 4-26-75 | REVISED TO INCORPORATE ECO's W0683-1, 2, 3, 4
NO | DATE | REVISION | APPROVED BY
COAST GUARD
ELECTRONICS ENGINEERING CENTER
WILDWOOD NEW JERSEY
Project No W0683
Drawn By W. T. F
Checked By KSC
Project Eng
Scale
Title
W0683-1A/DECODER
Approved By USCG
COMMANDING OFFICER
Date 9-25-74
Drawing No
Sheet 1 of 1



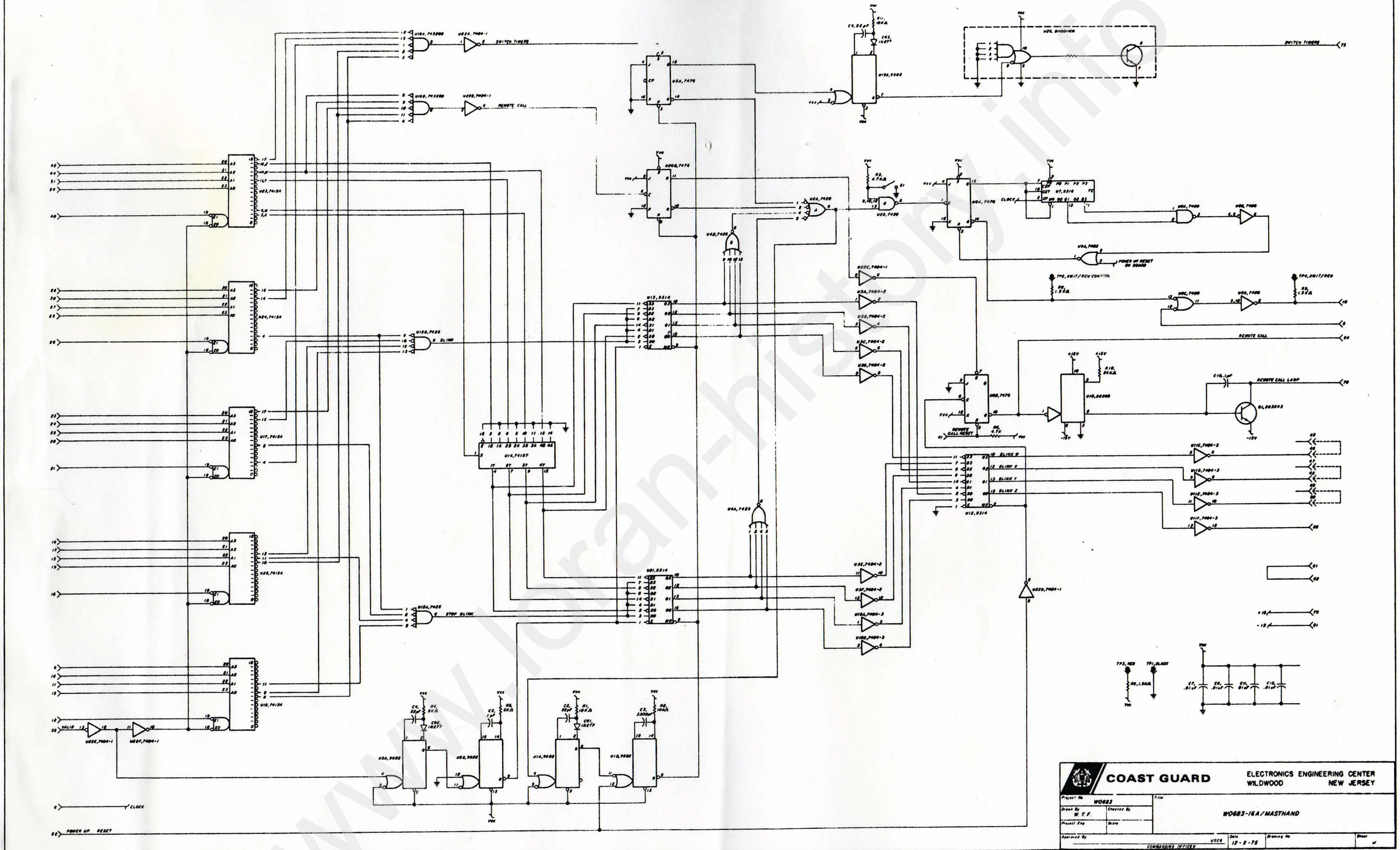
No	DATE	REVISION	APPROVED BY
1	4-20-75	REVISED TO INCORPORATE ECO's W0683-1, 2, 3, 4	

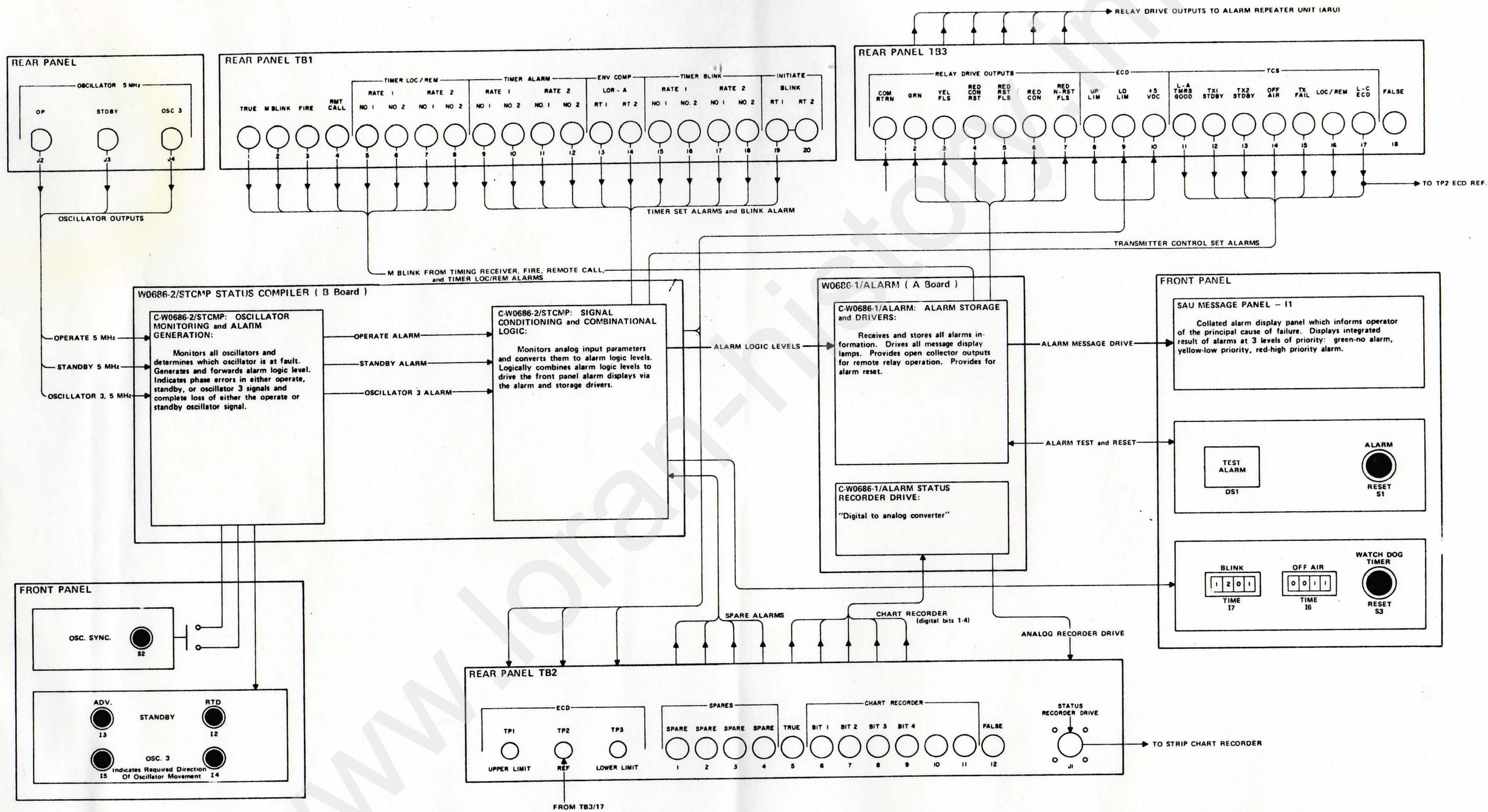
Notes:

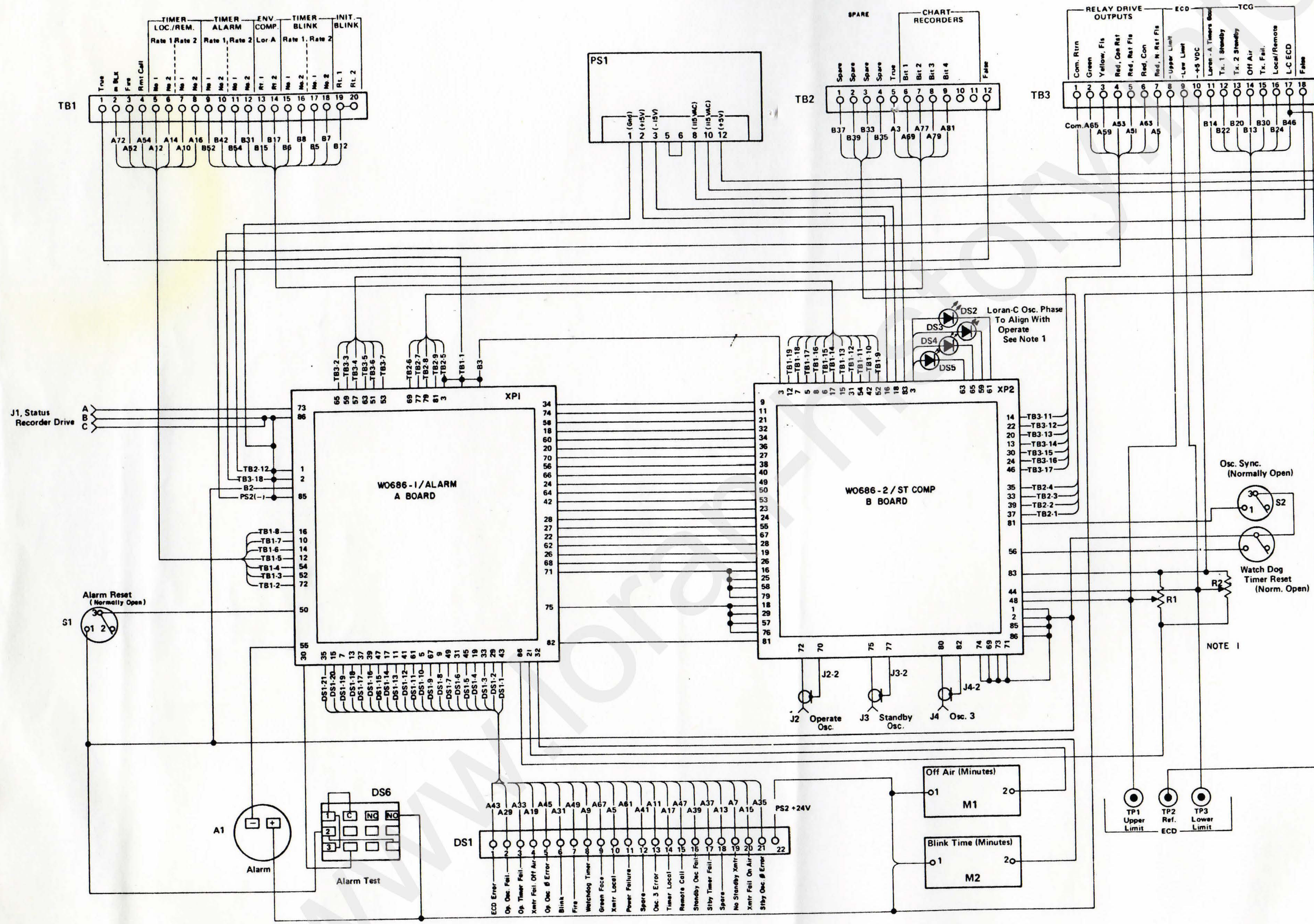
1. U18, U19, and U20 are actually 9324's, five bit comparators used as 6 input negative NAND gates by programming the five compare inputs to logic low levels and utilizing the five inputs and the active low chip enable.
2. Negative logic wired-OR; 8T90 has open collector outputs.
3. Resistors R13, R14, R15, R16, and R17 are each 4.7KΩ.
4. DG200 is dual analog switch, one section is used in lamp driver and the other section is used in counter driver. Function of both sections is level shifting. All pin outs, including supply voltages are shown.
5. All resistors are 1/4 watt. ± 5 %
6. All capacitors are ± 10%.

COAST GUARD ELECTRONICS ENGINEERING CENTER WILDWOOD NEW JERSEY

Project No W0683		Title: W0683 - 2A / HANDLER	
Drawn By J.E.F.	Checked By REC		
Project Eng.	Scale		
Approved By USCG COMMANDING OFFICER	Date Sept. 20, '74	Drawing No.	Sheet 1 of 1


SWITCH TIMERS
REMOTE CALL
BLINK
STOP BLINK
REMOTE CALL LAMP
POWER UP RESET
CLOCK
VALID
COAST GUARD
ELECTRONICS ENGINEERING CENTER
WILDWOOD NEW JERSEY
Project No W0683
Drawn By W. T. F.
Checked By
Project Eng
Scale
Title W0683-16A/MASTHAND
Approved By
USCG
COMMANDING OFFICER
Date 12-2-75
Drawing No
Sheet


RELAY DRIVE OUTPUTS TO ALARM REPEATER UNIT (ARU)
REAR PANEL
OSCILLATOR 5 MHz
OP
STDBY
OSC 3
J2
J3
J4
OSCILLATOR OUTPUTS
REAR PANEL TB1
TRUE
M BLINK
FIRE
RMT CALL
TIMER LOC / REM
TIMER ALARM
ENV COMP
TIMER BLINK
INITIATE
RATE 1
RATE 2
NO 1
NO 2
LOR - A
RT 1
RT 2
BLINK
TIMER SET ALARMS and BLINK ALARM
REAR PANEL TB3
RELAY DRIVE OUTPUTS
ECD
TCS
COM RTRN
GRN
YEL FLS
RED CON RST
RED RST FLS
RED CON
RED N-RST FLS
UP LIM
LO LIM
+5 VDC
L-A TMRS GOOD
TX1 STDBY
TX2 STDBY
OFF AIR
TX FAIL
LOC/REM
L-C ECD
FALSE
TO TP2 ECD REF.
TRANSMITTER CONTROL SET ALARMS
M BLINK FROM TIMING RECEIVER, FIRE, REMOTE CALL, and TIMER LOC/REM ALARMS
W0686-2/STCMP STATUS COMPILER (B Board)
C-W0686-2/STCMP: OSCILLATOR MONITORING and ALARM GENERATION:
Monitors all oscillators and determines which oscillator is at fault. Generates and forwards alarm logic level. Indicates phase errors in either operate, standby, or oscillator 3 signals and complete loss of either the operate or standby oscillator signal.
OPERATE 5 MHz
STANDBY 5 MHz
OSCILLATOR 3, 5 MHz
OPERATE ALARM
STANDBY ALARM
OSCILLATOR 3 ALARM
C-W0686-2/STCMP: SIGNAL CONDITIONING and COMBINATIONAL LOGIC:
Monitors analog input parameters and converts them to alarm logic levels. Logically combines alarm logic levels to drive the front panel alarm displays via the alarm and storage drivers.
ALARM LOGIC LEVELS
W0686-1/ALARM (A Board)
C-W0686-1/ALARM: ALARM STORAGE and DRIVERS:
Receives and stores all alarms information. Drives all message display lamps. Provides open collector outputs for remote relay operation. Provides for alarm reset.
C-W0686-1/ALARM STATUS RECORDER DRIVE:
"Digital to analog converter"
ALARM MESSAGE DRIVE
ALARM TEST and RESET
FRONT PANEL
SAU MESSAGE PANEL – I1
Collated alarm display panel which informs operator of the principal cause of failure. Displays integrated result of alarms at 3 levels of priority: green-no alarm, yellow-low priority, red-high priority alarm.
TEST ALARM
DS1
ALARM
RESET S1
BLINK
TIME I7
OFF AIR
TIME I6
WATCH DOG TIMER
RESET S3
FRONT PANEL
OSC. SYNC.
S2
ADV.
STANDBY
RTD
I3
I2
OSC. 3
Indicates Required Direction Of Oscillator Movement
I5
I4
SPARE ALARMS
CHART RECORDER (digital bits 1-4)
ANALOG RECORDER DRIVE
REAR PANEL TB2
ECD
TP1
TP2
TP3
UPPER LIMIT
REF
LOWER LIMIT
FROM TB3/17
SPARES
SPARE
TRUE
CHART RECORDER
BIT 1
BIT 2
BIT 3
BIT 4
FALSE
STATUS RECORDER DRIVE
J1
TO STRIP CHART RECORDER



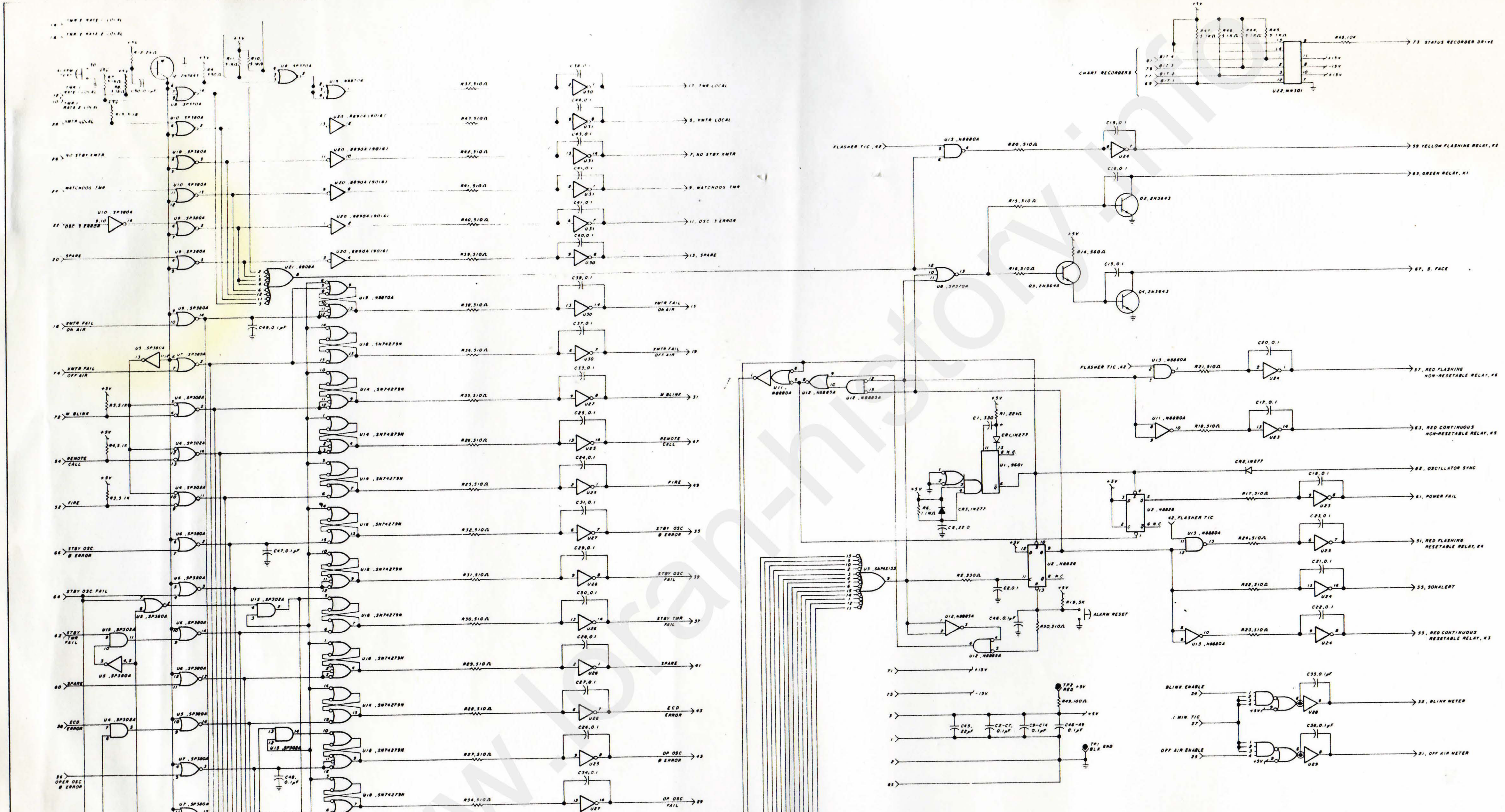
Note 1:

DS2 – Retarded: Standby
DS3 – Advanced: Standby
DS4 – Retarded: Osc. 3
DS5 – Advanced: Osc. 3

2. When the WO745 TIC panel (pg. 35) is installed at the station, instructions will be included to clip out the pots, R1 & R2.

(REVISED 7-16-75)

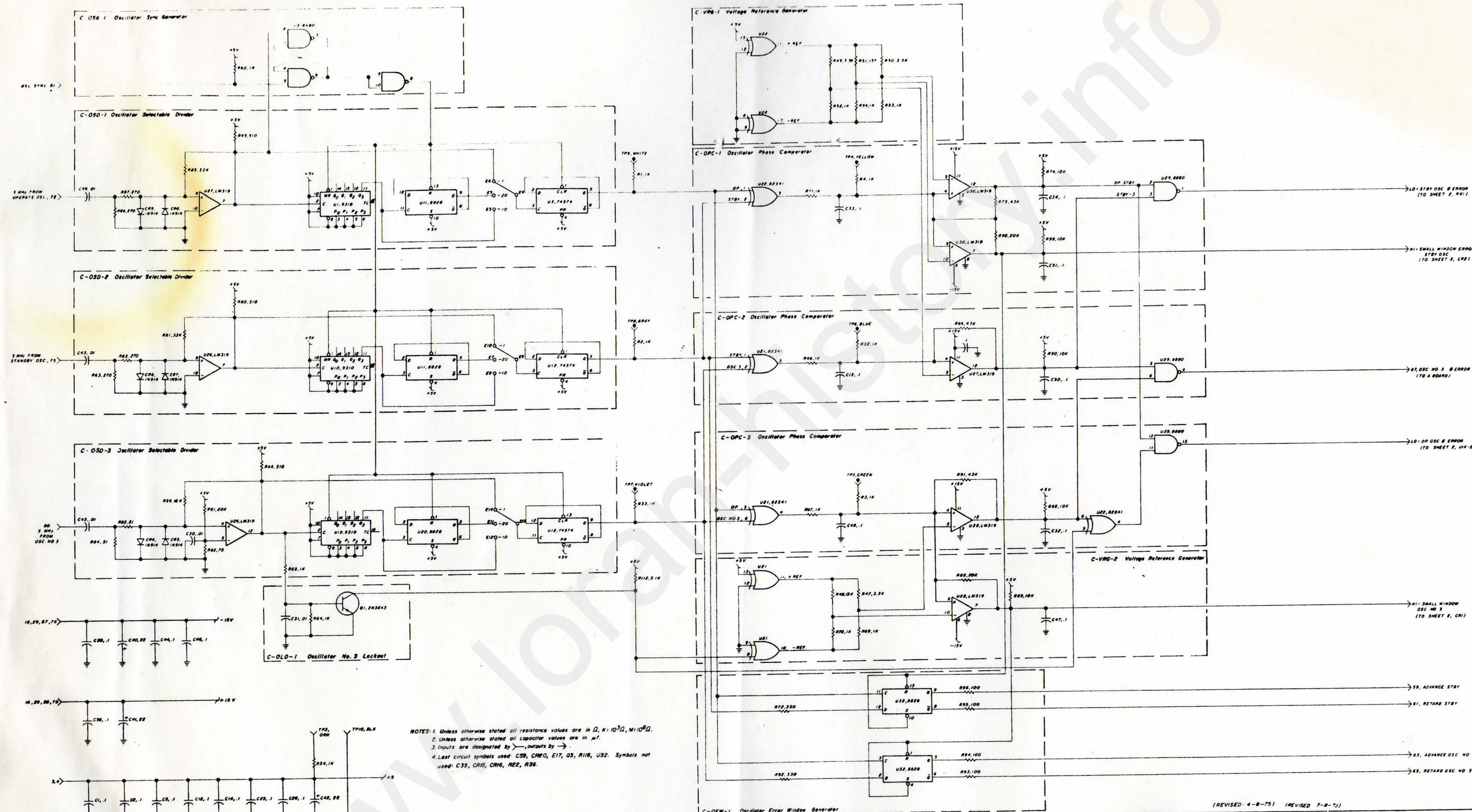
STATUS ALARM UNIT–WIRING DIAGRAM



NOTES
1. U23-U27 & U30-U31 ARE DH3725CN
2. ALL CAPACITOR VALUES ARE IN μF UNLESS STATED OTHERWISE
3. ALL RESISTANCE VALUES ARE IN OHMS UNLESS STATED OTHERWISE $K = 10^3\Omega$, $M = 10^6\Omega$
4. INPUTS ARE DESIGNATED BY ≻—— ; OUTPUTS BY ——→
5. LAST CKT SYMBOLS USED: C50, CR3, Q4, R50, U31

(REVISED 7-11-75)

COAST GUARD		ELECTRONICS ENGINEERING CENTER WILDWOOD NEW JERSEY
Project No: W0686		Title: W0686-1A/ALARM STATUS ALARM MODULE; SCHEMATIC DIAGRAM
Drawn By: W. T. F	Checked By:	
Project Eng:	Scale:	
Approved By: USCG COMMANDING OFFICER	Date: 11-26-74	Drawing No:	Sheet: of

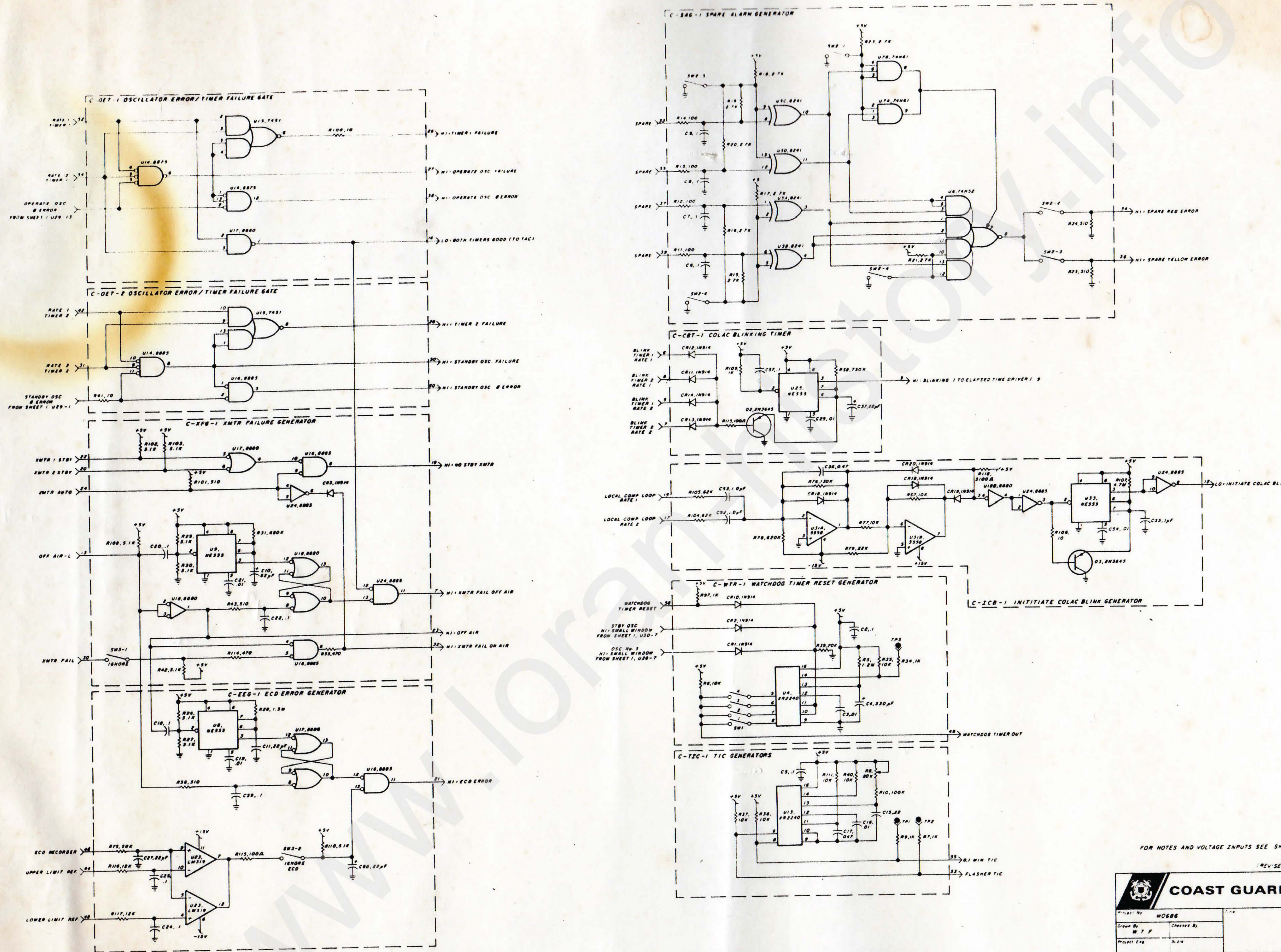


NOTES: 1. Unless otherwise stated all resistance values are in Ω, $K = 10^3\Omega$, $M = 10^6\Omega$.
2. Unless otherwise stated all capacitor values are in μf.
3. Inputs are designated by ≻—, outputs by →.
4. Last circuit symbols used: C59, CR20, E17, Q3, R118, U32. Symbols not used: C35, CR15, CR16, R22, R36.

(REVISED: 4-8-75) (REVISED 7-8-75)

COAST GUARD
ELECTRONICS ENGINEERING CENTER
WILDWOOD NEW JERSEY

Project No W0686	Title W0686-2A / STATUS COMPILER	
Drawn By J.E.F W.T.F	Checked By	
Project Eng	Scale	
Approved By USCG COMMANDING OFFICER	Date 3-7-74	Drawing No 686-D-108
		Sheet 1 of 2



FOR NOTES AND VOLTAGE INPUTS SEE SHEET 1

(REVISED 7-11-75)

COAST GUARD	ELECTRONICS ENGINEERING CENTER WILDWOOD NEW JERSEY
Project No W0686	Title STATUS COMPILER
Drawn By W.T.F	Checked By
Project Eng	Scale
Approved By USCG COMMANDING OFFICER	Date 3-21-75
Drawing No	Sheet 2 of 2

☆U.S. GOVERNMENT PRINTING OFFICE: 1975-608-426/504