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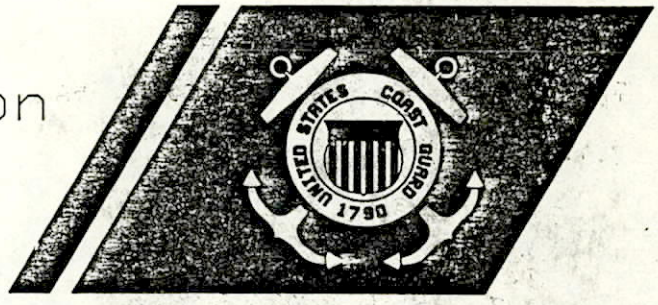

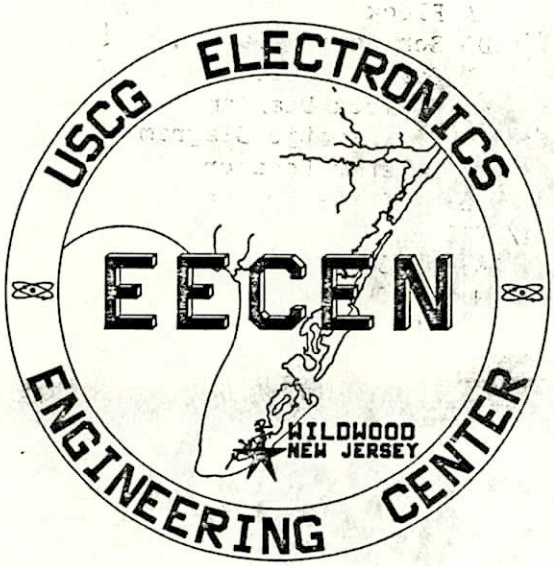

TECHNICAL MANUAL
FOR
AN/FPN-54A AND AN/FPN-65
LORAN-C TIMER SETS

CG7610-01-GE0-5405

LORAN-C TIMER SET
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1. GENERAL INFORMATION.

1.1. Introduction. This Technical Manual provides a description of the various units of the AN/FPN-54A and AN/FPN-65 Loran-C Timer Sets (LTS). The Loran-C Timer Set establishes and maintains the Loran-C timing reference based on a frequency standard input, generates the required Loran-C transmitter control waveforms, and provides the necessary signal conditioning to drive the installed transmitter. The AN/FPN-54A Loran-C Timer Set is used with the AN/FPN-39, AN/FPN-42, AN/FPN-44/44A, and AN/FPN-45 Transmitters. The AN/FPN-65 Loran-C Timer Set is used with the AN/FPN-64(V) Transmitter.

1.1.1. Nomenclature. For clarity, the following Loran-C system nomenclature will be used throughout this manual:

a. AN/FPN-54A or AN/FPN-65 Loran-C Timer Set may be referred to as follows:

(1) Loran-C Timer Set
(2) Timer Set
(3) LTS

b. TD-989-A/FPN-54A or TD-1365/FPN-65 Loran-C Timer may be referred to as follows:

(1) Loran-C Timer
(2) Loran Timer
(3) Timer

c. C-8621A/FPN Timer Set Control may be referred to as follows:

(1) Timer Set Control
(2) TSC

1.1.2. Equipment List. Table 1.1 lists the units of the Loran-C Timer Set covered in this manual.

NOTE

A Loran Transmitting Station will have either an AN/FPN-54A or an AN/FPN-65 LTS installed. Differences will be discussed throughout this Technical Manual.

Table 1.1. List of Loran-C Timer Set Equipments

Reference Designation	Equipment Description	Nomenclature
1	Electrical Equipment Cabinet (Includes 1T1 Isolation Transformer)	CY-7529/FPN
1A1	Loran-C Timer (Number 1)	TD-989A/FPN-54A or TD-1365/FPN-65
1A2	Timer Set Control	C-8621A/FPN
1A3	Loran-C Timer (Number 2)	TD-989A/FPN-54A or TD-1365/FPN-65
1A4	Backup Power Supply	PP-7839/G

1.2. General Description. Figure 1.1 shows a typical Loran-C Timer Set. At dual-rated Loran-C transmitting stations, two Loran-C Timer Sets will be installed; one for each rate.

1.2.1. Loran-C Timer Set Functions. The Loran-C Timer Set performs the following functions:

a. Provides the timing and control signals necessary to generate the Transmitter Drive Waveform.

b. Adjusts the signals to compensate for changes in local signal path delays.

c. Provides a means for external adjustment (local or remote) of the time of transmission of the Loran-C pulse.

1.3. Unit Description.

1.3.1. Loran Timer (1A1). The top TD-989/FPN-54A or TD-1365/FPN-65 Loran-C Timer (Figure 1.2) is designated 1A1 and will be referred to as Timer Number 1. It is referred to as the OPERATE Timer when it is actually providing signals and controlling the Loran transmission; otherwise, it is referred to as the STANDBY Timer. The Loran Timer provides accurate timing of the transmitter drive signals to control the time of transmission of the radiated Loran-C pulses. The Loran Timer requires an input from a frequency standard and the Operate RF feedback signal. It may also use Cross-Rate Blanking, Remote Control, and Communication Modulation signals where required. The Loran Timer (TD-989A/FPN-54A and TD-1365/FPN-65) performs the following functions:

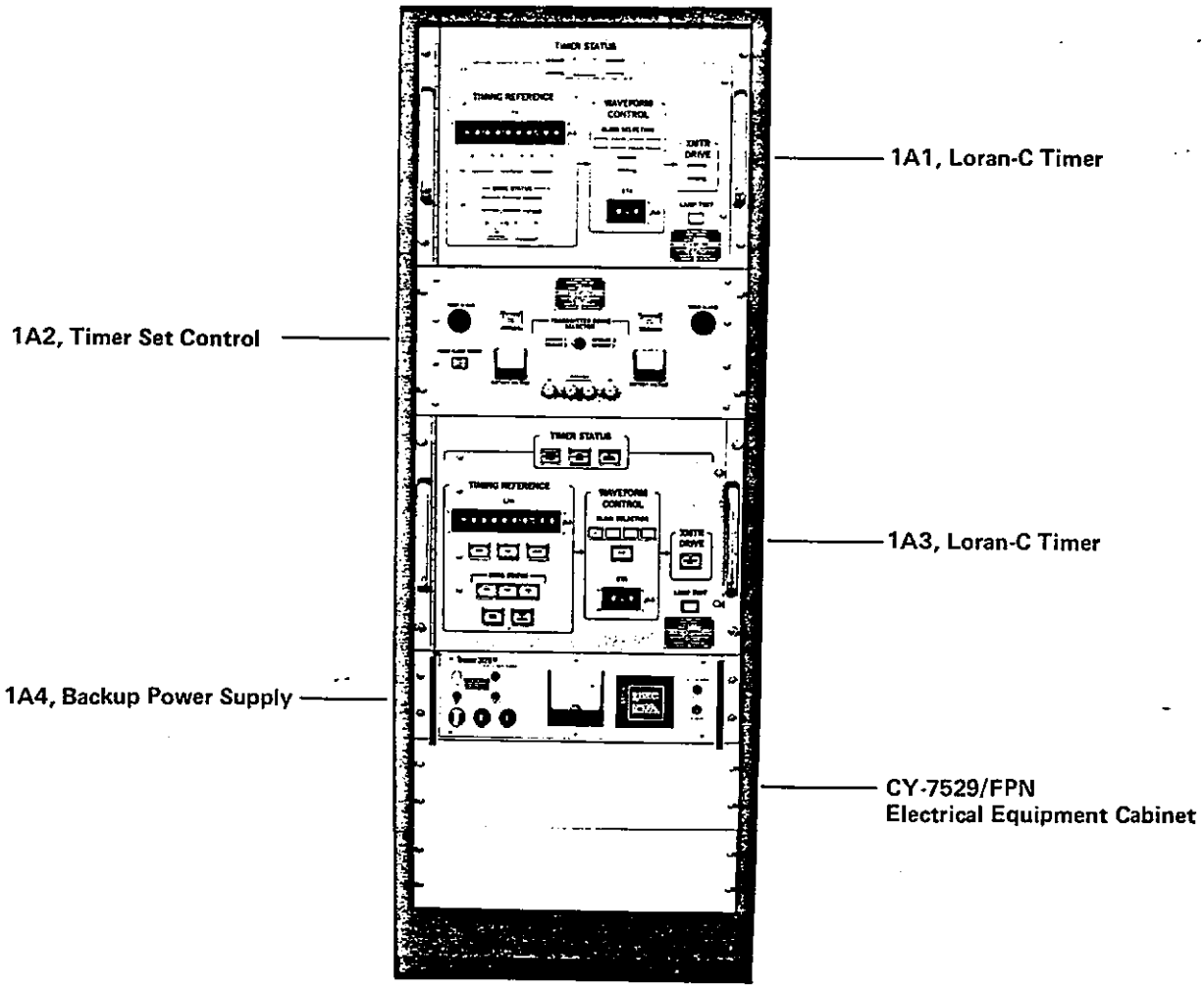


Figure 1.1. Loran-C Timer Set (Front View)

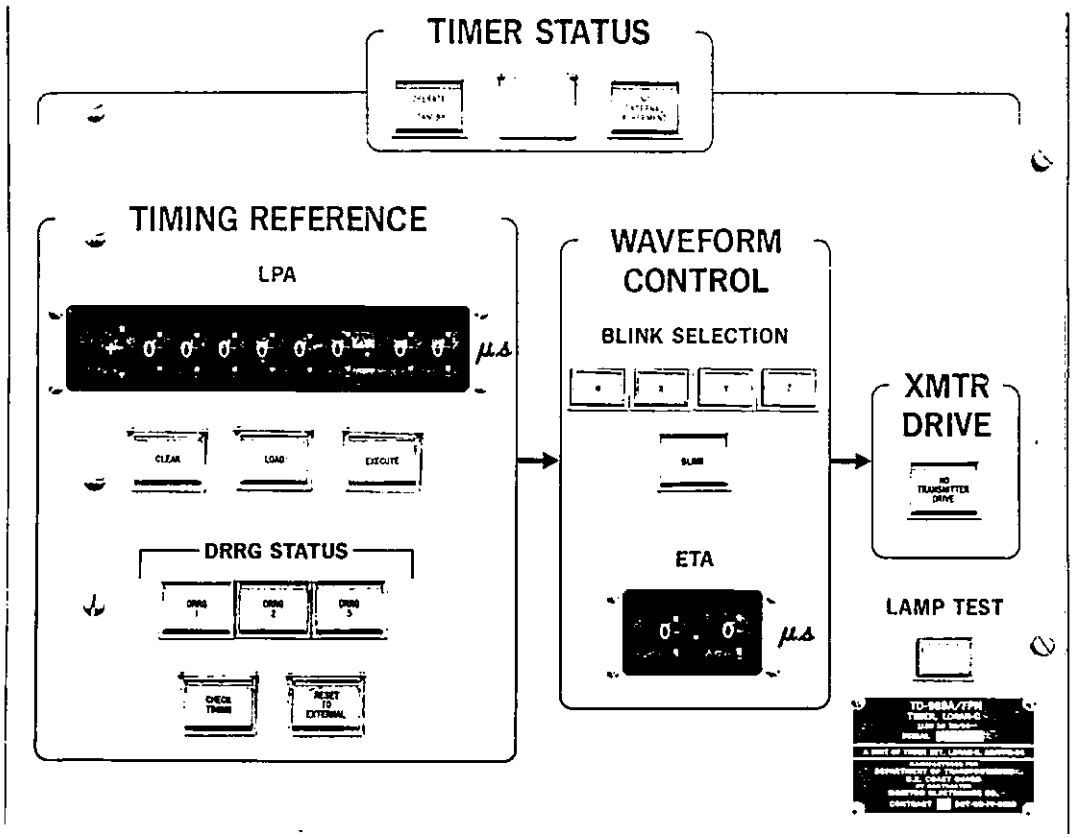


Figure 1.2. Loran Timer

a. Establishes and maintains a timing reference based on a 5-MHz sine wave signal input via three independent Digital Repetition Rate Generators (DRRGs).

b. Provides a way to externally adjust the timing reference by local or remote insertion of Local Phase Adjustments (LPAs). (Note: Coding Delay Adjustment (CDA) is another term for LPA.)

c. Monitors and displays external synchronization status of three Digital Repetition Rate Generators (DRRGs). Monitors timing agreement of all DRRGs, and automatically corrects any individual DRRG misalignment.

d. Synchronizes the DRRG reference of one Loran Timer to the other upon depressing the RESET TO EXTERNAL switch.

e. Provides a way to advance or retard the start of the Loran-C pulse envelope by insertion of Envelope Timing Adjustments (ETAs) to the TD-989A/FPN-54A Loran Timer. The TD-1365/FPN-65 Loran Timer does not use ETAs. The ETA dial for the TD-1365/FPN-65 Loran Timer is set to 0.1 and must remain at that setting.

f. Starts or stops Loran-C Blink on receipt of LOCAL or REMOTE commands.

g. Provides the following waveforms:

(1) Multipulse Triggers (MPTs)
(2) 100 kHz (used only on TD-989/FPN-54A Loran Timer)
(3) Phase Code Interval (PCI)
(4) Phase Code Set and Phase Code Reset
(5) Local Interval (LI)
(6) 5 MHz (used only with TD-1365/FPN-65 Loran Timer)

h. Receives Pulse Position Modulation (PPM) from a data link to adjust the time of transmission of Loran-C pulses, which provides communications using Loran-C signals.

i. Provides Local Interval blanking signals for dual-rate operation.

j. Adjusts the timing of transmitter drive signals to maintain a fixed time relationship between the fixed timing reference and the antenna current signal, thereby compensating for changes in the local signal path delay.

1.3.1.1. The TD-989/FPN-54A and TD-1365/FPN-65 Loran Timers contain the following modules:

	Description	Designation *
a.	DC Power Supply, Regulated, 5 VDC, 5 AMP	1A1A4
b.	DC Power Supply, Regulated, 28 VDC, 4 AMP	1A1A5
c.	DC Power Supply, Regulated, ±15 VDC, 0.3 AMP	1A1A6
d.	DC Power Supply, DC to DC Converter 28 VDC to 5.0 VDC, 10 AMP	1A1A7
e.	Front Panel Module WO486-21/FRONT PANEL	1A1A1A
f.	Coding Delay Adjust Module WO486-5A/CDA (Local)	1A1A1B
g.	Coding Delay Adjust Module WO486-5A/CDA (Remote)	1A1A1C
h.	Phase Shift Module WO486-4A/Ø-SHIFT	1A1A1D
i.	Digital Repetition Rate Generator Module WO486-3A/DRRG 1	1A1A1E
j.	Digital Repetition Rate Generator Module WO486-3A/DRRG 2	1A1A1F
k.	Digital Repetition Rate Generator Module WO486-3A/DRRG 3	1A1A1G
l.	Program Module WO486-7/PROGRAM	1A1A1H
m.	Control Module WO486-12A/CONTROL	1A1A1J
n.	Phase Code/MultiPulse Trigger Module WO486-30/PC/MPT	1A1A1K
o.	Envelope Timing Adjustment Module WO486-11/ETA	1A1A1L
p.	Error Sense Module WO486-10E/ERR SNS	1A1A1M
q.	Phase Shift Module WO486-4A/Ø-SHIFT	1A1A1N
r.	Blink Module WO486-6A/BLINK	1A1A1P
s.	Interface Module WO486-8A/INTERFACE	1A1A1R
t.	Signal Module WO486-22/SIGNAL	1A1A1S
u.	Dual-rate Interface/Communications Phase Shift Module WO486-28B/DRINT/CP	1A1A1T

* Prefix designation 1A1 is for Timer Number 1. Timer Number 2 will use prefix designation 1A3.

1.3.2. Timer Set Control (1A2). The C-8621A/FPN Timer Set Control (TSC) is used in both the AN/FPN-54A and AN/FPN-65 Loran Timer sets. The Timer Set Control (Figure 1.3) performs the following functions:

a. Selects either Timer Number 1 or Timer Number 2 as the Operate Timer.

b. Provides an audio alarm (on the Timer Set Control) upon detection of a Loran Timer red alarm.

c. Displays the voltage level of the 28 VDC Backup Power Supply.

d. Distributes 5 MHz and antenna current feedback signals to Timer Number 1 and Timer Number 2.

e. Distributes 115 VAC power to Timer Number 1 and Timer Number 2. Distributes 28 VDC backup power to either or both Loran Timers, depending on station equipment configuration.

f. Distributes transmitter drive signals to units in the AN/FPN-60(V) Transmitter Control Set (TCS) equipment rack, when used with the AN/FPN-54A Loran-C Timer Set.

g. Distributes transmitter drive signals to units in the AN/FSN-3 Local Status Monitor (LSM) equipment rack, when used with the AN/FPN-65 Loran-C Timer Set.

h. Provides drive signals for the cycle compensation loop chart recorder.

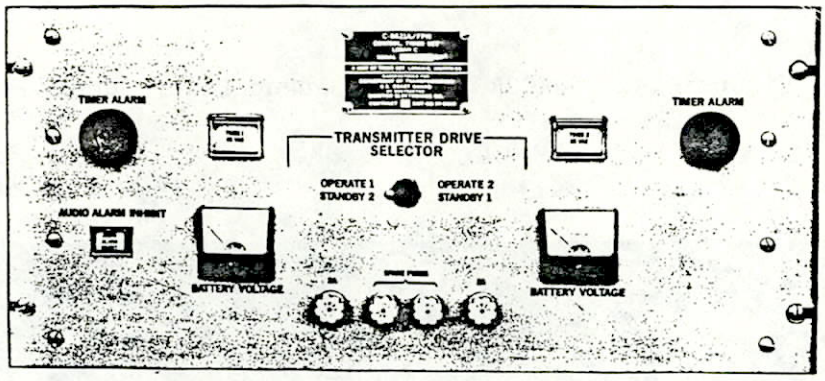


Figure 1.3. Timer Set Control

1.3.3. Loran Timer (1A3). The bottom Loran Timer (Figure 1.2) performs the same functions as the 1A1 Loran Timer, and is designated 1A3, and will be referred to as Timer Number 2.

NOTE

The input and output jacks located on the rear apron of the 1A1 and 1A3 Loran Timers are labeled identically. When referring to Timer Number 1, use 1A1A3J1, 1A1A3J2, etc..., and when referring to Timer Number 2, use 1A3A3J1, 1A3A3J2, etc...

1.3.4. Backup Power Supply (1A4). The PP-7839/G Power Supply, TRACOR 312 (D) (Figure 1.4), provides 28 VDC power, with battery backup to the 1A2 Timer Set Control. The Backup Power Supply receives input power from the main breaker panel and not from the 1T1 Isolation Transformer.

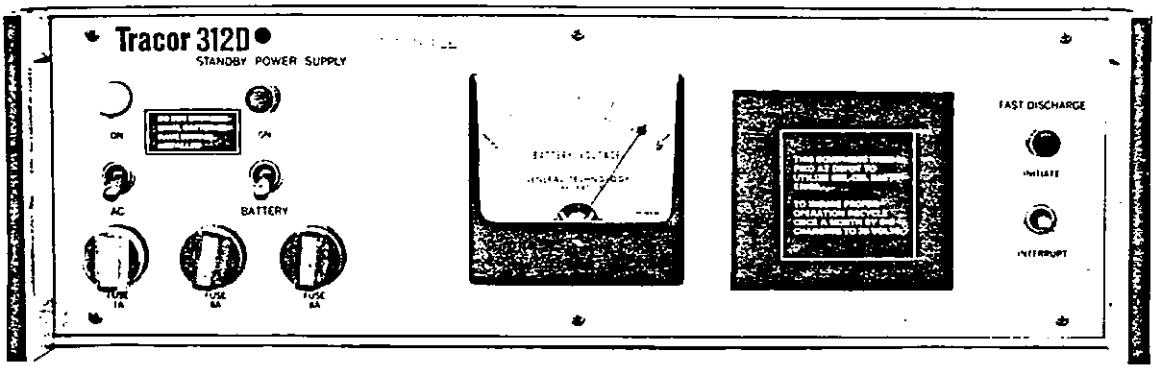


Figure 1.4. TRACOR 312 (D) Backup Power Supply

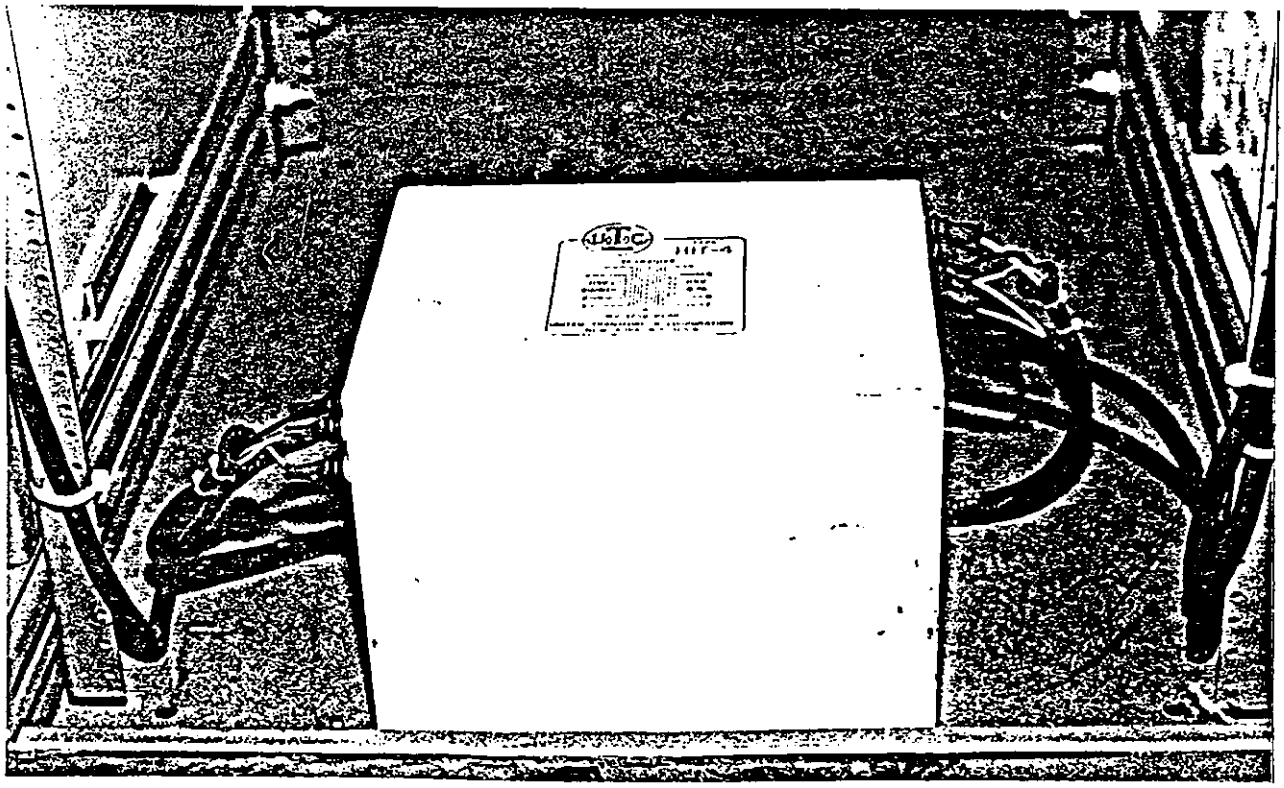


Figure 1.5. Power Isolation Transformer (Rear View)

1.3.5. Isolation Transformer (1T1). The Power Isolation Transformer (Figure 1.5) is part of the Electrical Equipment Cabinet (1) and isolates the AC power input to the 1A2 Timer Set Control.

1.4. Reference Data. Table 1.2 lists the electrical power requirements of the units in the Loran-C Timer Set. Tables 1.3 and 1.4 list specifications of the equipment supplied and the equipment required but not supplied, respectively. Figure 1.6 is a block diagram showing the relationships of the units of the LTS and a typical suite of associated peripheral equipment.

Table 1.2. Electrical Power Requirements

EQUIPMENT	INPUT POWER
Loran-C Timer Set	115 VAC ± 10% 50-60 Hz, single phase 620 W
Loran Timer 1A1 or 1A3	115 VAC ± 10% 50-60 Hz, single phase 250 W
Timer Set Control 1A2	115 VAC ± 10% 50-60 Hz, single phase
Backup Power Supply 1A4	90-130 VAC 48-420 Hz, single phase 120 W

1.4.1. Loran-C Timer Set Specifications. The following are the timing reference stability specifications of the LTS:

a. Short-term timing stability is less than 10^{-9} second jitter.

b. Long-term timing stability is that of the frequency standard input.

c. Timing accuracy as a function of temperature is $+2.5 \times 10^{-10}$ Sec/°C from 25 to 50 °C.

d. Operating temperature is from 0 to 55 °C.

e. Output signal resolution is 20 nSec.

1.4.2. Loran-C Timer Set Input Requirements. The following are the input requirements of the LTS:

a. 115 VAC, 10 Amp, Single Phase.

b. Operate RF, 12 to 15 V_{p-p} into an impedance of 50 ohms.

c. 5-MHz signal, 2.5 V RMS into an impedance of 50 ohms.

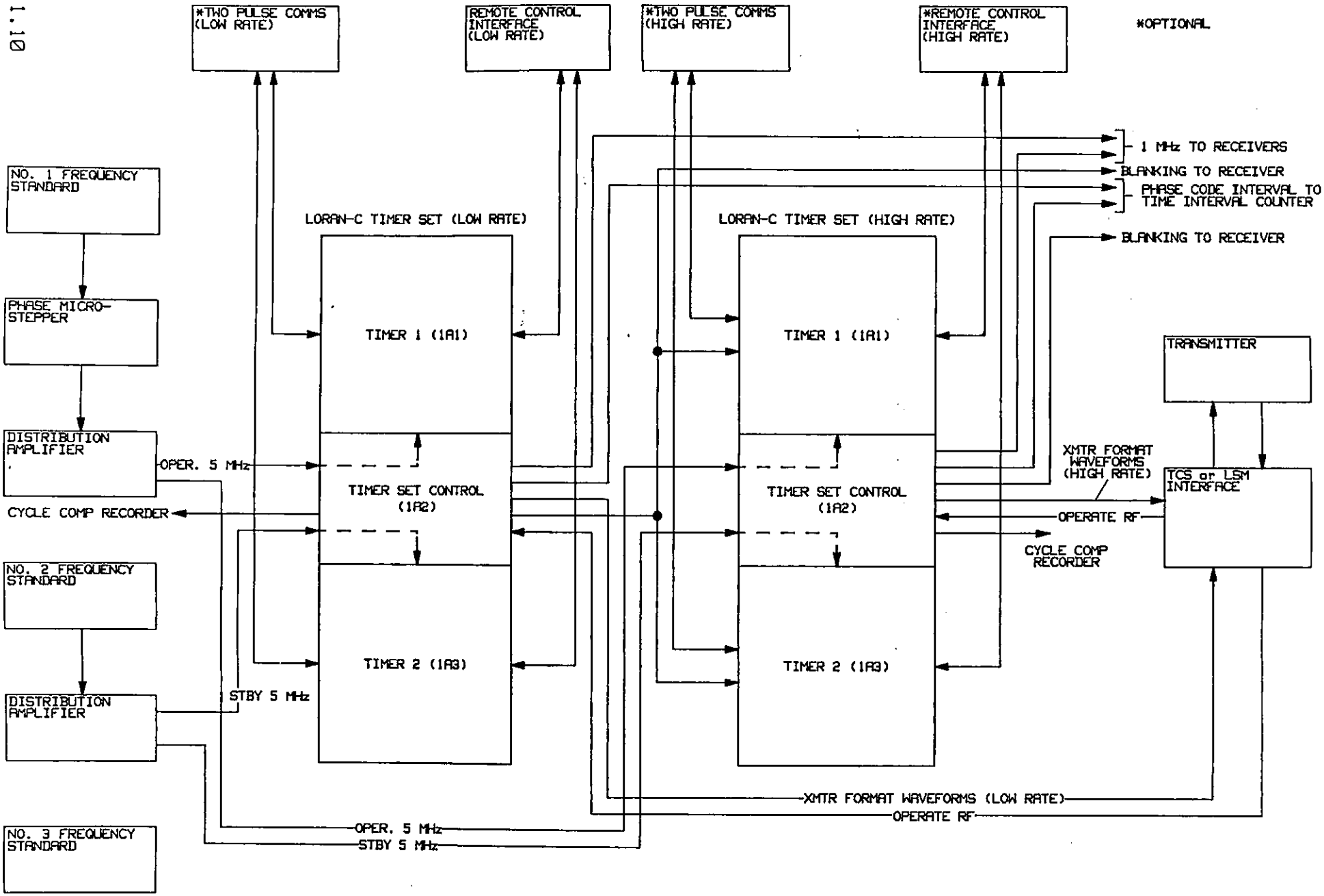


Figure 1.6. Block Diagram of Loran-C Timer Sets and Peripheral Equipment in a Dual-Rate Configuration

Table 1.3. Equipment Supplied

QUANTITY PER EQUIPMENT (Note A)	NOMENCLATURE		OVERALL DIMENSIONS			VOLUME	WEIGHT
	NAME	DESIGNATION	HEIGHT	WIDTH	DEPTH		
2	Loran Timer	TD-989A/FPN-54A (Note B)	14.0 in 35.6 cm	19.0 in 48.3 cm	24.0 in 61.0 cm	3.7 ft^3 .105 m^3	45 lbs 20.4 Kg
1	Timer Set Control	C-8621A/FPN	8.75 in 21.9 cm	19.0 in 48.3 cm	13.0 in 33.0 cm	1.25 ft^3 .035 m^3	20 lbs 9.1 Kg
1	Backup Power Supply Tracor 312 (D)	PP-7839/G	5.25 in 13.1 cm	19.0 in 48.3 cm	12.3 in 31.2 cm	.71 ft^3 .020 m^3	54 lbs 24.5 Kg
1	Electrical Equipment Cabinet	CY-7529/FPN	60.0 in 152.4 cm	22.5 in 57.2 cm	31.1 in 79.0 cm	21.8 ft^3 .617 m^3	110 lbs 50.0 Kg
1	Power Isolation Transformer		8.0 in 20.3 cm	9.0 in 22.9 cm	8.0 in 20.3 cm	.34 ft^3 .009 m^3	35 lbs 15.9 Kg

NOTE: A. Each quantity is doubled for a dual-rated station.
B. TD-1365/FPN-65 used with AN/FPN-64(V) Transmitter.

Table 1.4. Equipment Required but not Supplied

QUANTITY PER EQUIPMENT	NOMENCLATURE		REQUIRED USE	REQUIRED CHARACTERISTICS
	NAME	DESIGNATION		
1	Oscilloscope	AN/USM-281 (or equivalent)	Installation; Alignment and Testing	50 MHz Bandwidth; dual channel 10 millivolt sensitivity; delayed sweep
1	Analog Multimeter	CSV-260 (or equivalent)	Installation; Alignment and Testing	50 Volts DC; 150 Volts AC; 5 Amps DC;
1	Digital Multimeter	CCUH-8000A (or equivalent)	Installation; Alignment and Testing	200 ohms to 5 Megohms; 50 Volts DC; 150 Volts AC; 5 Amps DC;
1	Resistor		Installation and Testing	1 ohm, 50 Watt

1.4.3. Loran-C Timer Set Cycle Compensation Loop. The following are the Cycle Compensation Loop specifications for the LTS:

a. Slew rate is ±20 nSec per GRI when the operate RF is outside the timing reference. (When error is greater than ±1.5 uSec.)

b. Time constant is hardware selectable (See Table 2.10).

c. Range is ±5 uSec.

1.5. Inquiries. For logistics support, Supply Center Brooklyn is the Inventory Control Point (ICP). Refer to E/GICPINST 4408.1 (series) for XB stock numbers. For logistics assistance, contact Customer Services Branch at Supply Center, Brooklyn, New York.

NOTE

For the latest version of the E/GICPINST 4408.1 (series) Instruction, contact:

Commanding Officer (code 340)
U. S. Coast Guard Supply Center
830 Third Avenue
Brooklyn, NY 11232

For repair and maintenance support, contact the Intermediate Level Assistance Office for your unit.

1.6. Abbreviations. The abbreviations used throughout this manual are listed and defined in Table 1.5.

Table 1.5. List of Abbreviations

BCD	Binary Coded Decimal
CDA	Coding Delay Adjustment
CMPT	Coarse Multipulse Trigger
CP	Clarinet Pilgrim
Cycle Comp	Cycle Compensation Loop
DRRG	Digital Repetition Rate Generator
ECD	Envelope-to-Cycle Difference
EMPT	Early Multipulse Trigger
ET	Early Trigger
ETA	Envelope Timing Adjustment
GRI	Group Repetition Interval
IAW	In accordance with
LI	Local Interval
LORTO	Loran Time Zero
LPA	Local Phase Adjustment
LTS	Loran Timer Set
LSM	Local Status Monitor
MPT	Multipulse Trigger
mSec	Millisecond
nSec	Nanosecond
OP	Operate
PC	Phase Code
PCI	Phase Code Interval
PGEN	Pulse Generator
PMPT	Pseudo Multipulse Trigger
PPM	Pulse Position Modulation
PROM	Programmable Read Only Memory
P/S	Power Supply
RCG	Remote Control Group
RCI	Remote Control Interface
RF	Radio Frequency
ROS	Remote Operating System
Sec	Second
SAU	Status Alarm Unit
SPDT	Single Pole Double Throw
SSX	Solid-State Transmitter
STBY	Standby
TCS	Transmitter Control Set
TIC	Time Interval Counter
TPC	Two-Pulse Communications
TSC	Timer Set Control
TTL	Transistor-Transistor Logic
TTY	Teletype
UPS	Uninterruptible Power Supply
uSec	Microsecond
OTHER RATE	For dual-rate stations, the rate not being discussed
SAME RATE	For dual-rate stations, the rate that is being discussed

1.7. Safety Hazards. This manual is for use by the operator and technician. Therefore, it is incumbent upon that person to be familiar with potential electrical, mechanical, and environmental hazards associated with the Loran-C Timer Set.

1.7.1. Power Distribution. AC and DC power is distributed to Loran Timers, (1A1) and (1A3), by the Timer Set Control (1A2). Securing power to either Loran Timer requires a manual trip of the respective circuit breaker (on the Timer Set Control). To de-energize one of the Loran Timers, disconnect the 115 VAC and 28 VDC power harnesses from the Timer Set Control (1A2) to the Loran Timer. To de-energize the entire LTS, disconnect the 28 VDC backup power harness and trip the main circuit breaker, and if applicable, disconnect the 115 VAC from the Frequency Standard UPS.

WARNING

When securing power to either Loran Timer, a potential shock hazard still exists, because the circuit breaker only opens one side of the AC line to the Loran Timer, and AC voltage remains on the return line. Also, 28 VDC remains in the LTS when the AC circuit breaker is tripped.

CAUTION

When all power is removed from Loran Timer 1A1, TTL voltage (5 volts) will remain due to the signal interconnect harness from Loran Timer 1A3. Components in the Loran Timer may be damaged by shorting a power supply or signal lines when in this status. The same is true when power is removed from Loran Timer 1A3.

1.7.2. Reference Publications. Technical personnel must be familiar with the information regarding safety in the following publications:

a. M10550.13 - Electronics Manual, Administration and Supply

b. M10550.14 - Electronics Manual, Maintenance

c. M10550.15 - Electronics Manual, Engineering

d. M5100.29 - Safety Manual

e. M11000.1 - Civil Engineering Manual

f. CG-139 - Cardiopulmonary Resuscitation Handbook

g. CG-516 - First Aid Health Lesson Plan

1.7.3. Notes, Cautions, and Warnings. Notes, Cautions, and Warnings will be used in this manual to emphasize important instructions, procedures, and conditions. They will have the following format:

a. NOTE:

NOTE

"Notes" will be used for narrative or illustrative non-procedural data.

b. CAUTION:

CAUTION

"Cautions" will be used to call particular attention to a step or procedure which, if not strictly followed could result in damage to, or destruction of equipment.

c. WARNING:

WARNING

"Warnings" will be used to call particular attention to a step or procedure which, if not strictly followed, could result in serious injury to, or death of personnel.

2. INSTALLATION.

2.1. Introduction. This chapter provides procedures for unpacking and inspecting the Loran-C Timer Set. It describes procedures for installing, programming, adjusting, and initially operating each unit of the LTS. Procedures for the de-installation and shipment of the equipment are also included in this chapter.

2.2. Unpacking and Initial Inspection.

2.2.1. Inspect the shipping containers for external damage. If the containers are damaged, have the carrier's agent present when the containers are unpacked.

2.2.2. After unpacking the containers, inspect the chassis, modules, and cables for physical damage. Inspect all electrical wiring and connections to ensure that connections have not been damaged. Inspect for damage and note any scratches, dents, broken wires, or indicator/switches on the units.

2.3. Installation Instructions.

2.3.1. Materials. Table 2.1 lists the materials that are supplied, and Table 2.2 lists the materials that are required but not supplied for installing the LTS units.

2.3.2. General Installation Procedures.

2.3.2.1. Consider the following specifications before connecting the cables to the units in the LTS:

a. Cables that connect primary AC power, DC back-up power, timer room ground, and other required signals to the electrical equipment cabinet, may be routed through the bottom of the cabinet. The bottom opening is rectangular, and is designed to be placed over the signal building trenching. Stations that do not have signal trenches or computer deck must run cables in overhead ducting.

b. The primary 115 VAC power cable connecting the main circuit breaker panel to the terminal board in the electrical equipment cabinet shall have a minimum conductor size of AWG 14. Also, the primary power circuit breaker shall have a rating of 10 amperes.

WARNING

Before connecting the primary AC power cable to the main circuit breaker panel, place (and properly tag) the circuit breaker to its OFF position.

Table 2.1. Materials Supplied

Quantity per Equipment	Nomenclature		Dimensions		
	Name	Designation	Length	Width	Depth
32	Mounting Screws	10-32	1.0 in		
32	Captive Nuts	10-32			
2	Interconnect Timer Signal Harness	WO486-24-W104	43.0 in		
2	115 VAC Power Harness	W101	66.0 in		
2	115 VAC Inter-connect Power Harness	W102	43.0 in		
1	28 VDC Power Harness	W105	66.0 in		
2	28 VDC Inter-Connect Power Harness	W103	43.0 in		
4	Chassis Slide Mechanism				

Table 2.2. Materials Required but not Supplied

Quantity per Equipment	Nomenclature		Required Use and Characteristics
	Name	Designation	
1	Coaxial Cable	RG-58/U	Cross rate blanking for dual-rated stations. BNC connectors and Coaxial Tee required.
1	AC Power Cable	IAW local codes	Primary AC Power from external circuit breaker to terminal board 1TB1.
1	RF Feedback Cable	RG/22B/U	Operate RF Feedback.

2.3.2.2. Specific cable runs are classified by noise susceptibility. Red cable markers denote primary power AC, uninterruptible power (UPS) AC and, TTY current loops. Yellow cable markers denote frequency distribution cables (5 MHz, 1 MHz, and 100 kHz), high level phasing signals, PCI, and TCS or LSM drive signals. White cable markers denote low level RF, TTL logic levels (0-5 VDC), and analog signals. In order to minimize capacitive and inductive cross talk, observe the following procedures:

a. Avoid parallel runs of different cable classes between racks and entrance panels.

b. When parallel runs of different classes of cables cannot be avoided, separate the cable classes by at least four feet. This separation applies even if cable runs are made using "Square-D" type metallic ducting.

c. When cables of different classes must intersect, they should intersect at right angles.

d. When cable runs must be installed overhead at pre-existing Loran stations which do not have computer flooring, avoid making "yellow" or "white" cable runs parallel to AC power wiring for fluorescent lights.

e. Some cable shields should be trimmed at one end and not connected. They should be connected to chassis ground at the other end to avoid ground loops. Refer to the Floor and Grounding Plan and Wire Running List for more information.

2.3.3. Electrical Equipment Cabinet.

2.3.3.1. The location of the AN/FPN-54A LTS equipment cabinet is to the left of the AN/FPN-60 Transmitter Control Set (TCS) equipment cabinet, as viewed from the front. For dual-rated stations, both LTS equipment cabinets are placed to the left of the TCS equipment cabinet. Specific locations of the individual units within the LTS are as shown in Figure 2.1.

2.3.3.2. The location of the AN/FPN-65 LTS equipment cabinet is to the left of the AN/FSN-3 Local Status Monitor (LSM) equipment cabinet, as viewed from the front. For dual-rated stations, both LTS equipment cabinets are placed to the left of the LSM equipment cabinet. Specific locations of the individual units within the LTS are shown in Figure 2.1.

WARNING

Ensure that the circuit breaker designated for this rack is OFF and properly tagged.

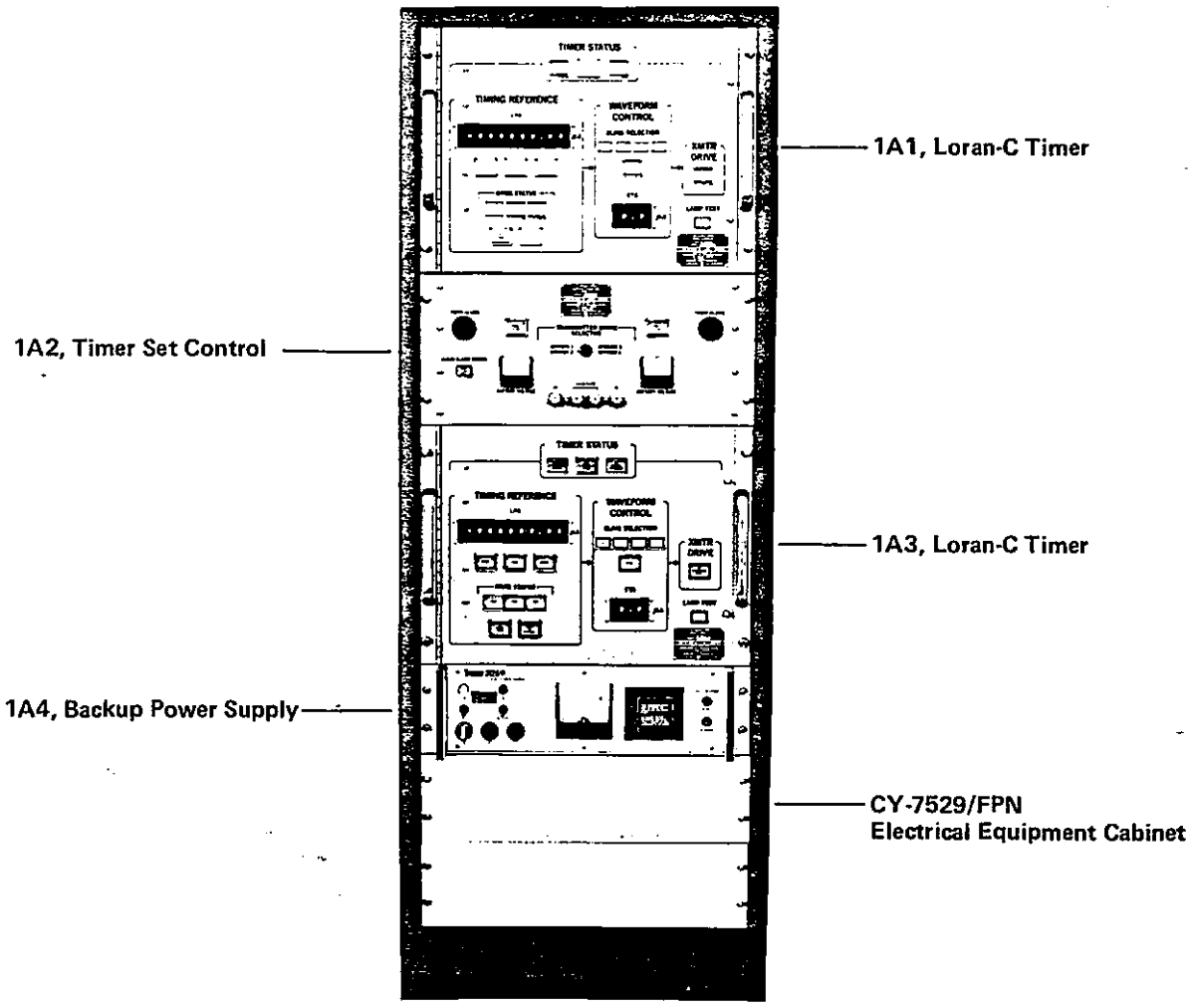
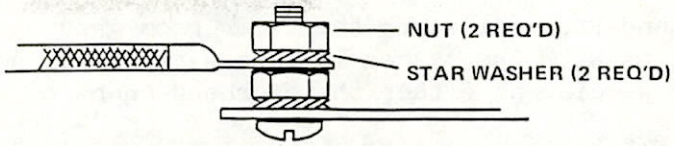


Figure 2.1. Loran-C Timer Set (Front View)



REMOVE PAINT FROM CABINET TO INSURE GOOD ELECTRICAL BOND

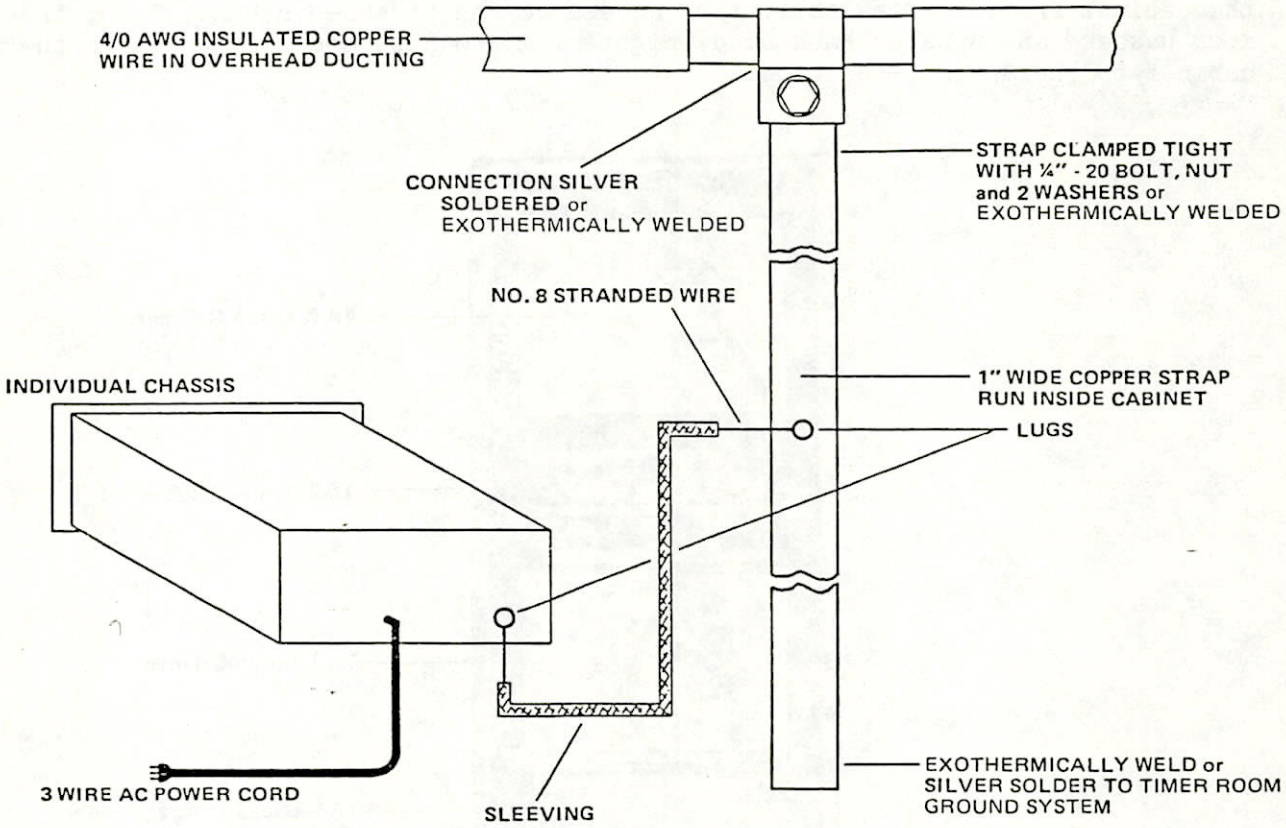


Figure 2.2. Typical Chassis and Cabinet Grounding Details

CAUTION

The Electrical Equipment Cabinet is on a separate circuit breaker, located inside the timer room. DO NOT energize the cabinet, until after the installation of all units. All units are energized upon the application of power.

2.3.3.3. Ground the cabinet to the timer room grounding system (see Figure 2.2). Local connection with the system is made with silver solder and pigtail connections or exothermic welding at either the overhead or below floor ducting.

2.3.4. Isolation Transformer.

2.3.4.1. Install the Isolation Transformer with the primary winding (3 terminals) on the left side of the equipment cabinet, and the secondary winding (4 terminals) on the right side as viewed from the rear (Figure 2.3). The transformer has four threaded studs on the bottom. Insert these studs through four holes in the bottom and to the rear of the equipment cabinet. While supporting the transformer, tilt the cabinet front to back permitting access to the threaded studs. Then, install lock washers and nuts on each stud, tightening the nuts securely. Return the cabinet to the upright position.

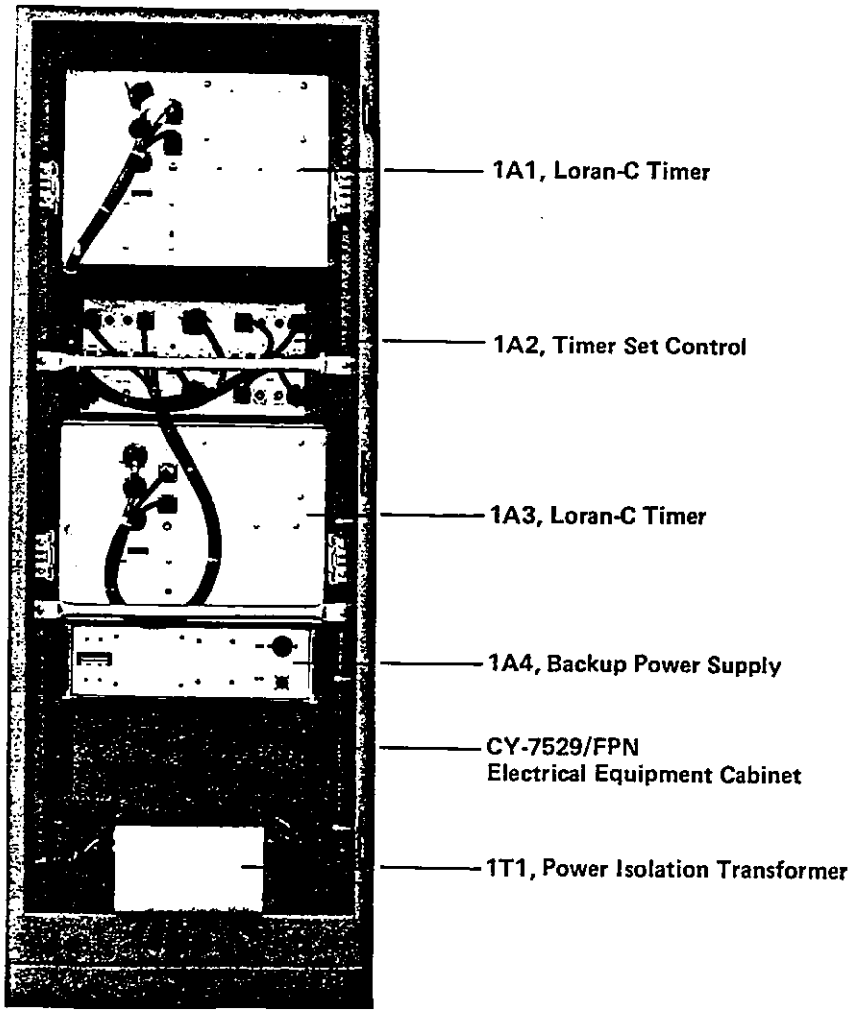


Figure 2.3. Electrical Equipment Cabinet (Rear View)

2.3.4.2. Refer to Figure 2.4 for primary power connections. Terminal Board 1TB1 is located directly in front of the Isolation Transformer in the base of the Electrical Equipment Cabinet. Route the primary AC power cable into the Electrical Equipment Cabinet and make the following connections:

a. Strap 1TB1-1, 1TB1-2, and 1TB1-3 together.

b. Strap 1TB1-4, 1TB1-5, and 1TB1-6 together.

c. Strap 1TB1-7, 1TB1-8, and 1TB1-9 together.

d. Connect a ground strap from 1TB1-5 to the equipment cabinet ground stud.

e. Connect the green lead from Isolation Transformer terminal 1T1-3 to 1TB1-4.

f. On Isolation Transformer (1T1) strap 1T1-4 and 1T1-7 together, then connect a green lead from 1T1-7 to 1TB1-6.

g. Connect a black lead from Isolation Transformer terminal 1T1-5 to 1TB1-3.

h. Connect a white lead from Isolation Transformer terminal 1T1-6 to 1TB1-7.

i. Connect the black lead of the primary 115 VAC power cable (from the breaker panel) to 1TB1-14.

j. Connect the white lead of the primary 115 VAC power cable (from the breaker panel) to 1TB1-15.

k. Connect the green lead of the primary 115 VAC power cable (from the breaker panel) to 1TB1-5.

l. Connect a black lead from Isolation Transformer terminal 1T1-1 to 1TB1-14.

m. Connect a white lead from Isolation Transformer terminal 1T1-2 to 1TB1-15.

n. Connect the black lead of Timer 1 115 VAC power harness (W101) to 1TB1-3.

o. Connect the black lead of Timer 2 115 VAC power harness (W101) to 1TB1-1.

p. Connect the white lead of Timer 1 115 VAC power harness (W101) to 1TB1-9.

q. Connect the white lead of Timer 2 115 VAC power harness (W101) to 1TB1-7.

r. Connect the green lead of Timer 1 115 VAC power harness (W101) to 1TB1-6.

s. Connect the green lead of Timer 2 115 VAC power harness (W101) to 1TB1-4.

t. Connect the black lead of the AC input from the 1A4 Power Supply to 1TB1-14.

u. Connect the white lead of the AC input from the 1A4 Power Supply to 1TB1-15.

v. Connect the green lead of the AC input from the 1A4 Power Supply to 1TB1-6.

w. Connect the white lead (positive) of the DC output from the 1A4 Power Supply to 1TB1-11.

x. Connect the black lead (negative) of the DC output from the 1A4 Power Supply to 1TB1-12.

y. Connect the white lead (positive) of the +28 VDC input (W105 Harness) to 1TB1-11.

z. Connect the black lead (negative) of the +28 VDC input (W105 Harness) to 1TB1-12.

NOTE

Ensure that all connections on 1TB1 are tight. Particular attention should be directed to the ground strap connections between 1TB1-5 and the electrical equipment cabinet ground stud.

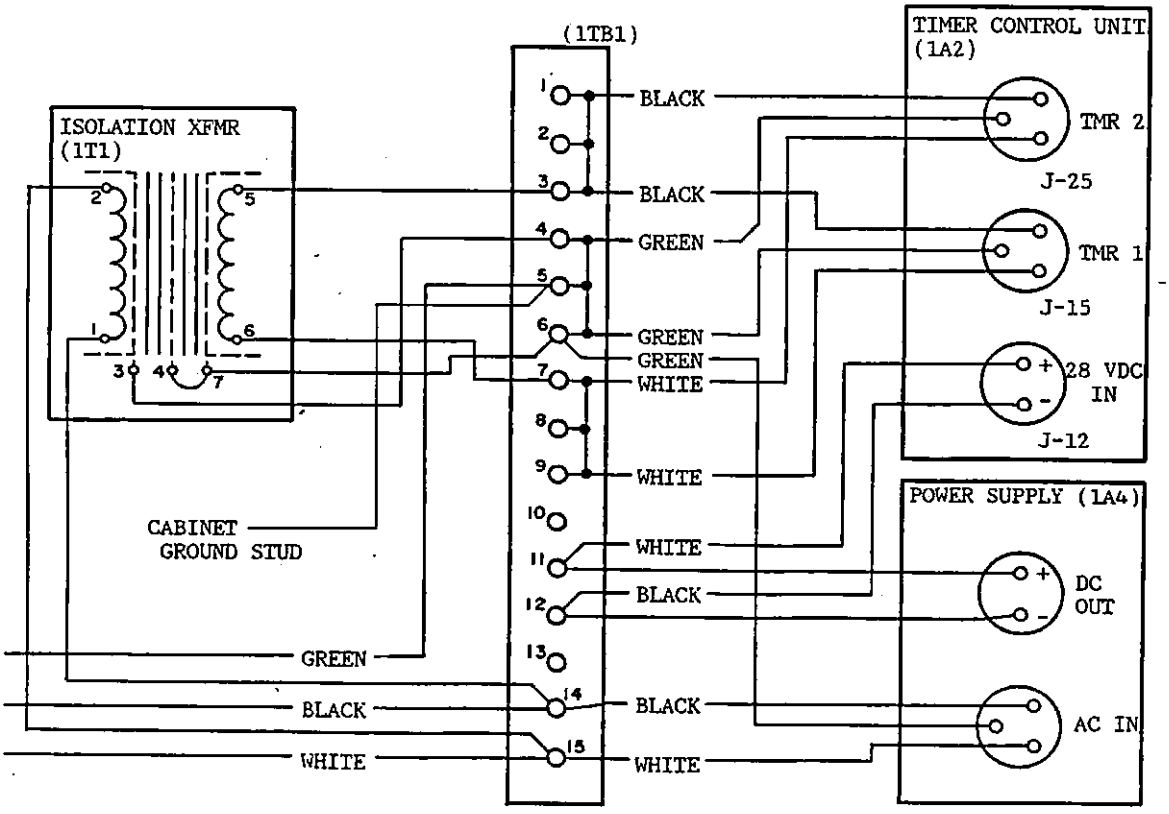
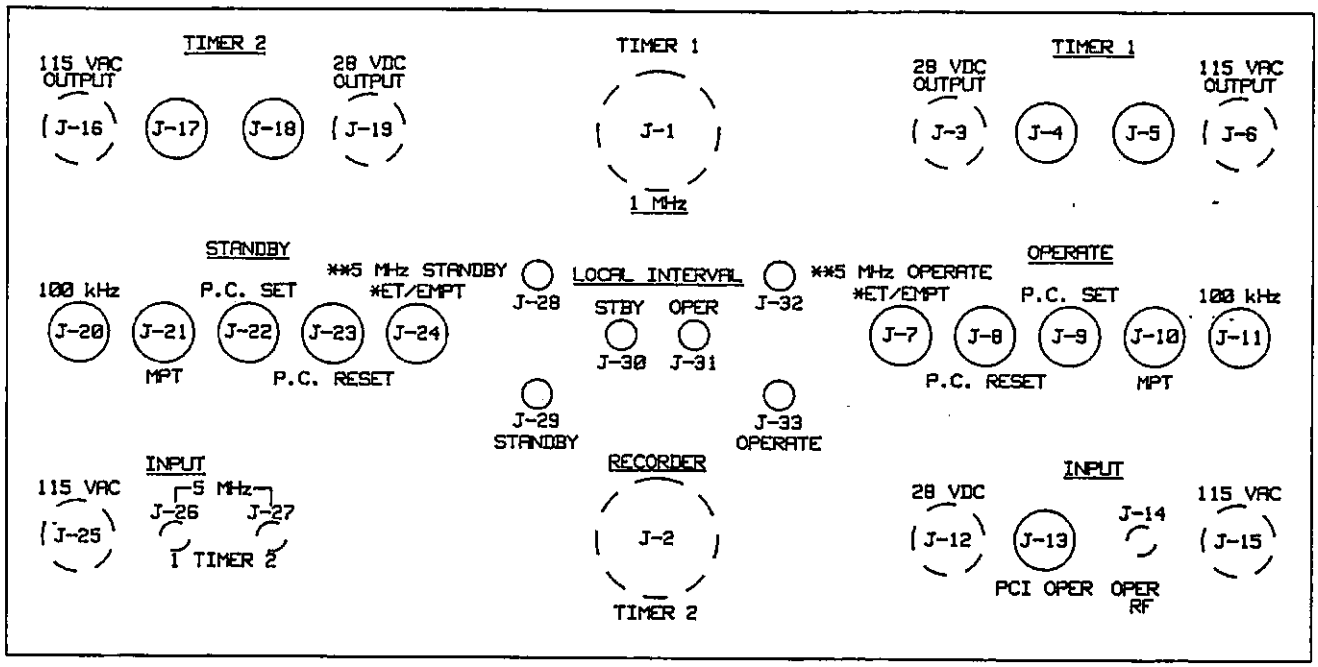


Figure 2.4. Connections for AC and DC Power

NOTE

See Figures 2.5 and 2.6 for Rear View of Timer Set Control (1A2) and Power Supply (1A4)



*AN/FPN-54A **AN/FPN-65

NOTE

Prefix all designations with 1A2A8. Solid Lines indicate those signals that are switched between Timer Number 1 and Timer Number 2 depending on position of Transmitter Drive Selector switch.

Figure 2.5. C-8621A/FPN Timer Set Control (Rear View)

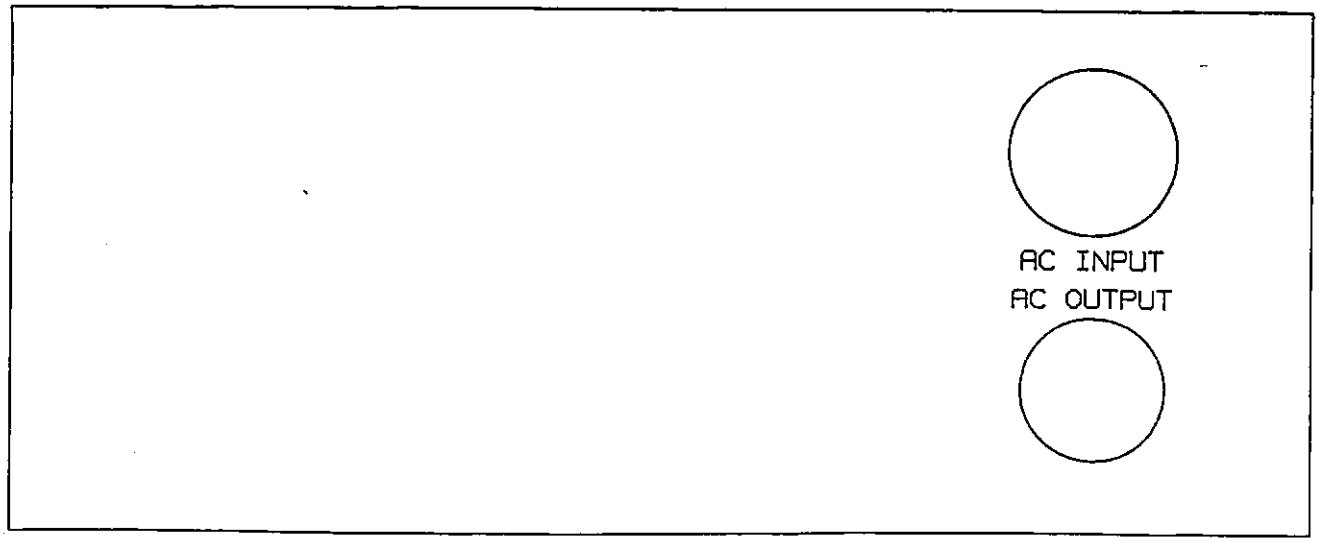


Figure 2.6. PP-7839/G Backup Power Supply (Rear View)

2.3.4.3. Anchor the LTS Electrical Equipment Cabinet by passing lag screws or bolts through the four holes located in the base of the cabinet, and secure to the deck.

2.3.4.4. The electrical equipment cabinet is a standard item that has been modified for Coast Guard use. Figure 2.3 shows the Electrical Equipment Cabinet (Rear View).

NOTE

Station drawings contain the types of cables used between the LTS and external equipment. This manual contains specifications for cables interconnecting the units of the LTS. All of the wiring and cabling in this chapter is for dual-rated stations. Single-rated stations will make connections to "low rate" jacks only.

2.3.5. Loran Timer (1A1).

2.3.5.1. Using the chassis slide mechanisms provided, install the 1A1 Loran Timer in the uppermost position of the Equipment Cabinet. Ensure that there is enough clearance so that the Loran Timer can slide in and out easily. If necessary, adjust the Loran Timer or slides for proper clearance.

WARNING

Ensure that the Equipment Cabinet is properly secured to the deck before extending the Timer chassis to its fully extended position.

2.3.6. Timer Set Control (1A2).

2.3.6.1. Position the Timer Set Control chassis directly beneath the 1A1 Loran Timer, and assemble the front panel screws and protective washers. Next, thread the panel screws into the cabinet mounting holes until the control chassis front panel is snug against the cabinet vertical support rails.

2.3.7. Loran Timer (1A3).

2.3.7.1. Position the 1A3 Loran Timer so that the side rails engage the chassis slide mechanism near the center of the cabinet just under the Timer Set Control. Carefully push the Loran Timer into the cabinet ensuring that there is enough clearance between the Loran Timer and the Timer Set Control. If the clearance is not adequate, adjust the position of the Loran Timer chassis and the chassis slide mechanism until both Loran Timers (1A1 and 1A3) may be inserted or withdrawn smoothly from the equipment cabinet. Once a proper fit is obtained, tighten all front panel mounting screws.

2.3.8. Backup Power Supply (1A4).

2.3.8.1. Position the Backup Power Supply beneath the 1A3 Loran Timer, and assemble the front panel screws and protective washers. Insert the panel screws in the cabinet mounting holes, and adjust the cabinet until the control chassis front panel is snug against the cabinet vertical support rails.

2.3.8.2. Route the primary AC and DC power cables for the Backup Power Supply in the Electrical Equipment Cabinet, and attach wires according to paragraph 2.3.4.2 (refer to Figure 2.4).

2.3.9. LTS Units Cable Interconnect. Once all units have been properly installed in the LTS equipment cabinet, and the primary and backup power cables have been connected, refer to Table 2.3 for the cable connections between the units in the LTS.

Table 2.3. LTS Units Cable Interconnect List

FROM	CABLE	TO
1TB1-3,6,9	115 VAC power harness (Timer Number 1)/W101	1A2A8J15
1TB1-1,4,7	115 VAC power harness (Timer Number 2)/W101	1A2A8J25
1TB1-11,12	28 VDC power harness/W105	1A2A8J12
1A2A8J6	115 VAC power interconnection harness/W102	1A1A3J4
1A2A8J16	115 VAC power interconnection harness/W102	1A3A3J4
1A2A8J3	28 VDC power interconnection harness/W103	1A1A3J5
1A2A8J19	28 VDC power interconnection harness/W103	1A3A3J5
1A2A8J1	Signal interconnection harness/W-486-24 W104	1A1A3J1
1A2A8J2	Signal interconnection harness/W-486-24 W104	1A3A3J1
1A1A3J6	Cross-Rate blanking (Dual-Rate only)/RG-58/U Connection made at High Rate Timer for Low Rate priority blanking	1A3A3J6

NOTE

Connectors using prefix 1A2A8, refer Figure 2.5, and connectors using prefix 1A1 or 1A3 refer to Figure 2.7.

2.3.9.1. Terminations. Inside the Timer Set Control (TSC) there are four 51-ohm BNC terminators. Typical terminations are:

a. At single-rate stations, the Operate RF inputs and 5-MHz signal inputs have BNC "Tee's" and 51-ohm BNC Terminators.

b. At dual-rate stations, the Operate RF inputs are terminated. Terminations for the 5-MHz signal lines exist only on the last TSC in the 5-MHz signal line. This is the Low Rate Loran-C Timer Set.

2.3.10. Connect the primary AC power cable to the main circuit breaker and energize, install the front panel filler plates, equipment cabinet side panels and door. Connections for UPS 115 VAC may also be made at this time.

CAUTION
Do not insert modules until DC Power Supply adjustments (paragraph 2.5.6) have been completed.

2.4. Installation Drawings. Figures 2.8 - 2.10 show the dimensions of the units of the LTS.

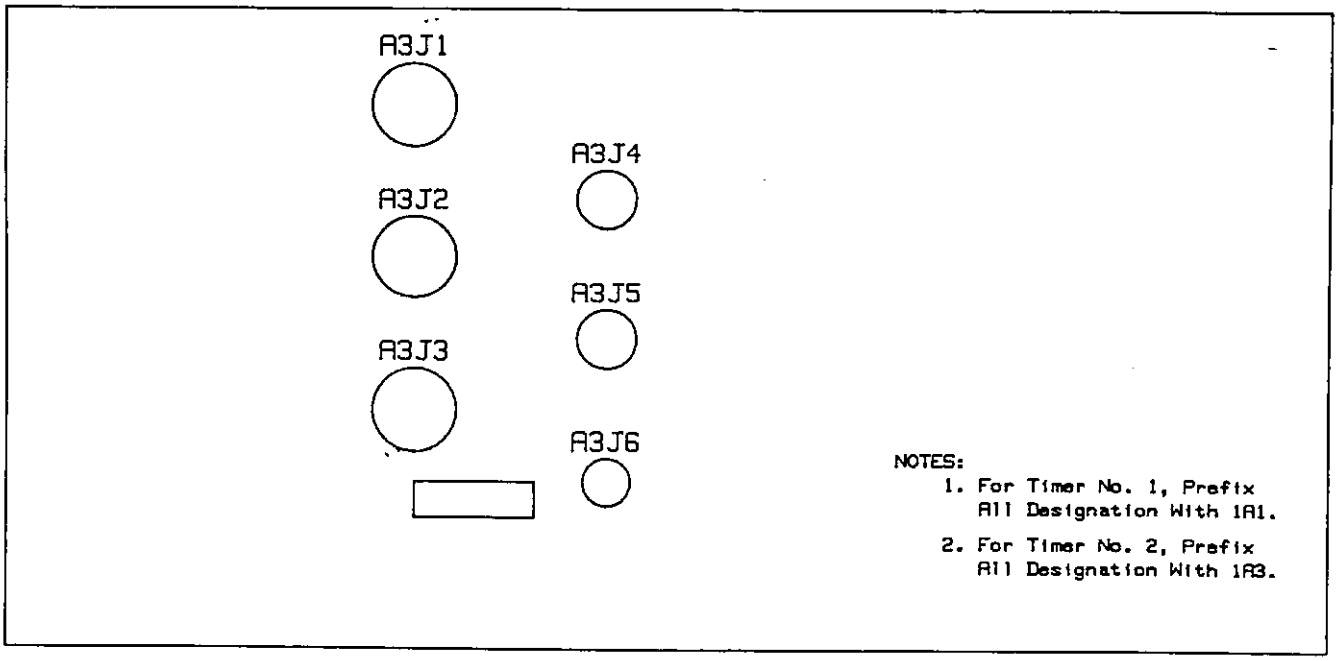


Figure 2.7. Loran Timer (Rear View)

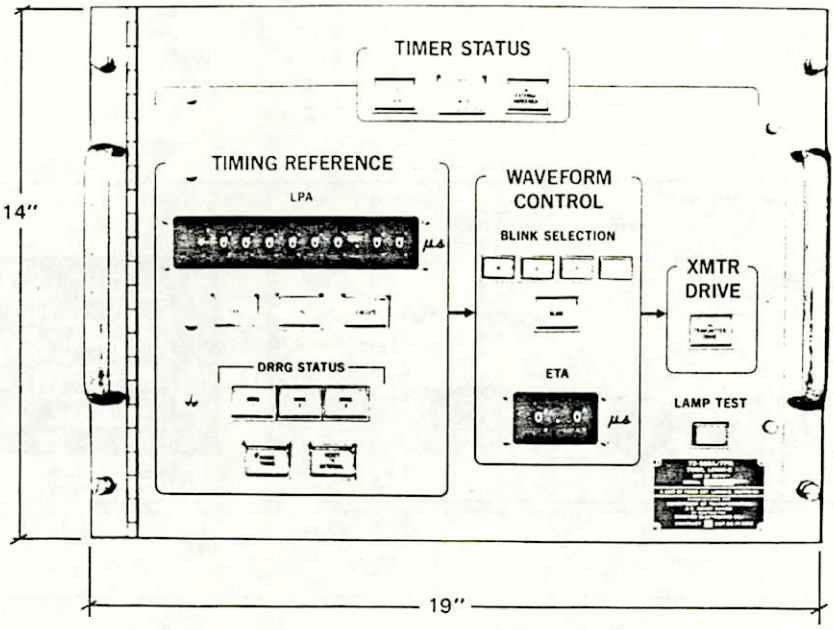


Figure 2.8. Loran Timer (Front View)

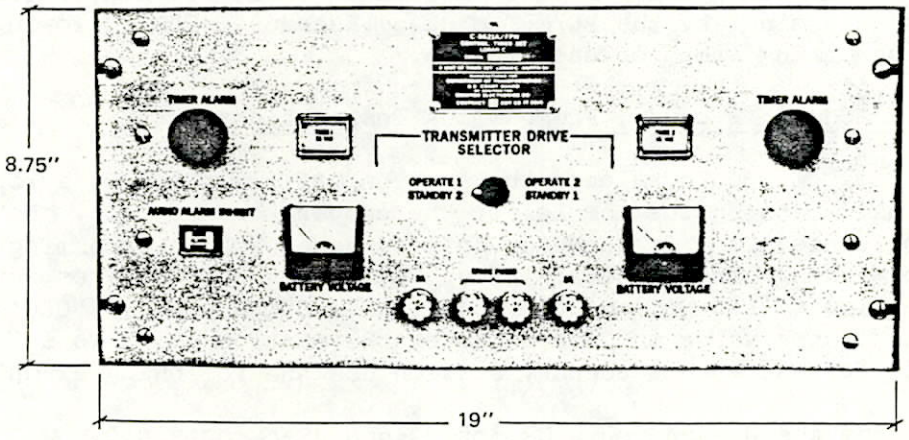


Figure 2.9. Timer Set Control

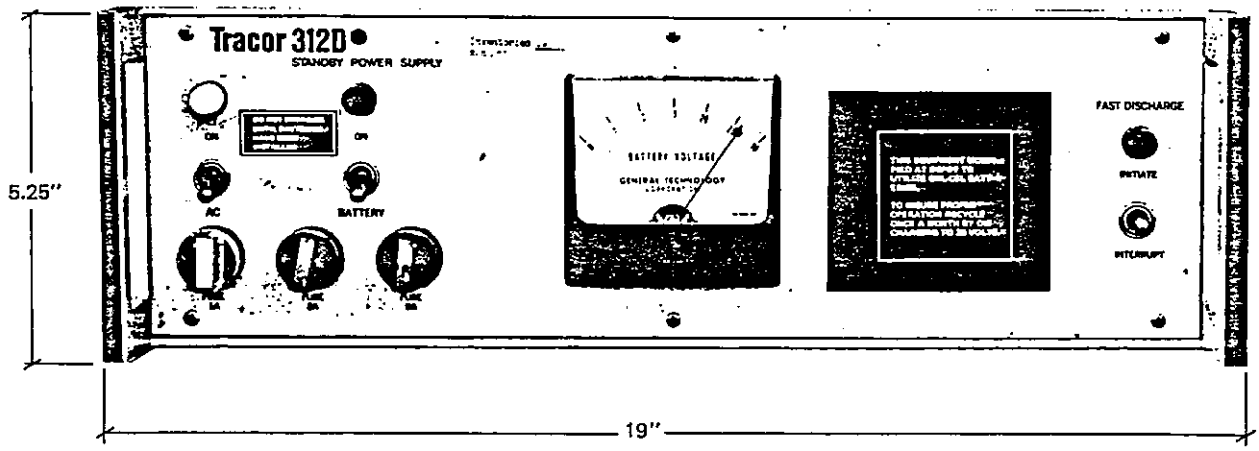


Figure 2.10. Backup Power Supply

2.5. Adjustments and Programming.

2.5.1. The Loran-C Timer Set may operate with different transmitter control configurations. Selected modules in the Loran Timer must be programmed for a specific station configuration. The Group Repetition Interval (GRI) and master or secondary operation is determined by the Program module (H card). ET/MPT or 5 MHz output, delay between EMPT and MPT, and single or dual-rate operation is determined by the DRINT/CP module (T card). The Cycle Compensation (Cycle Comp) time constant is determined by the Error Sense module (M card). Choice of SSX or Tube type transmitter is determined by the PC/MPT module (K card). The following paragraphs discuss the programming steps of each module.

2.5.2. Program Module (H card), Programming Instructions.

2.5.2.1. The Program module selects the station GRI (in uSec) by strapping the required terminal posts on the module for the proper Loran-C rate. No. 20 AWG stranded Teflon coated wire is used for this purpose. GRI programming is accomplished by adding three inputs: (i.e., by adding jumper wires between the appropriate terminals (Pin No.) on the module) 10,000's uSec + 1,000's uSec + 100's uSec, where each input value is determined by the station GRI. To set the Program module (H card) for use at a secondary station use the following example.

a. To program the H card for a GRI of 99,600 uSec, obtain by:

90,000 uSec + 9,000 uSec + 600 uSec = 99,600 uSec.

The Program module must be programmed so that the output to DRRG modules (E, F, and G cards) select the same GRI. Tables 2.4, 2.5, and 2.6 show the connections on the Program module (H card) that provide the required GRI and timing strobe (for the oscilloscope trigger) for DRRG modules E, F, and G respectively. The scope is normally triggered 100 uSec before Loran Interval Time Zero (LORTO). Table 2.7 shows the connections on the Program module (H card) that determine the appropriate blink commands to the Blink module (P card) and Local Interval reset and phase code control to the PC/MPT module (K card). Tables 2.4, 2.5, 2.6, and 2.7 are shown programmed for a GRI of 99,600 uSec as a secondary station.

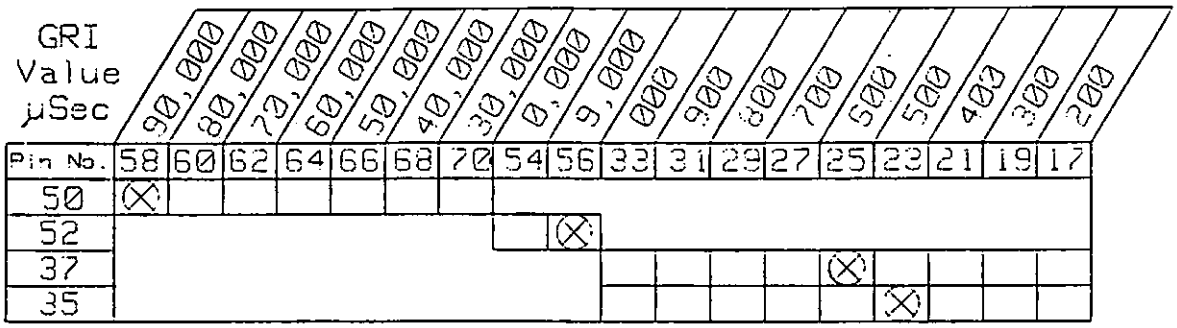
Table 2.4. Program Module (H card) for Output to DRRG Module (E card)

GRI Value µSec	90,300	80,000	70,000	60,300	50,000	40,000	30,000	0,000	9,000	000	900	800	700	600	500	400	300	200
Pin No.	47	49	51	53	55	57	59	61	63	65	67	69	71	73	75	77	79	81
45	X																	
43									X									
41														X				
39															X			

NOTE

Pin 39 is the Scope Trigger output and should be connected to the pin that is 100 uSec less than pin 41. If pin 41 is connected to zero or 200, connect pin 39 to zero or 200 respectively. An X indicates connection to be made between terminal (Pin No.) in vertical column to terminal (Pin No.) in horizontal row.

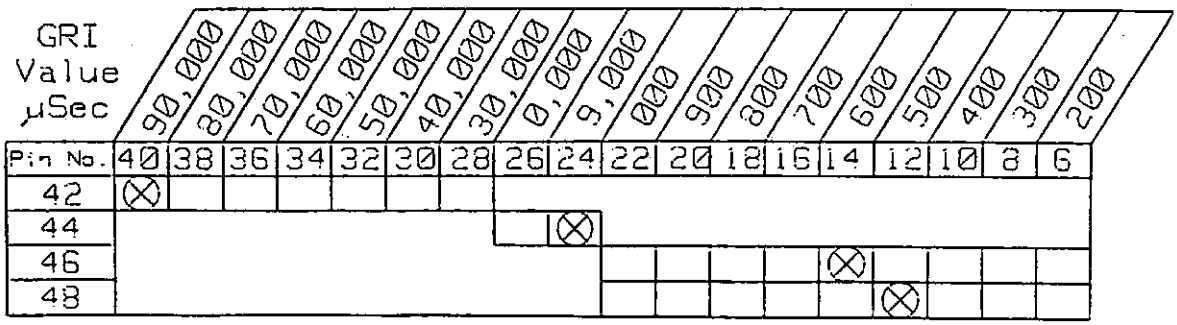
Table 2.5. Program Module (H card) for Output to DRRG Module (F card)



NOTE

Pin 35 is the Scope Trigger output and should be connected to the pin that is 100 usec less than pin 37. If pin 37 is connected to zero or 200, connect pin 35 to zero or 200 respectively.

Table 2.6. Program Modules (H card) for Output to DRRG Module (G card)



NOTE

Pin 48 is the Scope Trigger output and should be connected to the pin that is 100 usec less than Pin 46. If Pin 46 is connected to zero or 200, connect Pin 48 to zero or 200 respectively.

Table 2.7. Program Module (H card)

FUNCTION	Pin No.	1 GND	2 GND	85 GND	86 GND	3 VCC	4 VCC	83 VCC	84 VCC	5 M-BLINK	7 S-BLINK	11 MASTER	13 SECONDARY	72 MASTER	74 SECONDARY
BLINK LAMP	9										⊗				
BLINK SET INPUT	15												⊗		
PHASE CODE CONTROL	78					⊗									
M-BLINK	5	⊗													
S-BLINK	7														
LOCAL INT. RESET	76														⊗

NOTE

For Secondary operation, connect M-BLINK (Pin 5) to GND (Pin 1)

For Master operation, connect S-BLINK (Pin 7) to GND (Pin 1)

For Secondary operation, connect Phase Code Control (Pin 78) to VCC (Pin 3)

For Master operation, connect Phase Code Control (Pin 78) to GND (Pin 2)

2.5.3. DRINT/CP Module (T card), Programming Instructions.

2.5.3.1. DRINT/CP module (T card) must be programmed according to the particular transmitter installed and for single or dual-rate operation. Refer to Figure 7.29 for locations of all jumpers. Table 2.8 lists the connections for a particular station configuration. No. 20 AWG solid bare wire is used and should be soldered to the terminal posts, for programming connections as shown in Table 2.8.

2.5.4. PC/MPT Module (K card), Programming Instructions.

2.5.4.1. Refer to WO486-30/PC/MPT parts locator, Figure 7.32 for the location of thumbwheel switches S1, S2, and S3. Table 2.9 provides the preliminary thumbwheel switch settings for all transmitter types.

2.5.5. Error Sense Module (M card), Programming Instructions.

2.5.5.1. Error Sense module (M card) may be programmed to select various time constants for the Cycle Compensation (Cycle Comp) loop. Normally, the Error Sense module is programmed for the shortest time constant (shortest time constant is fastest operation). This time constant is equal to the number shown in Table 2.10 times the GRI in seconds (9960 = 0.0996 Sec). Table 2.10 shows the programming for the Error Sense module (M card).

3. DRINT/CP Module (T card), Programming Instructions.

2.5.3.1. DRINT/CP module (T card) must be programmed according to the particular transmitter installed and for single or dual rate operation. Refer to Figure 7.( ) for locations of all jumpers. Table 2.8 lists the connections for a particular station configuration. No. 20 AWG solid bare wire is used and should be soldered to the cambion posts, for Programming Connections as shown in Table 2.8.

Table 2.8. DRINT/CP Module (T) Programming

FUNCTION	DESIRED OUTPUT	TRANSMITTER	PROGRAMMING CONNECTIONS
Select ET/EMPT, EMPT, or 5 MHz from Loran Timer	5 MHz	AN/FPN-64(V)	E12 to E14 E13 to E15
	ET/EMPT or EMPT	AN/FPN-39 AN/FPN-42 AN/FPN-44,44A,45	E16 to E17 E18 to E19
Select delay between EMPT and MPT	60 uSec	AN/FPN-64(V)	E3 to E9 E4 to E10
	20 µSec	AN/FPN-39 AN/FPN-42 AN/FPN-44,44A,45 bias pedestal tail biter	E4 to E10
	160 uSec	AN/FPN-44,44A,45 bias pedestal under the pulse	E1 to E7 E2 to E8 E3 to E9 E4 to E10
Select ET/EMPT or EMPT	Single-Rate (ET/EMPT)	AN/FPN-64(V) AN/FPN-39 AN/FPN-42 AN/FPN-44,44A,45	E6 to E11
	Dual-Rate	AN/FPN-64(V)	E6 to E11
	Dual-Rate Low rate: ET/EMPT High rate: EMPT	AN/FPN-39 AN/FPN-42 AN/FPN-44,44A,45	Remove jumper E6 to E11 on High rate (ET present on Low rate only

Table 2.9. PC/MPT Module (K card) Programming

SWITCH	TUBE-TYPE TRANSMITTERS	AN/FPN-64(V)
S-3 (Hundreds)	0	5
S-2 (Tens)	1	1
S-1 (Units)	1	1

Table 2.10. Error Sense Module (M card) Programming

TIME CONSTANT/GRI	PROGRAMMING CONNECTIONS	
120	E8 to E9	E8 to E10
240	E8 to E9	E5 to E10
360	E8 to E9	E6 to E10
480	E5 to E9	E6 to E10
600	E7 to E9	E8 to E10
720	E7 to E9	E5 to E10
840	E7 to E9	E6 to E10

2.5.6. DC Power Supply Adjustments. Ensure the Loran Timer is in the Standby mode. Withdraw the Loran Timer to its fully locked open position. (For initial power supply adjustments remove all modules from the card file.) Remove the top cover, and remove fuses F1 and F2 in the Timer Set Control (1A2). Power Supplies 1A1A4, 1A1A5, 1A1A6 and 1A1A7 should be adjusted while installed in the Loran Timer. Energize the Loran Timer by pressing the Timer ( )115 VAC switch. Refer to Figure 2.11 for location of the power supply modules and chassis terminal boards. The following test equipment is required:

a. Calibrated oscilloscope with a X10 probe

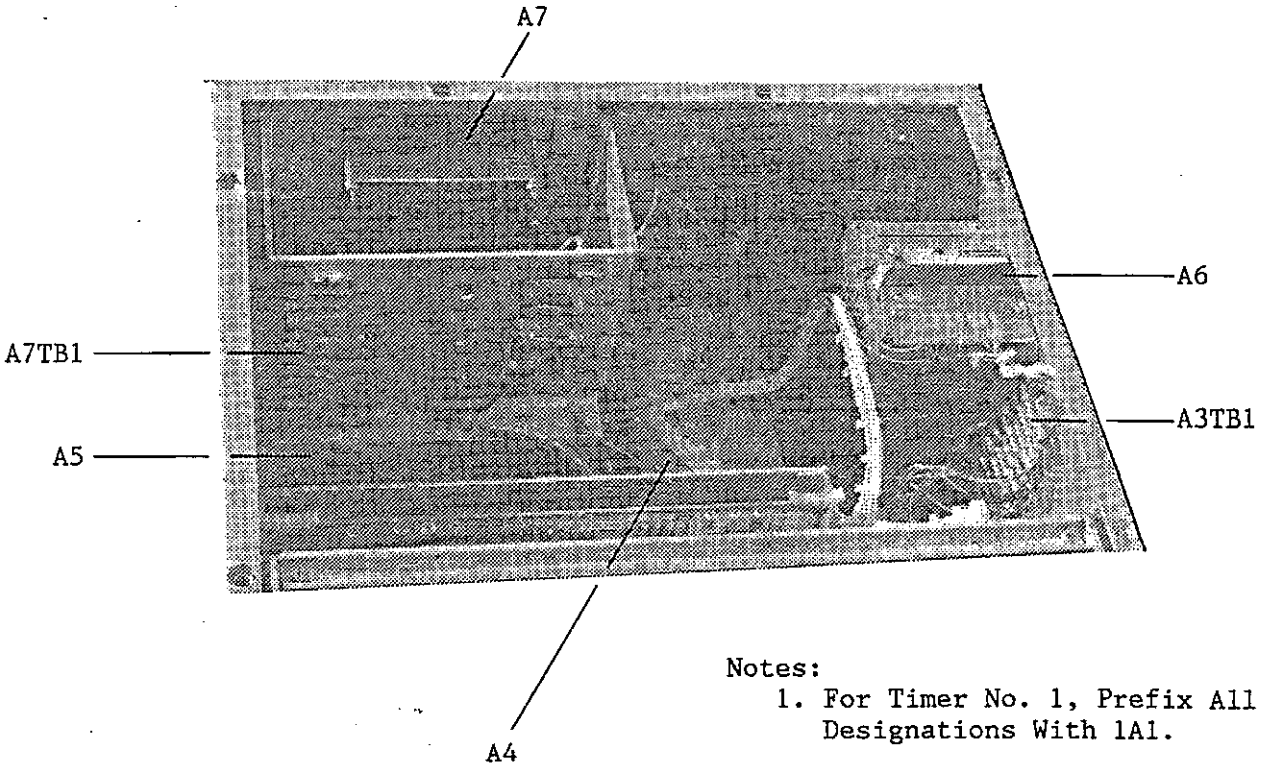
b. Digital Multimeter

CAUTION

Accomplish Power Supply checks and adjustments only when the Loran Timer is in the Standby mode.

NOTE

All Loran Timer power supply voltages are to be checked for ripple and "glitches". The ripple should not exceed 1.0 mV p-p. Put the scope probes on same terminals used to measure voltages. Do NOT measure voltage and ripple at the same time as some Digital Voltmeters can introduce noise.



Notes:

1. For Timer No. 1, Prefix All Designations With 1A1.
2. For Timer No. 2, Prefix All Designations With 1A3.

Figure 2.11. Power Supply Locations in the Loran Timer

2.5.6.1. 1A1A4 +5 VDC Power Supply Adjustment. Set the meter range to 10 VDC. Connect the negative lead of the multimeter to 1A1A3TB1-3, the positive lead to 1A1A3TB1-1. If necessary, adjust the voltage control (VA) on the rear apron of the Loran Timer chassis until the meter indicates 5.0 VDC $\pm$0.1 VDC.

NOTE

Power Supply 1A1A4 current limit adjustment is factory set and should not be adjusted.

2.5.6.2. 1A1A5 +28 VDC Power Supply Adjustment. Set the meter range to 50 VDC. Connect the negative lead of the multimeter to 1A1A7TB1-8, connect the positive lead of the meter to 1A1A7TB1-9. If necessary, adjust the Voltage Adjust control on the top front left corner of the power supply 1A1A5 to obtain 28.0 VDC.

2.5.6.3. 1A1A6 ±15 VDC Power Supply Adjustment. The 1A1A6 power supply is a dual output, ±15V supply. This power supply has an overvoltage protection circuit (LC-OV-11) that is set for 35.5 VDC or approximately 18.3% over power supply output, and must be set before adjusting the power supply output. Use the following procedure to adjust the Over-Voltage Protection circuit and the power supply output:

a. Set the voltmeter range to 50 VDC. Connect the negative lead to 1A1A3TB1-5, and the positive lead to 1A1A3TB1-9.

b. Adjust the voltage control (marked VDC ADJ) on the left side of the power supply 1A1A6 to obtain 35.5 VDC.

c. Slowly adjust the Over-Voltage Protector (LC-OV-11) until there is an abrupt drop in the output voltage. The over-voltage protection circuit is now set. DO NOT adjust the over-voltage protector beyond this point.

d. De-energize the Loran Timer primary power so the Over-Voltage Protection circuit will reset. Before re-applying power, decrease (turn CCW) the VDC ADJ Control on the left side of the power supply several turns.

e. Energize the Loran Timer and adjust the VDC ADJ Control so the output of the 1A1A6 power supply is +30.0 VDC ±0.1 VDC.

f. Check the voltage between ground and 1A1TB1-5 (should be -15 V ±1 V) and between ground and 1A1TB1-9 (should be +15 V ±1 V).

2.5.6.4. 1A1A7 +5 VDC Power Supply Adjustment.

NOTE

The 1A1A5 Power Supply must be adjusted before the 1A1A7 Power Supply is adjusted.

a. Set the meter range to 10 VDC. Connect the negative lead of the multimeter to 1A1A7TB1-8, connect the positive lead to 1A1A7TB1-2.

b. If necessary, adjust the 1A1A7 power supply Output Voltage control to obtain +5.0 VDC, ±0.1 VDC.

2.5.6.5. Module Installation. Once all required modules are programmed properly and all power supply adjustments have been made, remove power from the Loran Timer and install all printed circuit modules so that the colored extractor handles are at the top (component side to the right), and matched to the color stripes on the rail of the module file. Slide each module into its guide, and firmly press into place using thumb pressure at the top and bottom of the module.

2.5.6.6. After all modules have been installed, energize the Loran Timer and recheck power supply adjustments (refer to paragraph 2.5.6).

2.5.6.7. Disconnect the meter leads, replace the top cover, and release the lock mechanism to slide the Loran Timer into the cabinet. Power supplies 1A3A4, 1A3A5, 1A3A6, and 1A3A7 located in 1A3 Loran Timer Number 2 may be adjusted using the procedures discussed in paragraph 2.5.6.

2.6. Initial Operation. Initial operational check is to be performed after all connections to external equipments have been made (see Figure 1.6).

2.6.1. Equipment Turn-On. Perform the following steps to energize the Loran-C Timer Set:

a. Press the TIMER 1 115 VAC and TIMER 2 115 VAC indicator/switches on the Timer Set Control so that the lamps illuminate.

b. Ensure that fuses F1 and F2 are in the Timer Set Control.

c. Press the LOCAL/REMOTE indicator/switch on both Loran Timers so that both lamps indicate the same mode of operation (LOCAL or REMOTE).

d. Press the CHECK TIMING indicator/switch on both Loran Timers.

e. Press the RESET TO EXTERNAL switch on either Loran Timer. It may be necessary to press the RESET TO EXTERNAL switch several times for all lights to extinguish.

f. All red lights should now be out and the Loran-C Timer Set is ready for operation.

2.6.2. Equipment Turn-Off. The following steps are necessary for de-energizing the Loran-C Timer Set:

a. Remove fuses F1 and F2 from the Timer Set Control.

b. Press the TIMER 1 115 VAC and TIMER 2 115 VAC indicator/switches on the Timer Set Control so that the lamps are extinguished.

c. If applicable, disconnect the UPS 115 VAC.

2.6.3. Equipment Operation Check. Perform the following steps to initially check the Loran Timer for proper operation. Refer to Figure 2.12 for location of all switches and indicators.

2.6.3.1. Lamp Test. Depress and hold the LAMP TEST switch for a few seconds. All front panel lamps on the Loran Timer should light (except as noted below), and the Audio Alarm should sound (if not inhibited). Illumination of the REMOTE/LOCAL and OPERATE/STANDBY lamps will depend upon the mode of operation. BLINK lamps W, X, Y and Z will not light in either the OPERATE or STANDBY mode when the LAMP TEST switch is depressed.

2.6.3.2. LPA Entry into Timer Number 1. Set Loran Timer No. 1 for LOCAL operation. Use the thumbwheel switches on the front of Loran Timer No. 1 and select an LPA equal to 1 GRI. Momentarily depress the LOAD indicator/switch. The LOAD lamp should light and the CLEAR lamp should extinguish. Momentarily depress the EXECUTE indicator/switch. The EXECUTE lamp should remain on until the Loran Timer executes the LPA. When the Loran Timer completes execution, the EXECUTE lamp will extinguish and the CLEAR lamp should light. The NO EXTERNAL AGREEMENT lamp should be lit on Loran Timers No. 1 and No. 2, and if not inhibited, the audio alarm should be heard.

2.6.3.3. LPA Entry into Timer Number 2. Set Loran Timer No. 2 for LOCAL operation. Select the same value LPA used in the previous step for Timer Number 2. Momentarily depress the LOAD and then the EXECUTE indicator/switches. When Timer Number 2 has entered the LPA, the NO EXTERNAL AGREEMENT lamp should extinguish on Loran Timers No. 1 and No. 2 and the audio alarm will terminate.

2.6.3.4. Blink Test. Set the Loran Timer for LOCAL operation. Begin blink by depressing the W indicator/switch on the Loran Timer. The W lamp will light and the BLINK lamp will flash according to the Loran Timer configuration. If the Loran Timer is configured as a Master, the BLINK lamp will flash the blink code for W. (Due to factors in design, the blink indicator will not indicate the first "short" flash for the blink code, but will indicate all other parts of the blink code). If the Loran Timer is configured as a Secondary, the BLINK lamp will flash on and off in the pattern for Secondary Blink. Stop blink by depressing the W indicator/switch; the W lamp and the BLINK lamp should extinguish. Perform the same procedure for starting and stopping blink on X, Y, and Z, one at a time.

2.6.3.5. Check Timing. Remove fuse F1, and depress the TIMER 1 115 VAC switch. Replace F1 and depress the TIMER 1 115 VAC switch. This will cause the DRRG modules to be out of agreement. The CHECK TIMING lamp should light. Depress the CHECK TIMING indicator/switch and the light should extinguish. Depress the RESET TO EXTERNAL indicator/switch to clear Timer alarms.

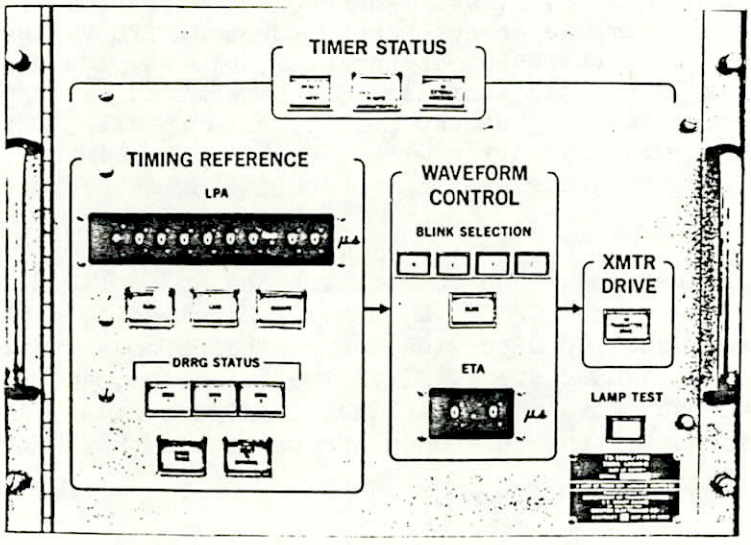


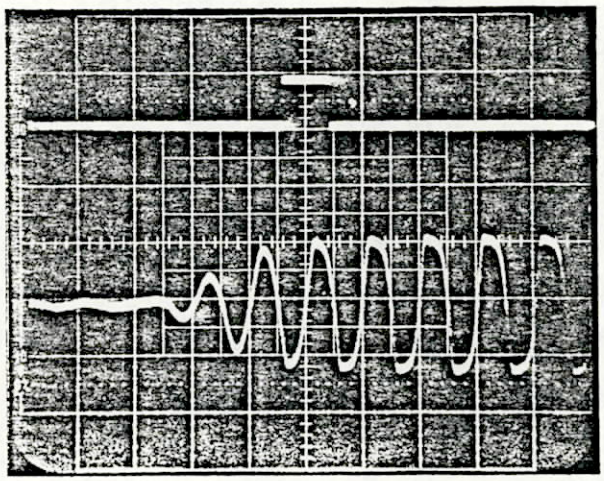
Figure 2.12. Loran-C Timer

2.7. Cycle Compensation Loop Jump Point. This adjustment procedure is performed as the first "ON-AIR" alignment for the Operate Loran Timer. This alignment will compensate for the local path delays (difference between the time the appropriate signals leave the Loran Timer and the time the "OPERATE RF" from the transmitter is sampled by the Cycle Comp) which will vary from station to station. Since the local path delay is a sum of transmission line delays, station layout, transmitter delays, and transmitter type, it is very important that all transmitters and associated equipment be completely installed before this adjustment is made. Since the Loran-C Timer Set was originally developed, several major changes have been incorporated in the system which have caused the Cycle Comp alignment to become a more critical adjustment. The most extensive change was the introduction of the WO486-28B/DRINT/CP module (T card). This module permits the transmitted Loran-C signal to be modulated (pulse position modulation on any or all Loran-C pulses) with communications information.

At some installations, communications modulation is introduced into the signal by phase shifting (advancing or delaying) the Cycle Comp 100 kHz, which in turn shifts the multipulse triggers (MPT). The Cycle Comp loop jump point can be exceeded, resulting in "10 uSec jumps" in the transmitted signal, on a regular basis if communications modulation is present and the input trigger to the reclock circuit is near the reclock edge of the reclock waveform. If the quiescent point of the Cycle Comp loop is properly calibrated, then the input trigger (MPT8 from the WO486-30/PC/MPT module) will reside as far as possible from any reclock edge of the Cycle Comp 100 kHz. Since reclock edges occur every 10 uSec, the input trigger should be centered in this "10 uSec reclock window". Exact centering will allow modulation of $\pm$5 uSec before a jump point is reached. Realistically, due to the precision with which the jump point can be calibrated and due to normal Cycle Comp loop activity a modulation limit of about $\pm$3.5 uSec should be imposed.

2.7.1. Procedures for Setting Cycle Comp Jump Point. This procedure is divided into two steps. Step 1 is the "Coarse" adjustment and step 2 is the "Fine" adjustment. The coarse adjustment will determine which zero crossing of OPERATE RF will be sampled by the Cycle Comp loop. The fine adjustment will center the "10 uSec Reclock Window" on the coarse MPT (CMPT). This is accomplished by changing the start time (pin 10 of DRRG E, F, and G cards) and stop time (pin 8 of DRRG E, F, and G cards) of the Cycle Comp Reference Strobe (M card, TP5 yellow) in 1 uSec increments, by selecting the DRRG outputs available at pins 81, 65, 67, 69, 68, 77, 75, 73, 79, and 71. Since the start/stop is determined by majority gating of these selected outputs, the same adjustment must be made to all 3 DRRG modules. The actual adjustment is made by moving wires (changing taps) on the backplane of the card file and is made only during a new installation or replacement of a Loran Timer.

2.7.1.1. Coarse Adjustment. Use an oscilloscope as outlined in Figure 2.13. Adjust S1, S2 and S3 on the PC/MPT (K card) as required to center the Reference Select Gate (approximately 8 uSec wide) on the third positive zero crossover. S1 will move the gate in 1 uSec steps, S2 in 10 uSec steps, and S3 in 100 uSec steps. Connect and set an oscilloscope as outlined in Figure 2.14. Adjust S1 and S2 on the PC/MPT (K card) to center the Reference Strobe within the Reference Select Gate as shown in the figure.



SIGNAL AND SOURCE	SETTINGS
	TRIGGER
Channel A: TP4 (Blue) ERROR SENSE module (M) Reference Select Gate	(-) External
Channel B: TP2 (Orange) ERROR SENSE module (M) Limited Operate RF	MODE Delayed Sweep
Trigger: TP7 (RED) any DRRG module (E,F,G) Channel A & B, ALT	HORIZONTAL: 10 uSec/Div Main Sweep 0.5 mSec/Div
X10 Scope Probes	VERTICAL: 5 V/Div

Figure 2.13. Coarse Positioning of the Reference Strobe

2.7.1.2. Fine Adjustment. To determine the amount and direction to program the "taps" on the DRRG module's backplane, view the Reclock Pulse Width signal on the DRINT/CP module (T card) at TP4 (gray). Trigger the oscilloscope on (-) Internal, set the vertical to 1V/Div or 2V/Div and the horizontal to 1 uSec/Div. If the Reclock Pulse Width is not low for 5 uSec, $\pm$.5 uSec, then fine adjustment will be required. Note the width of the waveform, and refer to Table 2.11 to determine the amount and direction of adjustment that is required (e.g., if the reclock pulse width is 2.0 uSec, Table 2.11 would require that the reference strobe start/stop time occur 3 uSec later). Once you have determined the amount and direction of required adjustment, refer to Table 2.12 to determine the proper tap settings. To use Table 2.12, you must first determine to what taps pins 10 and 8 (DRRG module) are connected by checking the backplane wiring. Locate these settings in the "Present tap setting" column. Locate the correct tap settings along the same line in the column under the required adjustment. In the example above, the Reclock Pulse Width was 2.0 uSec. Table 2.11 listed a "3 uSec later" adjustment. If the Loran Timer under test has a preset tap setting of pin 10 connected to pin 68 and pin 8 connected to pin 73, then the correct tap settings (as listed along the same line, under the "3 uSec later" column) require connection of pin 10 to pin 73 and pin 8 to pin 81. This will effect a change of "3 uSec later". Once the taps have been changed on all 3 DRRG modules, recheck the coarse adjustment as outlined in Figure 2.13 and Figure 2.14. Small adjustments of S1 might be required to achieve the waveforms shown. Make the adjustments required and then recheck the Reclock Pulse Width as outlined above and make the corrections as required. Repeat the

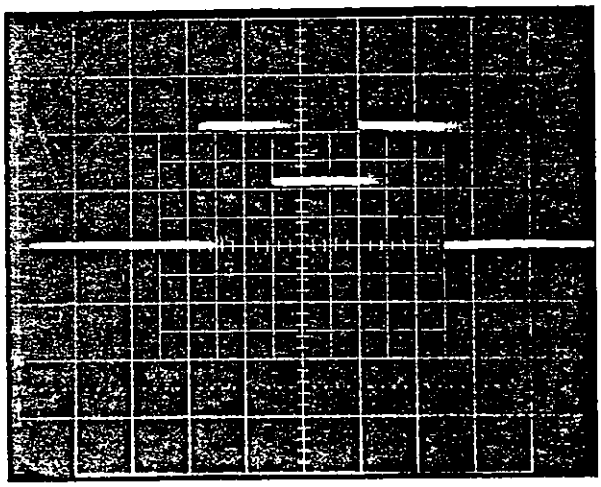
Table 2.11. Reclock Pulse Width Adjustment
(See paragraph 2.7.1.2)

DRINT TP4 (LOW) WIDTH IN uSEC	0.0 to 0.5	0.5 to 1.5	1.5 to 2.5	2.5 to 3.5	3.5 to 4.5	4.5 to 5.5	5.5 to 6.5	6.5 to 7.5	7.5 to 8.5	8.5 to 9.5	9.5 or Greater
AMOUNT ADJUST REQUIRED	5 uSec Later	4 uSec Later	3 uSec Later	2 usec Later	1 uSec Later	No Adjust Req'd.	1 uSec Earlier	2 uSec Earlier	3 uSec Earlier	4 uSec Earlier	5 uSec Earlier

Table 2.12. Tap Setting Adjustment
(See Paragraph 2.7.1.2)

PRESENT TAP SETTINGS			TAP SETTINGS FOR REQUIRED AMOUNT OF ADJUSTMENT																	
			1 uSec LATER		2 uSec LATER		3 uSec LATER		4 uSec LATER		5 uSec LATER		5 uSec EARLIER		4 uSec EARLIER		3 uSec EARLIER		2 uSec EARLIER		1 uSec EARLIER	
10	8		10	8	10	8	10	8	10	8	10	8	10	8	10	8	10	8	10	8	10	8
81	69		65	68	67	77	69	75	68	73	77	79	77	79	75	71	73	81	79	65	71	67
65	68		67	77	69	75	68	73	77	79	75	71	75	71	73	81	79	65	71	67	81	69
67	77		69	75	68	73	77	79	75	71	73	81	73	81	79	65	71	67	81	69	65	68
69	75		68	73	77	79	75	71	73	81	79	65	79	65	71	67	81	69	65	68	67	77
68	73		77	79	75	71	73	81	79	65	71	67	71	67	81	69	65	68	67	77	69	75
77	79		75	71	73	81	79	65	71	67	81	69	81	69	65	68	67	77	69	75	68	73
75	71		73	81	79	65	71	67	81	69	65	68	65	68	67	77	69	75	68	73	77	79
73	81		79	65	71	67	81	69	65	68	67	77	67	77	69	75	68	73	77	79	75	71
79	65		71	67	81	69	65	68	67	77	69	75	69	75	68	73	77	79	75	71	73	81
71	67		81	69	65	68	67	77	69	75	68	73	68	73	77	79	75	71	73	81	79	65

NOTE: Numbers represent pin numbers for DRRG (E, F, G) connector pins.
Pins 10 and 8 represent start/stop connections.

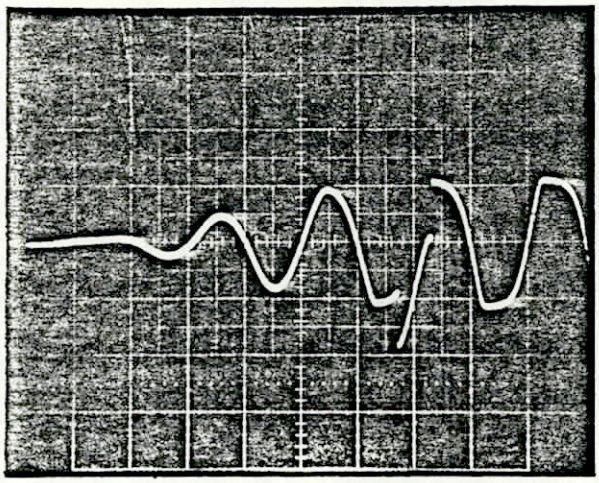


SIGNAL AND SOURCE	SETTINGS
	TRIGGER
Channel A: TP5 (Yellow) ERROR SENSE module (M) Reference Strobe	(-) External
Channel B: TP4 (Blue) ERROR SENSE module (M) Reference Select Gate	MODE Delayed Sweep
Trigger: TP7 (RED) any DRRG module (E,F,G) Vertical Mode: A&B ADDED	HORIZONTAL: 2 uSec/Div Main Sweep 0.5 mSec/Div
X10 Scope Probes	VERTICAL: 2 V/Div

Figure 2.14. Fine Positioning of the Reference Strobe

Coarse and Fine adjustment procedures until the Reclock Pulse Width is 5 uSec, $\pm$.5 uSec. As a final check to insure that the Reference Strobe has settled on the third positive zero crossover point, use an oscilloscope as outlined in Figure 2.15 after the Cycle Comp has settled, and insure that it is sampling on the third positive zero crossover. When the above procedure is followed with either Loran Timer and either transmitter, the station's Cycle Comp Jump Point has been properly calibrated. The second Loran Timer backplane can simply be wired to agree with the tap settings in the first Loran Timer. Check the coarse adjustment as outlined in Figure 2.13, and the fine adjustment as outlined in paragraph 2.7.1.2 to insure that all conditions are met. A transmitter switch will not materially change the Cycle Comp Jump Point. If both transmitters are equally "healthy", the Reclock Pulse Width on the DRINT/CP module should change less than 100 nSec with a transmitter switch.

Future changes in the adjustment of the Cycle Comp Jump Point will be necessary only if major changes are made in the station configuration (e.g., change transmitter type, relocate signal power building, reroute transmission lines, etc.). The coarse calibration procedure (Figure 2.13) must always be carried out, however, whenever an ERR SNS module or PC/MPT module is replaced.



SIGNAL AND SOURCE	SETTINGS
	TRIGGER
Channel A: TP5 (Yellow) ERROR SENSE Module (M) Reference Strobe	(-) External
Channel B: TP2 (Orange) ERROR SENSE module (M) Limited Operate RF	MODE Delayed Sweep
Trigger: TP7 (RED) any DRRG module (E,F,G)	HORIZONTAL: 5 uSec/Div (Main Sweep 0.5 mSec/Div
Channel A & B, ADDED	VERTICAL: 2 V/Div

Figure 2.15. Reference Strobe Sampling Point

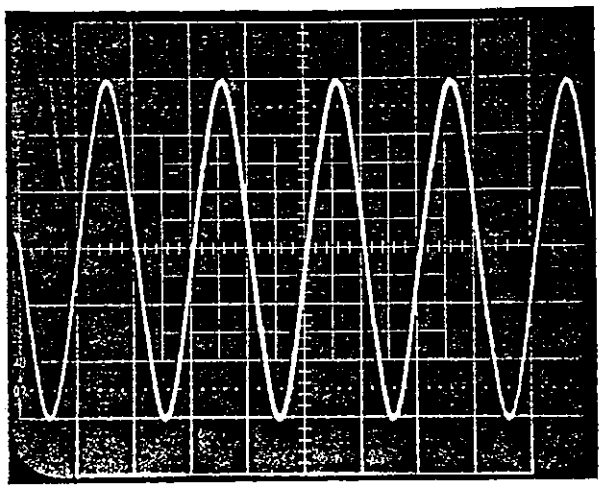
NOTE

Performing the Fine Cycle Comp Jump Point adjustment will have the same effect on timing as inserting an LPA (i.e., selecting DRRG taps to make a "1 uSec later" change will shift the Loran Timer reference the same as inserting a +1 uSec LPA). When this occurs, insert an LPA of the appropriate magnitude and direction to compensate for the change.

2.8. 100 kHz Output Signal Adjustment. Use an oscilloscope as outlined in Figure 2.16. Adjust potentiometer, R6, on the Interface module (R card) to obtain a 12 Vpp waveform.

NOTE

At tube transmitter stations, if all other gain adjustments for the transmitted Loran signal are at maximum, and higher radiated power is required, the observed waveform may be adjusted to levels higher than 12 Vpp in accordance with station drawings. However, higher levels will cause changes in the transmitting equipment jump points.



SIGNAL AND SOURCE	SETTINGS
	TRIGGER
Channel A: TP1 (Red) INTERFACE module (R) 100 kHz	(-) Internal
Ground reference is 0.4 divisions below center	MODE MAIN
Nominal level is 12 Vpp	HORIZONTAL: 5 uSec/Div
	VERTICAL: 2 V/Div

Figure 2.16. 100 kHz Output Signal Adjustment

2.9. LTS Input/Output Signals. Table 2.13 lists the input signals to, and Table 2.14 lists the output signals from, the Loran-C Timer Sets.

2.10. De-installation and Shipping.

2.10.1. The following procedure should be followed when replacing LTS units:

a. Order a replacement unit.

b. When replacement unit arrives, disconnect cables from defective unit and remove it from the cabinet.

c. Install new unit and connect cables.

d. Pack defective unit in same shipping container and return as specified in original shipping documentation.

Table 2.13. LTS Signal Input List for AN/FPN-54A and AN/FPN-65 Loran-C Timer Sets

	EQUIPMENT	JACK OR TERMINAL	SIGNAL
INPUTS TO LTS	LORAN TIMER 1A1	J2 J3 J6	Loran-C Communications Signals Remote Control Signals Cross-Rate Blanking
	LORAN TIMER 1A3	J2 J3 J6	Loran-C Communications Signals Remote Control Signals Cross-Rate Blanking
	TIMER SET CONTROL 1A2	J14 J26 J27	Operate RF 5 MHz (From Operate Frequency Standard) 5 MHz (From Standby Frequency Standard)

Table 2.14. LTS Signal Output List for AN/FPN-54A and AN/FPN-65 Loran-C Timer Sets

	EQUIPMENT	JACK OR TERMINAL	SIGNAL
	TIMER 1A1	J2 J3	Loran-C Communications Synchronizing Signals Remote Indications
	TIMER 1A3	J2 J3	Loran-C Communications Synchronizing Signals Remote Indications
OUTPUTS OF LTS	TIMER SET CONTROL 1A2	J7 J8 J9 J10 J11 J13 J20 J21 J22 J23 J24 J30 J31 J7 J24 J33 J32	* Early Triggers and Early MPT (OPERATE) Phase Code Reset (OPERATE) Phase Code Set (OPERATE) MPT (OPERATE) *** 100 kHz (OPERATE) Phase Code Interval 100 kHz (STANDBY) MPT (STANDBY) Phase Code Set (STANDBY) Phase Code Reset (STANDBY) * Early Triggers and Early MPT (STANDBY) Local Interval (STANDBY) Local Interval (OPERATE) ** 5 MHz (OPERATE) ** 5 MHz (STANDBY) Cycle Compensation Loop Recorder Drive 1 MHz to Timing Receiver

* Outputs of AN/FPN-54A LTS only.
** Outputs of AN/FPN-65 LTS only.
*** Not used with SSX, but still present at J11.

2. INSTALLATION.

2.1. Introduction. This chapter provides procedures for unpacking and inspecting the Loran-C Timer Set. It describes procedures for installing, programming, adjusting, and initially operating each unit of the LTS. Procedures for the de-installation and shipment of the equipment are also included in this chapter.

2.2. Unpacking and Initial Inspection.

2.2.1. Inspect the shipping containers for external damage. If the containers are damaged, have the carrier's agent present when the containers are unpacked.

2.2.2. After unpacking the containers, inspect the chassis, modules, and cables for physical damage. Inspect all electrical wiring and connections to ensure that connections have not been damaged. Inspect for damage and note any scratches, dents, broken wires, or indicator/switches on the units.

2.3. Installation Instructions.

2.3.1. Materials. Table 2.1 lists the materials that are supplied, and Table 2.2 lists the materials that are required but not supplied for installing the LTS units.

2.3.2. General Installation Procedures.

2.3.2.1. Consider the following specifications before connecting the cables to the units in the LTS:

a. Cables that connect primary AC power, DC back-up power, timer room ground, and other required signals to the electrical equipment cabinet, may be routed through the bottom of the cabinet. The bottom opening is rectangular, and is designed to be placed over the signal building trenching. Stations that do not have signal trenches or computer deck must run cables in overhead ducting.

b. The primary 115 VAC power cable connecting the main circuit breaker panel to the terminal board in the electrical equipment cabinet shall have a minimum conductor size of AWG 14. Also, the primary power circuit breaker shall have a rating of 10 amperes.

WARNING

Before connecting the primary AC power cable to the main circuit breaker panel, place (and properly tag) the circuit breaker to its OFF position.

Table 2.1. Materials Supplied

Quantity per Equipment	Nomenclature		Dimensions		
	Name	Designation	Length	Width	Depth
32	Mounting Screws	10-32	1.0 in		
32	Captive Nuts	10-32			
2	Interconnect Timer Signal Harness	W0486-24-W104	43.0 in		
2	115 VAC Power Harness	W101	66.0 in		
2	115 VAC Inter-connect Power Harness	W102	43.0 in		
1	28 VDC Power Harness	W105	66.0 in		
2	28 VDC Inter-Connect Power Harness	W103	43.0 in		
4	Chassis Slide Mechanism				

Table 2.2. Materials Required but not Supplied

Quantity per Equipment	Nomenclature		Required Use and Characteristics
	Name	Designation	
1	Coaxial Cable	RG-58/U	Cross rate blanking for dual-rated stations. BNC connectors and Coaxial Tee required.
1	AC Power Cable	IAW local codes	Primary AC Power from external circuit breaker to terminal board 1TB1.
1	RF Feedback Cable	RG/22B/U	Operate RF Feedback.

2.3.2.2. Specific cable runs are classified by noise susceptibility. Red cable markers denote primary power AC, uninterruptible power (UPS) AC and, TTY current loops. Yellow cable markers denote frequency distribution cables (5 MHz, 1 MHz, and 100 kHz), high level phasing signals, PCI, and TCS or LSM drive signals. White cable markers denote low level RF, TTL logic levels (0-5 VDC), and analog signals. In order to minimize capacitive and inductive cross talk, observe the following procedures:

a. Avoid parallel runs of different cable classes between racks and entrance panels.

b. When parallel runs of different classes of cables cannot be avoided, separate the cable classes by at least four feet. This separation applies even if cable runs are made using "Square-D" type metallic ducting.

c. When cables of different classes must intersect, they should intersect at right angles.

d. When cable runs must be installed overhead at pre-existing Loran stations which do not have computer flooring, avoid making "yellow" or "white" cable runs parallel to AC power wiring for fluorescent lights.

e. Some cable shields should be trimmed at one end and not connected. They should be connected to chassis ground at the other end to avoid ground loops. Refer to the Floor and Grounding Plan and Wire Running List for more information.

2.3.3. Electrical Equipment Cabinet.

2.3.3.1. The location of the AN/FPN-54A LTS equipment cabinet is to the left of the AN/FPN-60 Transmitter Control Set (TCS) equipment cabinet, as viewed from the front. For dual-rated stations, both LTS equipment cabinets are placed to the left of the TCS equipment cabinet. Specific locations of the individual units within the LTS are as shown in Figure 2.1.

2.3.3.2. The location of the AN/FPN-65 LTS equipment cabinet is to the left of the AN/FSN-3 Local Status Monitor (LSM) equipment cabinet, as viewed from the front. For dual-rated stations, both LTS equipment cabinets are placed to the left of the LSM equipment cabinet. Specific locations of the individual units within the LTS are shown in Figure 2.1.

WARNING

Ensure that the circuit breaker designated for this rack is OFF and properly tagged.

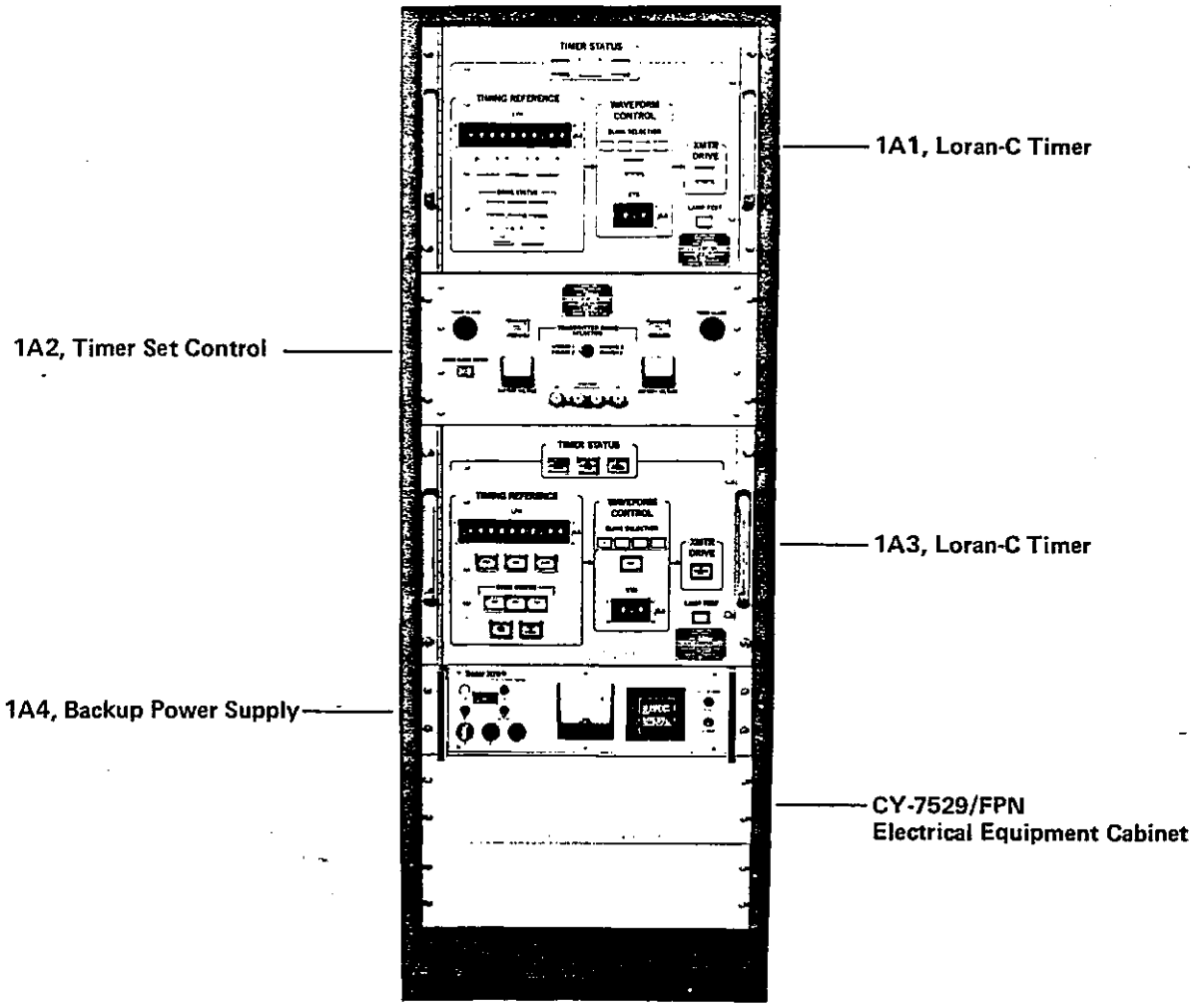
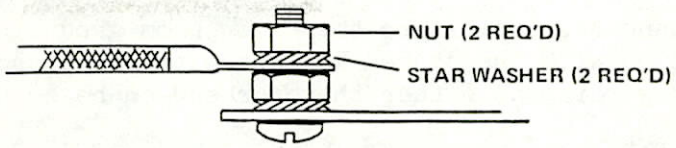


Figure 2.1. Loran-C Timer Set (Front View)



REMOVE PAINT FROM CABINET TO INSURE GOOD ELECTRICAL BOND

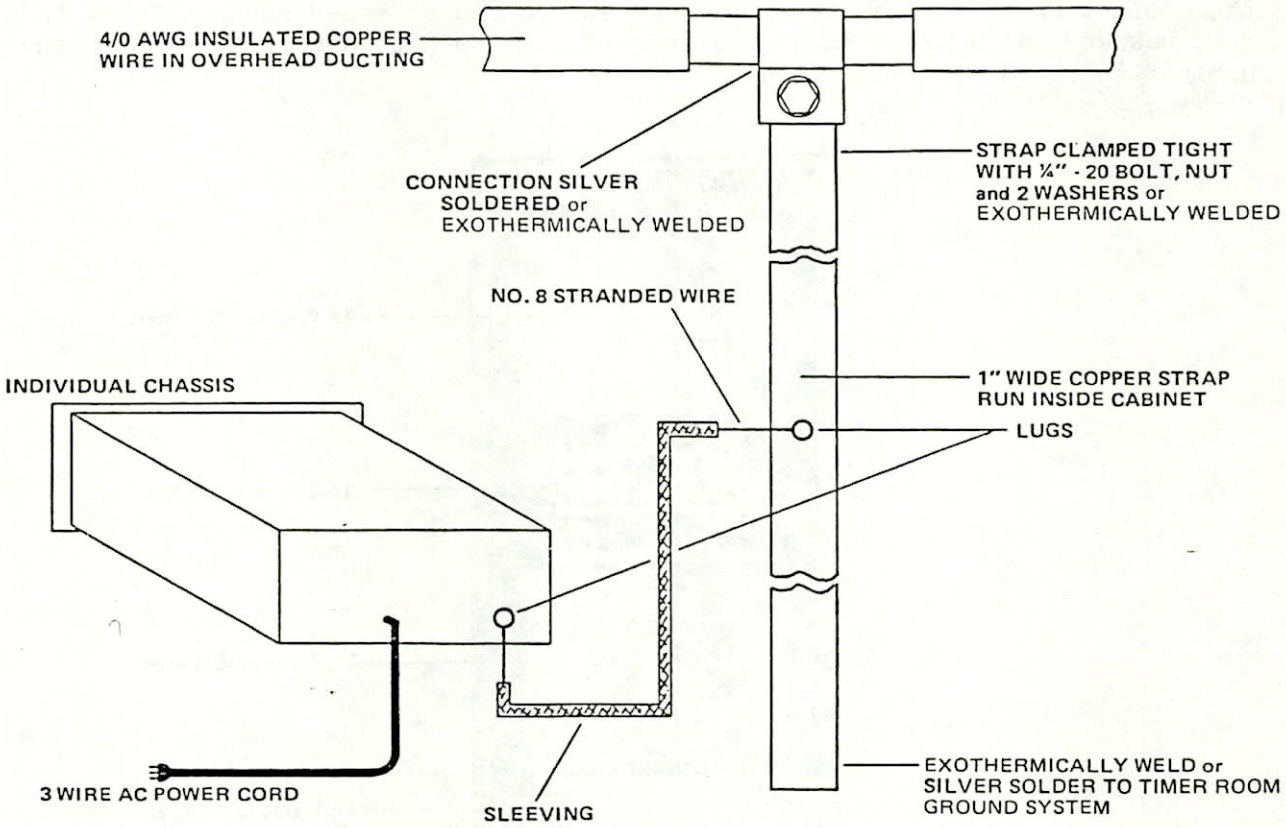


Figure 2.2. Typical Chassis and Cabinet Grounding Details

CAUTION
The Electrical Equipment Cabinet is on a separate circuit breaker, located inside the timer room. DO NOT energize the cabinet, until after the installation of all units. All units are energized upon the application of power.

2.3.3.3. Ground the cabinet to the timer room grounding system (see Figure 2.2). Local connection with the system is made with silver solder and pigtail connections or exothermic welding at either the overhead or below floor ducting.

2.3.4. Isolation Transformer.

2.3.4.1. Install the Isolation Transformer with the primary winding (3 terminals) on the left side of the equipment cabinet, and the secondary winding (4 terminals) on the right side as viewed from the rear (Figure 2.3). The transformer has four threaded studs on the bottom. Insert these studs through four holes in the bottom and to the rear of the equipment cabinet. While supporting the transformer, tilt the cabinet front to back permitting access to the threaded studs. Then, install lock washers and nuts on each stud, tightening the nuts securely. Return the cabinet to the upright position.

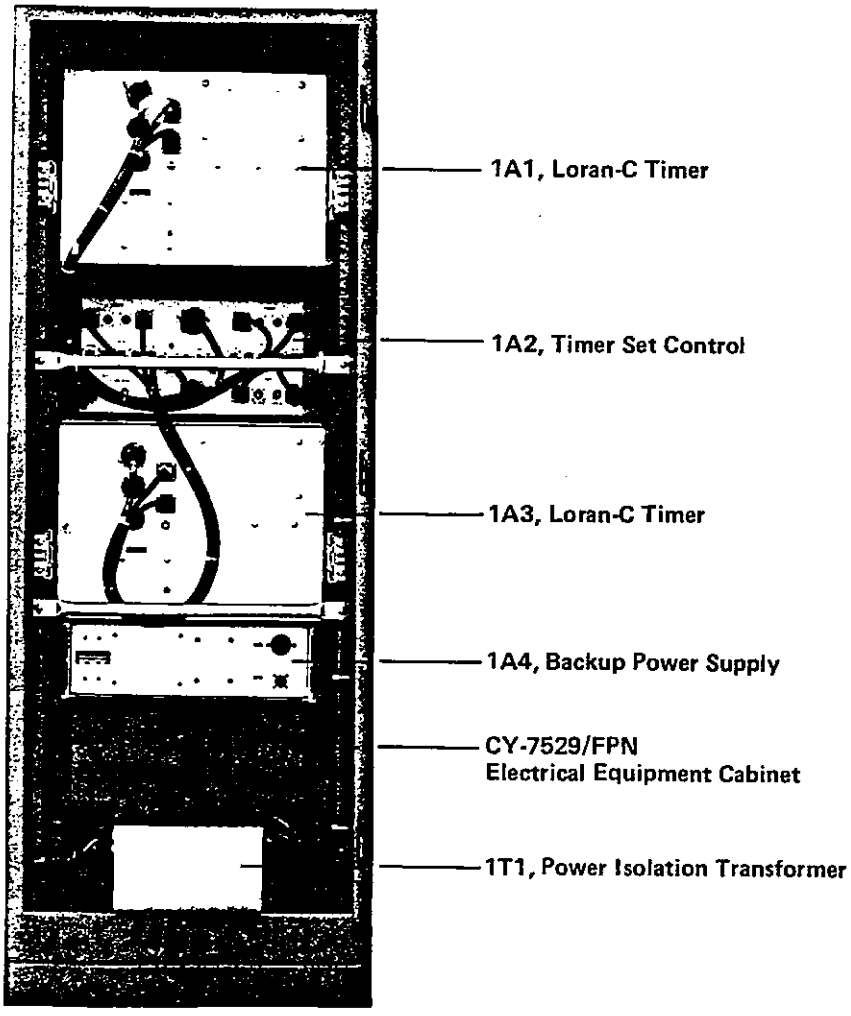


Figure 2.3. Electrical Equipment Cabinet (Rear View)

2.3.4.2. Refer to Figure 2.4 for primary power connections. Terminal Board 1TB1 is located directly in front of the Isolation Transformer in the base of the Electrical Equipment Cabinet. Route the primary AC power cable into the Electrical Equipment Cabinet and make the following connections:

a. Strap 1TB1-1, 1TB1-2, and 1TB1-3 together.

b. Strap 1TB1-4, 1TB1-5, and 1TB1-6 together.

c. Strap 1TB1-7, 1TB1-8, and 1TB1-9 together.

d. Connect a ground strap from 1TB1-5 to the equipment cabinet ground stud.

e. Connect the green lead from Isolation Transformer terminal 1T1-3 to 1TB1-4.

f. On Isolation Transformer (1T1) strap 1T1-4 and 1T1-7 together, then connect a green lead from 1T1-7 to 1TB1-6.

g. Connect a black lead from Isolation Transformer terminal 1T1-5 to 1TB1-3.

h. Connect a white lead from Isolation Transformer terminal 1T1-6 to 1TB1-7.

i. Connect the black lead of the primary 115 VAC power cable (from the breaker panel) to 1TB1-14.

j. Connect the white lead of the primary 115 VAC power cable (from the breaker panel) to 1TB1-15.

k. Connect the green lead of the primary 115 VAC power cable (from the breaker panel) to 1TB1-5.

l. Connect a black lead from Isolation Transformer terminal 1T1-1 to 1TB1-14.

m. Connect a white lead from Isolation Transformer terminal 1T1-2 to 1TB1-15.

n. Connect the black lead of Timer 1 115 VAC power harness (W101) to 1TB1-3.

o. Connect the black lead of Timer 2 115 VAC power harness (W101) to 1TB1-1.

p. Connect the white lead of Timer 1 115 VAC power harness (W101) to 1TB1-9.

q. Connect the white lead of Timer 2 115 VAC power harness (W101) to 1TB1-7.

r. Connect the green lead of Timer 1 115 VAC power harness (W101) to 1TB1-6.

s. Connect the green lead of Timer 2 115 VAC power harness (W101) to 1TB1-4.

t. Connect the black lead of the AC input from the 1A4 Power Supply to 1TB1-14.

u. Connect the white lead of the AC input from the 1A4 Power Supply to 1TB1-15.

v. Connect the green lead of the AC input from the 1A4 Power Supply to 1TB1-6.

w. Connect the white lead (positive) of the DC output from the 1A4 Power Supply to 1TB1-11.

x. Connect the black lead (negative) of the DC output from the 1A4 Power Supply to 1TB1-12.

y. Connect the white lead (positive) of the +28 VDC input (W105 Harness) to 1TB1-11.

z. Connect the black lead (negative) of the +28 VDC input (W105 Harness) to 1TB1-12.

NOTE

Ensure that all connections on 1TB1 are tight. Particular attention should be directed to the ground strap connections between 1TB1-5 and the electrical equipment cabinet ground stud.

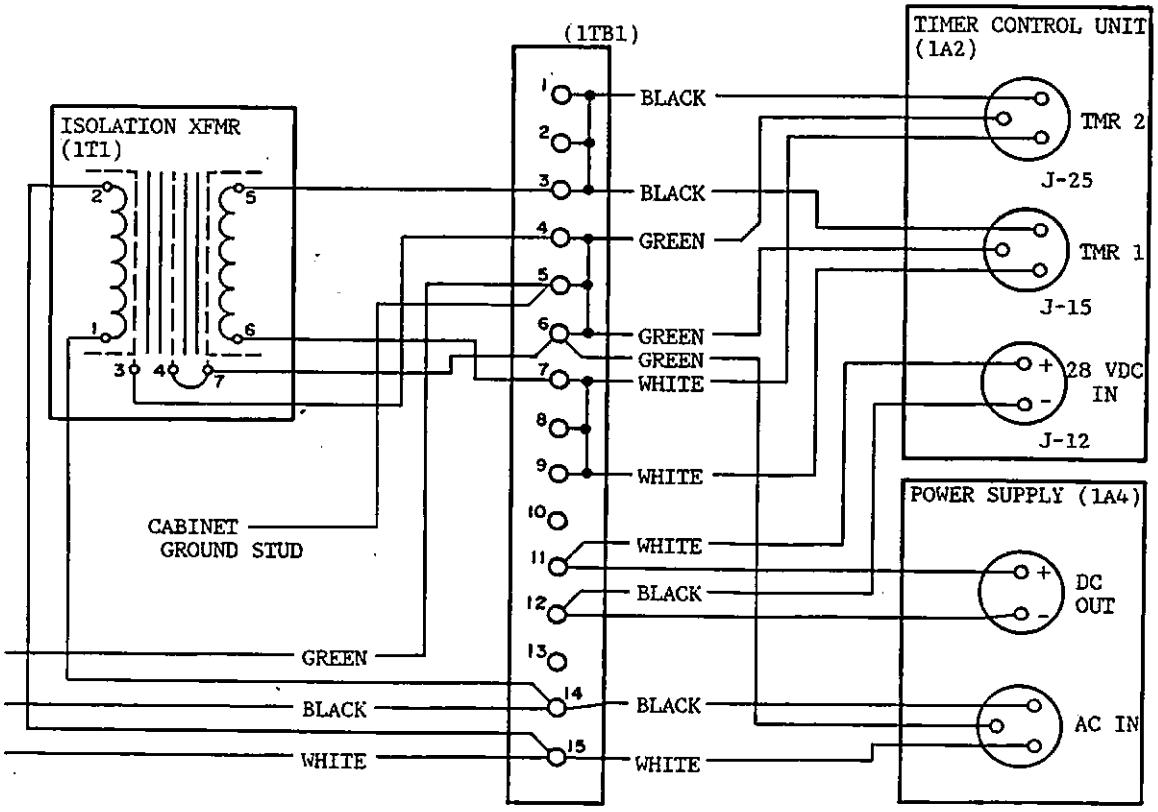
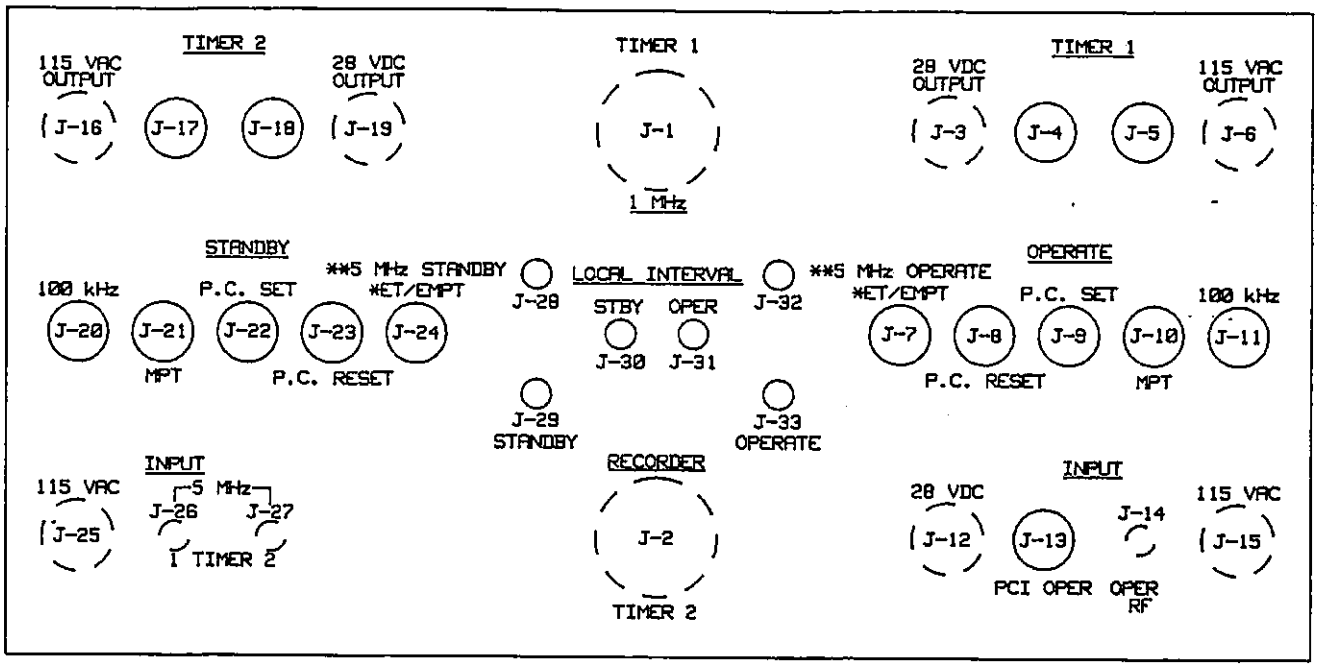


Figure 2.4. Connections for AC and DC Power

NOTE

See Figures 2.5 and 2.6 for Rear View of Timer Set Control (1A2) and Power Supply (1A4)



*AN/FPN-54A **AN/FPN-65

NOTE

Prefix all designations with 1A2A8. Solid Lines indicate those signals that are switched between Timer Number 1 and Timer Number 2 depending on position of Transmitter Drive Selector switch.

Figure 2.5. C-8621A/FPN Timer Set Control (Rear View)

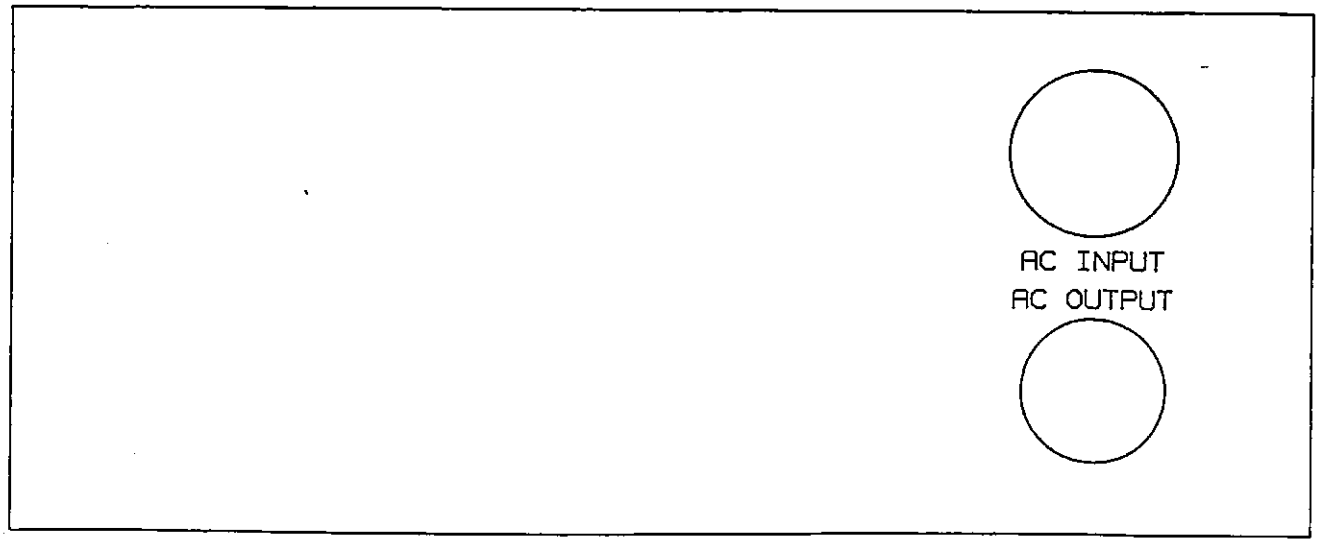


Figure 2.6. PP-7839/G Backup Power Supply (Rear View)

2.3.4.3. Anchor the LTS Electrical Equipment Cabinet by passing lag screws or bolts through the four holes located in the base of the cabinet, and secure to the deck.

2.3.4.4. The electrical equipment cabinet is a standard item that has been modified for Coast Guard use. Figure 2.3 shows the Electrical Equipment Cabinet (Rear View).

NOTE

Station drawings contain the types of cables used between the LTS and external equipment. This manual contains specifications for cables interconnecting the units of the LTS. All of the wiring and cabling in this chapter is for dual-rated stations. Single-rated stations will make connections to "low rate" jacks only.

2.3.5. Loran Timer (1A1).

2.3.5.1. Using the chassis slide mechanisms provided, install the 1A1 Loran Timer in the uppermost position of the Equipment Cabinet. Ensure that there is enough clearance so that the Loran Timer can slide in and out easily. If necessary, adjust the Loran Timer or slides for proper clearance.

WARNING

Ensure that the Equipment Cabinet is properly secured to the deck before extending the Timer chassis to its fully extended position.

2.3.6. Timer Set Control (1A2).

2.3.6.1. Position the Timer Set Control chassis directly beneath the 1A1 Loran Timer, and assemble the front panel screws and protective washers. Next, thread the panel screws into the cabinet mounting holes until the control chassis front panel is snug against the cabinet vertical support rails.

2.3.7. Loran Timer (1A3).

2.3.7.1. Position the 1A3 Loran Timer so that the side rails engage the chassis slide mechanism near the center of the cabinet just under the Timer Set Control. Carefully push the Loran Timer into the cabinet ensuring that there is enough clearance between the Loran Timer and the Timer Set Control. If the clearance is not adequate, adjust the position of the Loran Timer chassis and the chassis slide mechanism until both Loran Timers (1A1 and 1A3) may be inserted or withdrawn smoothly from the equipment cabinet. Once a proper fit is obtained, tighten all front panel mounting screws.

2.3.8. Backup Power Supply (1A4).

2.3.8.1. Position the Backup Power Supply beneath the 1A3 Loran Timer, and assemble the front panel screws and protective washers. Insert the panel screws in the cabinet mounting holes, and adjust the cabinet until the control chassis front panel is snug against the cabinet vertical support rails.

2.3.8.2. Route the primary AC and DC power cables for the Backup Power Supply in the Electrical Equipment Cabinet, and attach wires according to paragraph 2.3.4.2 (refer to Figure 2.4).

2.3.9. LTS Units Cable Interconnect. Once all units have been properly installed in the LTS equipment cabinet, and the primary and backup power cables have been connected, refer to Table 2.3 for the cable connections between the units in the LTS.

Table 2.3. LTS Units Cable Interconnect List

FROM	CABLE	TO
1TB1-3,6,9	115 VAC power harness (Timer Number 1)/W101	1A2A8J15
1TB1-1,4,7	115 VAC power harness (Timer Number 2)/W101	1A2A8J25
1TB1-11,12	28 VDC power harness/W105	1A2A8J12
1A2A8J6	115 VAC power interconnection harness/W102	1A1A3J4
1A2A8J16	115 VAC power interconnection harness/W102	1A3A3J4
1A2A8J3	28 VDC power interconnection harness/W103	1A1A3J5
1A2A8J19	28 VDC power interconnection harness/W103	1A3A3J5
1A2A8J1	Signal interconnection harness/W-486-24 W104	1A1A3J1
1A2A8J2	Signal interconnection harness/W-486-24 W104	1A3A3J1
1A1A3J6	Cross-Rate blanking (Dual-Rate only)/RG-58/U Connection made at High Rate Timer for Low Rate priority blanking	1A3A3J6

NOTE

Connectors using prefix 1A2A8, refer Figure 2.5, and connectors using prefix 1A1 or 1A3 refer to Figure 2.7.

2.3.9.1. Terminations. Inside the Timer Set Control (TSC) there are four 51-ohm BNC terminators. Typical terminations are:

a. At single-rate stations, the Operate RF inputs and 5-MHz signal inputs have BNC "Tee's" and 51-ohm BNC Terminators.

b. At dual-rate stations, the Operate RF inputs are terminated. Terminations for the 5-MHz signal lines exist only on the last TSC in the 5-MHz signal line. This is the Low Rate Loran-C Timer Set.

2.3.10. Connect the primary AC power cable to the main circuit breaker and energize, install the front panel filler plates, equipment cabinet side panels and door. Connections for UPS 115 VAC may also be made at this time.

CAUTION
Do not insert modules until DC Power Supply adjustments (paragraph 2.5.6) have been completed.

2.4. Installation Drawings. Figures 2.8 - 2.10 show the dimensions of the units of the LTS.

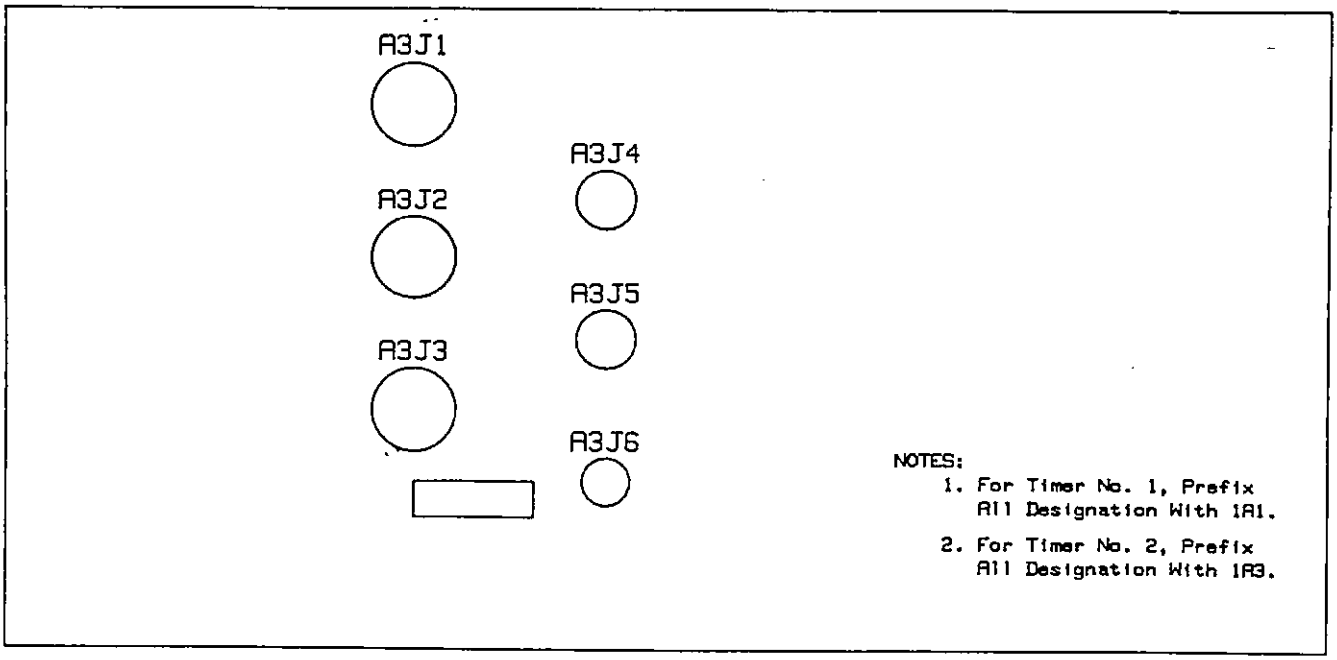


Figure 2.7. Loran Timer (Rear View)

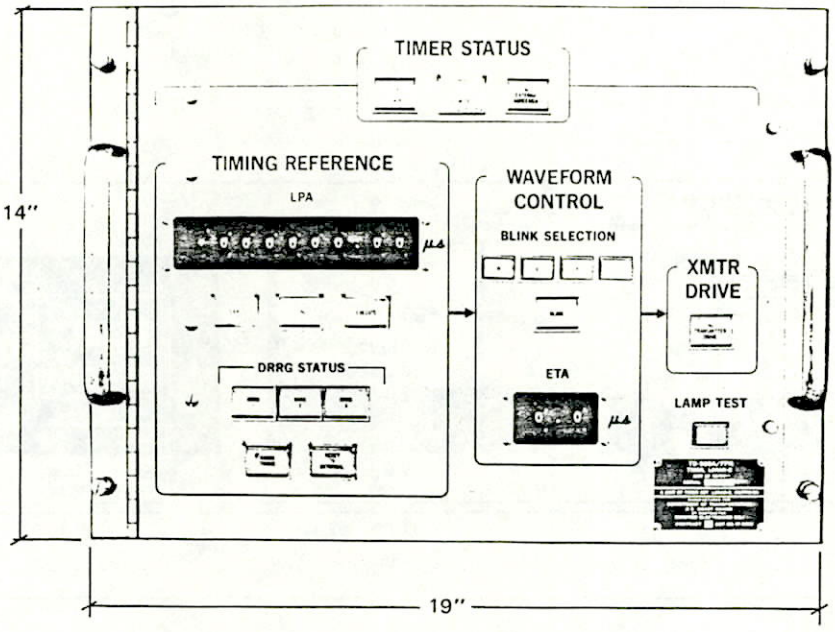


Figure 2.8. Loran Timer (Front View)

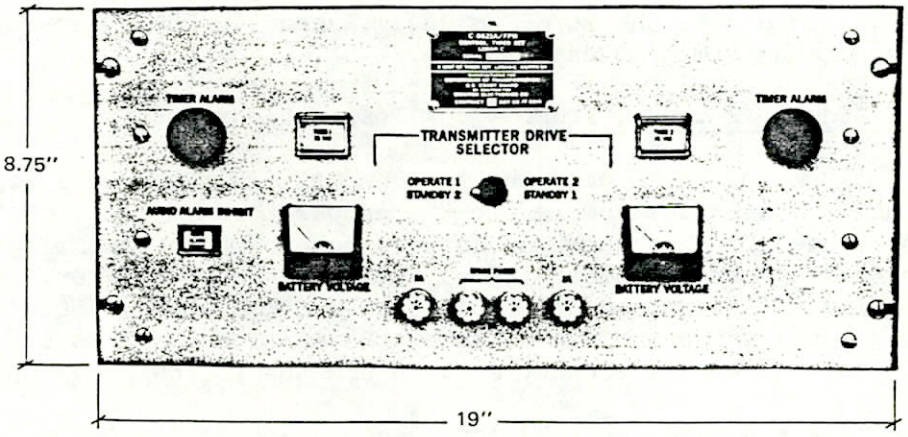


Figure 2.9. Timer Set Control

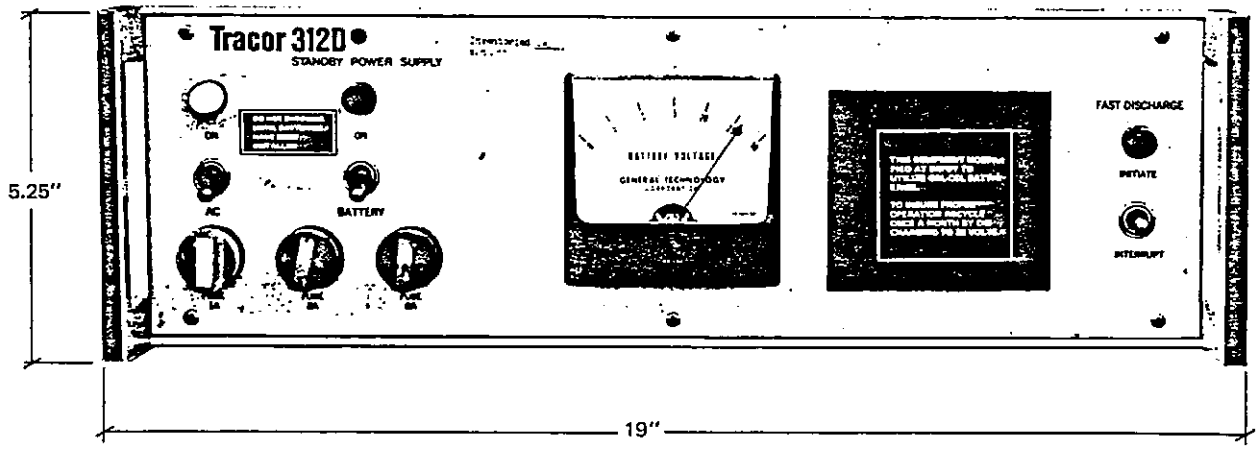


Figure 2.10. Backup Power Supply

2.5. Adjustments and Programming.

2.5.1. The Loran-C Timer Set may operate with different transmitter control configurations. Selected modules in the Loran Timer must be programmed for a specific station configuration. The Group Repetition Interval (GRI) and master or secondary operation is determined by the Program module (H card). ET/MPT or 5 MHz output, delay between EMPT and MPT, and single or dual-rate operation is determined by the DRINT/CP module (T card). The Cycle Compensation (Cycle Comp) time constant is determined by the Error Sense module (M card). Choice of SSX or Tube type transmitter is determined by the PC/MPT module (K card). The following paragraphs discuss the programming steps of each module.

2.5.2. Program Module (H card), Programming Instructions.

2.5.2.1. The Program module selects the station GRI (in uSec) by strapping the required terminal posts on the module for the proper Loran-C rate. No. 20 AWG stranded Teflon coated wire is used for this purpose. GRI programming is accomplished by adding three inputs: (i.e., by adding jumper wires between the appropriate terminals (Pin No.) on the module) 10,000's uSec + 1,000's uSec + 100's uSec, where each input value is determined by the station GRI. To set the Program module (H card) for use at a secondary station use the following example.

a. To program the H card for a GRI of 99,600 uSec, obtain by:

90,000 uSec + 9,000 uSec + 600 uSec = 99,600 uSec.

The Program module must be programmed so that the output to DRRG modules (E, F, and G cards) select the same GRI. Tables 2.4, 2.5, and 2.6 show the connections on the Program module (H card) that provide the required GRI and timing strobe (for the oscilloscope trigger) for DRRG modules E, F, and G respectively. The scope is normally triggered 100 uSec before Loran Interval Time Zero (LORTO). Table 2.7 shows the connections on the Program module (H card) that determine the appropriate blink commands to the Blink module (P card) and Local Interval reset and phase code control to the PC/MPT module (K card). Tables 2.4, 2.5, 2.6, and 2.7 are shown programmed for a GRI of 99,600 uSec as a secondary station.

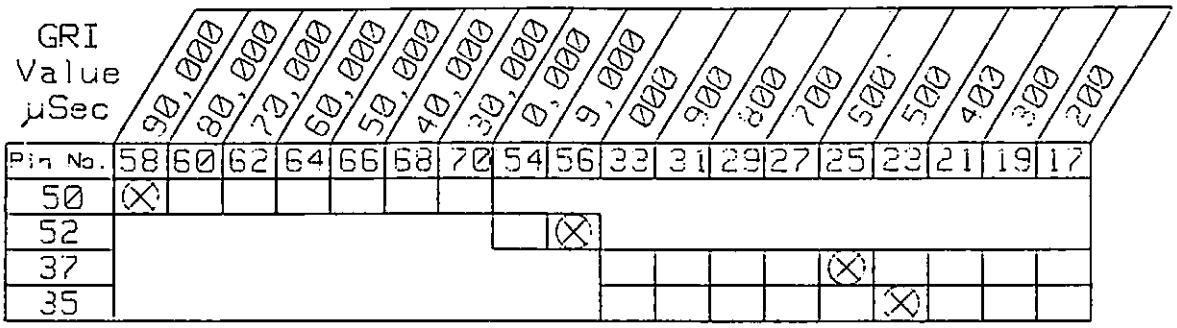
Table 2.4. Program Module (H card) for Output to DRRG Module (E card)

GRI Value µSec	90,200	80,000	70,000	60,200	50,000	40,000	30,000	0,000	9,000	000	900	800	700	600	500	400	300	200
Pin No.	47	49	51	53	55	57	59	61	63	65	67	69	71	73	75	77	79	81
45	X																	
43									X									
41														X				
39															X			

NOTE

Pin 39 is the Scope Trigger output and should be connected to the pin that is 100 uSec less than pin 41. If pin 41 is connected to zero or 200, connect pin 39 to zero or 200 respectively. An X indicates connection to be made between terminal (Pin No.) in vertical column to terminal (Pin No.) in horizontal row.

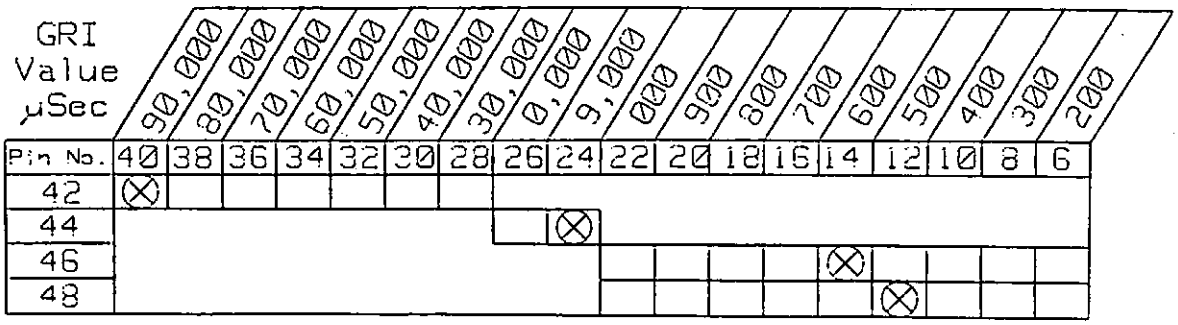
Table 2.5. Program Module (H card) for Output to DRRG Module (F card)



NOTE

Pin 35 is the Scope Trigger output and should be connected to the pin that is 100 usec less than pin 37. If pin 37 is connected to zero or 200, connect pin 35 to zero or 200 respectively.

Table 2.6. Program Modules (H card) for Output to DRRG Module (G card)



NOTE

Pin 48 is the Scope Trigger output and should be connected to the pin that is 100 usec less than Pin 46. If Pin 46 is connected to zero or 200, connect Pin 48 to zero or 200 respectively.

Table 2.7. Program Module (H card)

FUNCTION	Pin No.	1 GND	2 GND	85 GND	86 GND	3 VCC	4 VCC	83 VCC	84 VCC	5 M-BLINK	7 S-BLINK	11 MASTER	13 SECONDARY	72 MASTER	74 SECONDARY
BLINK LAMP	9										⊗				
BLINK SET INPUT	15												⊗		
PHASE CODE CONTROL	78					⊗									
M-BLINK	5	⊗													
S-BLINK	7														
LOCAL INT. RESET	76														⊗

NOTE

For Secondary operation, connect M-BLINK (Pin 5) to GND (Pin 1)

For Master operation, connect S-BLINK (Pin 7) to GND (Pin 1)

For Secondary operation, connect Phase Code Control (Pin 78) to VCC (Pin 3)

For Master operation, connect Phase Code Control (Pin 78) to GND (Pin 2)

2.5.3. DRINT/CP Module (T card), Programming Instructions.

2.5.3.1. DRINT/CP module (T card) must be programmed according to the particular transmitter installed and for single or dual-rate operation. Refer to Figure 7.29 for locations of all jumpers. Table 2.8 lists the connections for a particular station configuration. No. 20 AWG solid bare wire is used and should be soldered to the terminal posts, for programming connections as shown in Table 2.8.

2.5.4. PC/MPT Module (K card), Programming Instructions.

2.5.4.1. Refer to WO486-30/PC/MPT parts locator, Figure 7.32 for the location of thumbwheel switches S1, S2, and S3. Table 2.9 provides the preliminary thumbwheel switch settings for all transmitter types.

2.5.5. Error Sense Module (M card), Programming Instructions.

2.5.5.1. Error Sense module (M card) may be programmed to select various time constants for the Cycle Compensation (Cycle Comp) loop. Normally, the Error Sense module is programmed for the shortest time constant (shortest time constant is fastest operation). This time constant is equal to the number shown in Table 2.10 times the GRI in seconds (9960 = 0.0996 Sec). Table 2.10 shows the programming for the Error Sense module (M card).

Table 2.8. DRINT/CP Module (T Card) Programming

FUNCTION	DESIRED OUTPUT	TRANSMITTER	PROGRAMMING CONNECTIONS
Select ET/EMPT, EMPT, or 5 MHz from Loran-C Timer	5 MHz	AN/FPN-64(V)	E12 to E14 E13 to E15
	ET/EMPT or EMPT	AN/FPN-39 AN/FPN-42 AN/FPN-44,44A,45	E16 to E17 E18 to E19
Select delay between EMPT and MPT	40 uSec	AN/FPN-64(V)	E3 to E9 E4 to E10
	20 uSec	AN/FPN-39 AN/FPN-42 AN/FPN-44,44A,45 bias pedestal tail biter	E4 to E10
	160 uSec	AN/FPN-44,44A,45 bias pedestal under the pulse	E1 to E7 E2 to E8 E3 to E9 E4 to E10
Select ET/EMPT or EMPT	Single-Rate (ET/EMPT)	AN/FPN-39 AN/FPN-42 AN/FPN-44,44A,45	E6 to E11
	Dual-Rate Low rate: ET/EMPT High rate: EMPT	AN/FPN-39 AN/FPN-42 AN/FPN-44,44A,45	Remove jumper E6 to E11 on High rate (ET present on Low rate only

3. DRINT/CP Module (T card), Programming Instructions.

2.5.3.1. DRINT/CP module (T card) must be programmed according to the particular transmitter installed and for single or dual rate operation. Refer to Figure 7.( ) for locations of all jumpers. Table 2.8 lists the connections for a particular station configuration. No. 20 AWG solid bare wire is used and should be soldered to the cambion posts, for Programming Connections as shown in Table 2.8.

Table 2.8. DRINT/CP Module (T) Programming

FUNCTION	DESIRED OUTPUT	TRANSMITTER	PROGRAMMING CONNECTIONS
Select ET/EMPT, EMPT, or 5 MHz from Loran Timer	5 MHz	AN/FPN-64(V)	E12 to E14 E13 to E15
	ET/EMPT or EMPT	AN/FPN-39 AN/FPN-42 AN/FPN-44,44A,45	E16 to E17 E18 to E19
Select delay between EMPT and MPT	60 uSec	AN/FPN-64(V)	E3 to E9 E4 to E10
	20 uSec	AN/FPN-39 AN/FPN-42 AN/FPN-44,44A,45 bias pedestal tail biter	E4 to E10
	160 uSec	AN/FPN-44,44A,45 bias pedestal under the pulse	E1 to E7 E2 to E8 E3 to E9 E4 to E10
Select ET/EMPT or EMPT	Single-Rate (ET/EMPT)	AN/FPN-64(V) AN/FPN-39 AN/FPN-42 AN/FPN-44,44A,45	E6 to E11
	Dual-Rate	AN/FPN-64(V)	E6 to E11
	Dual-Rate Low rate: ET/EMPT High rate: EMPT	AN/FPN-39 AN/FPN-42 AN/FPN-44,44A,45	Remove jumper E6 to E11 on High rate (ET present on Low rate only

Table 2.9. PC/MPT Module (K card) Programming

SWITCH	TUBE-TYPE TRANSMITTERS	AN/FPN-64(V)
S-3 (Hundreds)	0	5
S-2 (Tens)	1	1
S-1 (Units)	1	1

Table 2.10. Error Sense Module (M card) Programming

TIME CONSTANT/GRI	PROGRAMMING CONNECTIONS	
120	E8 to E9	E8 to E10
240	E8 to E9	E5 to E10
360	E8 to E9	E6 to E10
480	E5 to E9	E6 to E10
600	E7 to E9	E8 to E10
720	E7 to E9	E5 to E10
840	E7 to E9	E6 to E10

2.5.6. DC Power Supply Adjustments. Ensure the Loran Timer is in the Standby mode. Withdraw the Loran Timer to its fully locked open position. (For initial power supply adjustments remove all modules from the card file.) Remove the top cover, and remove fuses F1 and F2 in the Timer Set Control (1A2). Power Supplies 1A1A4, 1A1A5, 1A1A6 and 1A1A7 should be adjusted while installed in the Loran Timer. Energize the Loran Timer by pressing the Timer ( )115 VAC switch. Refer to Figure 2.11 for location of the power supply modules and chassis terminal boards. The following test equipment is required:

a. Calibrated oscilloscope with a X10 probe

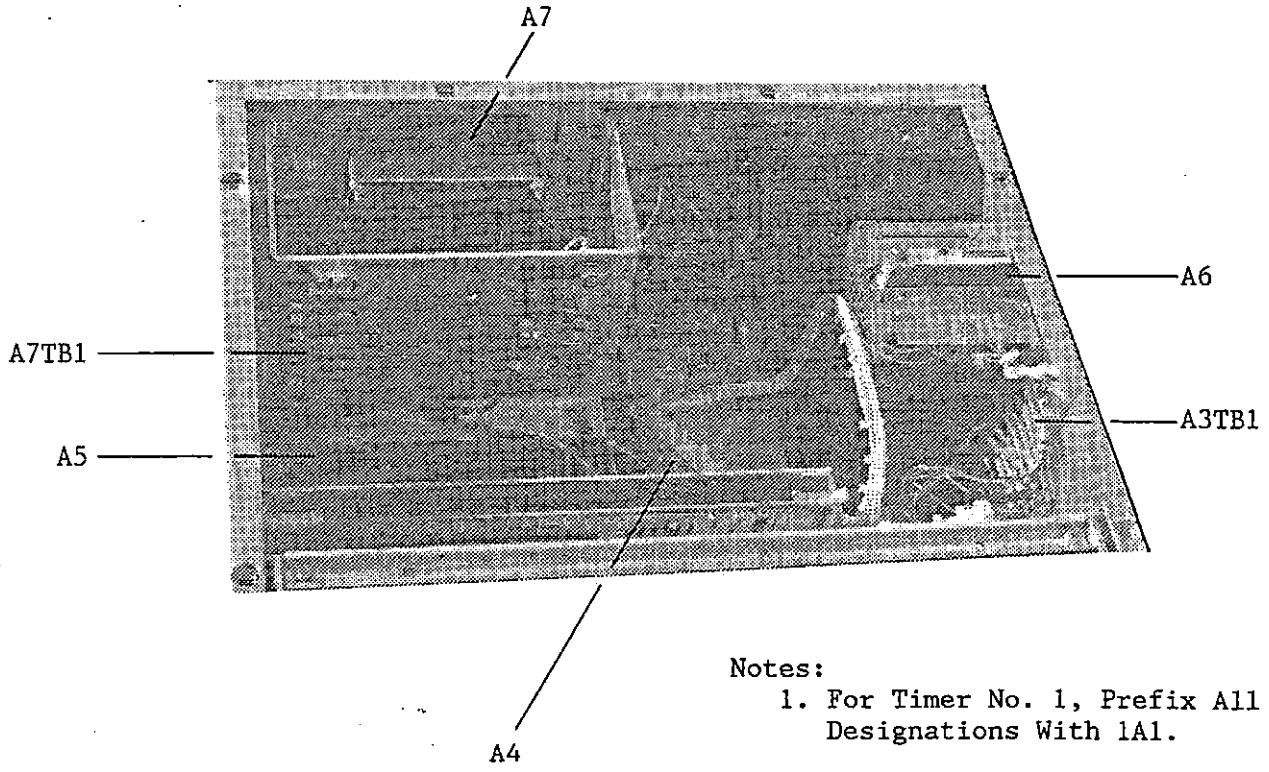
b. Digital Multimeter

CAUTION

Accomplish Power Supply checks and adjustments only when the Loran Timer is in the Standby mode.

NOTE

All Loran Timer power supply voltages are to be checked for ripple and "glitches". The ripple should not exceed 1.0 mV p-p. Put the scope probes on same terminals used to measure voltages. Do NOT measure voltage and ripple at the same time as some Digital Voltmeters can introduce noise.



Notes:

1. For Timer No. 1, Prefix All Designations With 1A1.
2. For Timer No. 2, Prefix All Designations With 1A3.

Figure 2.11. Power Supply Locations in the Loran Timer

2.5.6.1. 1A1A4 +5 VDC Power Supply Adjustment. Set the meter range to 10 VDC. Connect the negative lead of the multimeter to 1A1A3TB1-3, the positive lead to 1A1A3TB1-1. If necessary, adjust the voltage control (VA) on the rear apron of the Loran Timer chassis until the meter indicates 5.0 VDC $\pm$0.1 VDC.

NOTE

Power Supply 1A1A4 current limit adjustment is factory set and should not be adjusted.

2.5.6.2. 1A1A5 +28 VDC Power Supply Adjustment. Set the meter range to 50 VDC. Connect the negative lead of the multimeter to 1A1A7TB1-8, connect the positive lead of the meter to 1A1A7TB1-9. If necessary, adjust the Voltage Adjust control on the top front left corner of the power supply 1A1A5 to obtain 28.0 VDC.

2.5.6.3. 1A1A6 ±15 VDC Power Supply Adjustment. The 1A1A6 power supply is a dual output, ±15V supply. This power supply has an overvoltage protection circuit (LC-OV-11) that is set for 35.5 VDC or approximately 18.3% over power supply output, and must be set before adjusting the power supply output. Use the following procedure to adjust the Over-Voltage Protection circuit and the power supply output:

a. Set the voltmeter range to 50 VDC. Connect the negative lead to 1A1A3TB1-5, and the positive lead to 1A1A3TB1-9.

b. Adjust the voltage control (marked VDC ADJ) on the left side of the power supply 1A1A6 to obtain 35.5 VDC.

c. Slowly adjust the Over-Voltage Protector (LC-OV-11) until there is an abrupt drop in the output voltage. The over-voltage protection circuit is now set. DO NOT adjust the over-voltage protector beyond this point.

d. De-energize the Loran Timer primary power so the Over-Voltage Protection circuit will reset. Before re-applying power, decrease (turn CCW) the VDC ADJ Control on the left side of the power supply several turns.

e. Energize the Loran Timer and adjust the VDC ADJ Control so the output of the 1A1A6 power supply is +30.0 VDC ±0.1 VDC.

f. Check the voltage between ground and 1A1TB1-5 (should be -15 V ±1 V) and between ground and 1A1TB1-9 (should be +15 V ±1 V).

2.5.6.4. 1A1A7 +5 VDC Power Supply Adjustment.

NOTE

The 1A1A5 Power Supply must be adjusted before the 1A1A7 Power Supply is adjusted.

a. Set the meter range to 10 VDC. Connect the negative lead of the multimeter to 1A1A7TB1-8, connect the positive lead to 1A1A7TB1-2.

b. If necessary, adjust the 1A1A7 power supply Output Voltage control to obtain +5.0 VDC, ±0.1 VDC.

2.5.6.5. Module Installation. Once all required modules are programmed properly and all power supply adjustments have been made, remove power from the Loran Timer and install all printed circuit modules so that the colored extractor handles are at the top (component side to the right), and matched to the color stripes on the rail of the module file. Slide each module into its guide, and firmly press into place using thumb pressure at the top and bottom of the module.

2.5.6.6. After all modules have been installed, energize the Loran Timer and recheck power supply adjustments (refer to paragraph 2.5.6).

2.5.6.7. Disconnect the meter leads, replace the top cover, and release the lock mechanism to slide the Loran Timer into the cabinet. Power supplies 1A3A4, 1A3A5, 1A3A6, and 1A3A7 located in 1A3 Loran Timer Number 2 may be adjusted using the procedures discussed in paragraph 2.5.6.

2.6. Initial Operation. Initial operational check is to be performed after all connections to external equipments have been made (see Figure 1.6).

2.6.1. Equipment Turn-On. Perform the following steps to energize the Loran-C Timer Set:

a. Press the TIMER 1 115 VAC and TIMER 2 115 VAC indicator/switches on the Timer Set Control so that the lamps illuminate.

b. Ensure that fuses F1 and F2 are in the Timer Set Control.

c. Press the LOCAL/REMOTE indicator/switch on both Loran Timers so that both lamps indicate the same mode of operation (LOCAL or REMOTE).

d. Press the CHECK TIMING indicator/switch on both Loran Timers.

e. Press the RESET TO EXTERNAL switch on either Loran Timer. It may be necessary to press the RESET TO EXTERNAL switch several times for all lights to extinguish.

f. All red lights should now be out and the Loran-C Timer Set is ready for operation.

2.6.2. Equipment Turn-Off. The following steps are necessary for de-energizing the Loran-C Timer Set:

a. Remove fuses F1 and F2 from the Timer Set Control.

b. Press the TIMER 1 115 VAC and TIMER 2 115 VAC indicator/switches on the Timer Set Control so that the lamps are extinguished.

c. If applicable, disconnect the UPS 115 VAC.

2.6.3. Equipment Operation Check. Perform the following steps to initially check the Loran Timer for proper operation. Refer to Figure 2.12 for location of all switches and indicators.

2.6.3.1. Lamp Test. Depress and hold the LAMP TEST switch for a few seconds. All front panel lamps on the Loran Timer should light (except as noted below), and the Audio Alarm should sound (if not inhibited). Illumination of the REMOTE/LOCAL and OPERATE/STANDBY lamps will depend upon the mode of operation. BLINK lamps W, X, Y and Z will not light in either the OPERATE or STANDBY mode when the LAMP TEST switch is depressed.

2.6.3.2. LPA Entry into Timer Number 1. Set Loran Timer No. 1 for LOCAL operation. Use the thumbwheel switches on the front of Loran Timer No. 1 and select an LPA equal to 1 GRI. Momentarily depress the LOAD indicator/switch. The LOAD lamp should light and the CLEAR lamp should extinguish. Momentarily depress the EXECUTE indicator/switch. The EXECUTE lamp should remain on until the Loran Timer executes the LPA. When the Loran Timer completes execution, the EXECUTE lamp will extinguish and the CLEAR lamp should light. The NO EXTERNAL AGREEMENT lamp should be lit on Loran Timers No. 1 and No. 2, and if not inhibited, the audio alarm should be heard.

2.6.3.3. LPA Entry into Timer Number 2. Set Loran Timer No. 2 for LOCAL operation. Select the same value LPA used in the previous step for Timer Number 2. Momentarily depress the LOAD and then the EXECUTE indicator/switches. When Timer Number 2 has entered the LPA, the NO EXTERNAL AGREEMENT lamp should extinguish on Loran Timers No. 1 and No. 2 and the audio alarm will terminate.

2.6.3.4. Blink Test. Set the Loran Timer for LOCAL operation. Begin blink by depressing the W indicator/switch on the Loran Timer. The W lamp will light and the BLINK lamp will flash according to the Loran Timer configuration. If the Loran Timer is configured as a Master, the BLINK lamp will flash the blink code for W. (Due to factors in design, the blink indicator will not indicate the first "short" flash for the blink code, but will indicate all other parts of the blink code). If the Loran Timer is configured as a Secondary, the BLINK lamp will flash on and off in the pattern for Secondary Blink. Stop blink by depressing the W indicator/switch; the W lamp and the BLINK lamp should extinguish. Perform the same procedure for starting and stopping blink on X, Y, and Z, one at a time.

2.6.3.5. Check Timing. Remove fuse F1, and depress the TIMER 1 115 VAC switch. Replace F1 and depress the TIMER 1 115 VAC switch. This will cause the DRRG modules to be out of agreement. The CHECK TIMING lamp should light. Depress the CHECK TIMING indicator/switch and the light should extinguish. Depress the RESET TO EXTERNAL indicator/switch to clear Timer alarms.

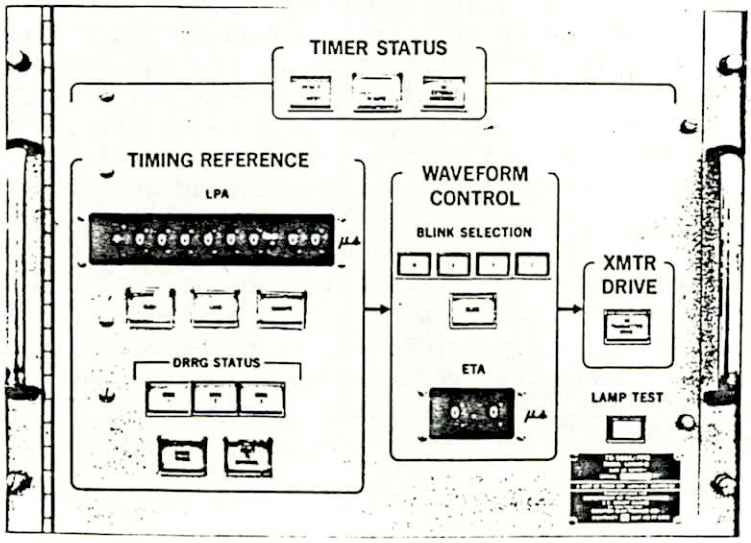


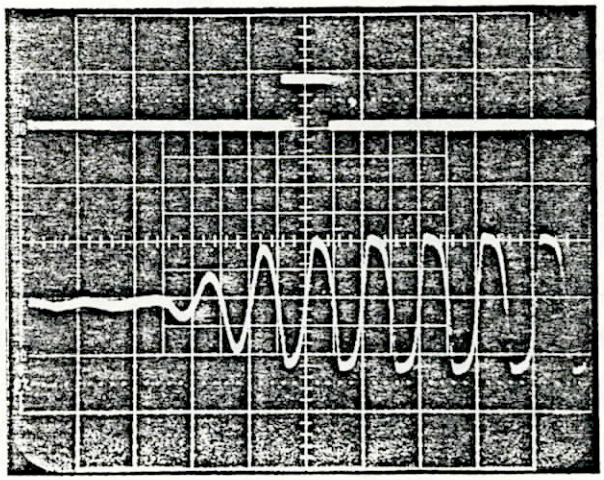
Figure 2.12. Loran-C Timer

2.7. Cycle Compensation Loop Jump Point. This adjustment procedure is performed as the first "ON-AIR" alignment for the Operate Loran Timer. This alignment will compensate for the local path delays (difference between the time the appropriate signals leave the Loran Timer and the time the "OPERATE RF" from the transmitter is sampled by the Cycle Comp) which will vary from station to station. Since the local path delay is a sum of transmission line delays, station layout, transmitter delays, and transmitter type, it is very important that all transmitters and associated equipment be completely installed before this adjustment is made. Since the Loran-C Timer Set was originally developed, several major changes have been incorporated in the system which have caused the Cycle Comp alignment to become a more critical adjustment. The most extensive change was the introduction of the WO486-28B/DRINT/CP module (T card). This module permits the transmitted Loran-C signal to be modulated (pulse position modulation on any or all Loran-C pulses) with communications information.

At some installations, communications modulation is introduced into the signal by phase shifting (advancing or delaying) the Cycle Comp 100 kHz, which in turn shifts the multipulse triggers (MPT). The Cycle Comp loop jump point can be exceeded, resulting in "10 uSec jumps" in the transmitted signal, on a regular basis if communications modulation is present and the input trigger to the reclock circuit is near the reclock edge of the reclock waveform. If the quiescent point of the Cycle Comp loop is properly calibrated, then the input trigger (MPT8 from the WO486-30/PC/MPT module) will reside as far as possible from any reclock edge of the Cycle Comp 100 kHz. Since reclock edges occur every 10 uSec, the input trigger should be centered in this "10 uSec reclock window". Exact centering will allow modulation of ±5 uSec before a jump point is reached. Realistically, due to the precision with which the jump point can be calibrated and due to normal Cycle Comp loop activity a modulation limit of about ±3.5 uSec should be imposed.

2.7.1. Procedures for Setting Cycle Comp Jump Point. This procedure is divided into two steps. Step 1 is the "Coarse" adjustment and step 2 is the "Fine" adjustment. The coarse adjustment will determine which zero crossing of OPERATE RF will be sampled by the Cycle Comp loop. The fine adjustment will center the "10 uSec Reclock Window" on the coarse MPT (CMPT). This is accomplished by changing the start time (pin 10 of DRRG E, F, and G cards) and stop time (pin 8 of DRRG E, F, and G cards) of the Cycle Comp Reference Strobe (M card, TP5 yellow) in 1 uSec increments, by selecting the DRRG outputs available at pins 81, 65, 67, 69, 68, 77, 75, 73, 79, and 71. Since the start/stop is determined by majority gating of these selected outputs, the same adjustment must be made to all 3 DRRG modules. The actual adjustment is made by moving wires (changing taps) on the backplane of the card file and is made only during a new installation or replacement of a Loran Timer.

2.7.1.1. Coarse Adjustment. Use an oscilloscope as outlined in Figure 2.13. Adjust S1, S2 and S3 on the PC/MPT (K card) as required to center the Reference Select Gate (approximately 8 uSec wide) on the third positive zero crossover. S1 will move the gate in 1 uSec steps, S2 in 10 uSec steps, and S3 in 100 uSec steps. Connect and set an oscilloscope as outlined in Figure 2.14. Adjust S1 and S2 on the PC/MPT (K card) to center the Reference Strobe within the Reference Select Gate as shown in the figure.



SIGNAL AND SOURCE	SETTINGS
	TRIGGER
Channel A: TP4 (Blue) ERROR SENSE module (M) Reference Select Gate	(-) External
Channel B: TP2 (Orange) ERROR SENSE module (M) Limited Operate RF	MODE Delayed Sweep
Trigger: TP7 (RED) any DRRG module (E,F,G) Channel A & B, ALT	HORIZONTAL: 10 uSec/Div Main Sweep 0.5 mSec/Div
X10 Scope Probes	VERTICAL: 5 V/Div

Figure 2.13. Coarse Positioning of the Reference Strobe

2.7.1.2. Fine Adjustment. To determine the amount and direction to program the "taps" on the DRRG module's backplane, view the Reclock Pulse Width signal on the DRINT/CP module (T card) at TP4 (gray). Trigger the oscilloscope on (-) Internal, set the vertical to 1V/Div or 2V/Div and the horizontal to 1 uSec/Div. If the Reclock Pulse Width is not low for 5 uSec, $\pm$.5 uSec, then fine adjustment will be required. Note the width of the waveform, and refer to Table 2.11 to determine the amount and direction of adjustment that is required (e.g., if the reclock pulse width is 2.0 uSec, Table 2.11 would require that the reference strobe start/stop time occur 3 uSec later). Once you have determined the amount and direction of required adjustment, refer to Table 2.12 to determine the proper tap settings. To use Table 2.12, you must first determine to what taps pins 10 and 8 (DRRG module) are connected by checking the backplane wiring. Locate these settings in the "Present tap setting" column. Locate the correct tap settings along the same line in the column under the required adjustment. In the example above, the Reclock Pulse Width was 2.0 uSec. Table 2.11 listed a "3 uSec later" adjustment. If the Loran Timer under test has a preset tap setting of pin 10 connected to pin 68 and pin 8 connected to pin 73, then the correct tap settings (as listed along the same line, under the "3 uSec later" column) require connection of pin 10 to pin 73 and pin 8 to pin 81. This will effect a change of "3 uSec later". Once the taps have been changed on all 3 DRRG modules, recheck the coarse adjustment as outlined in Figure 2.13 and Figure 2.14. Small adjustments of S1 might be required to achieve the waveforms shown. Make the adjustments required and then recheck the Reclock Pulse Width as outlined above and make the corrections as required. Repeat the

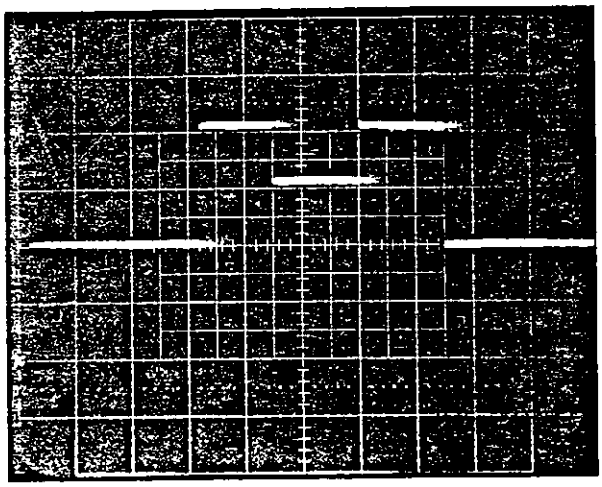
Table 2.11. Reclock Pulse Width Adjustment
(See paragraph 2.7.1.2)

DRINT TP4 (LOW) WIDTH IN uSEC	0.0 to 0.5	0.5 to 1.5	1.5 to 2.5	2.5 to 3.5	3.5 to 4.5	4.5 to 5.5	5.5 to 6.5	6.5 to 7.5	7.5 to 8.5	8.5 to 9.5	9.5 or Greater
AMOUNT ADJUST REQUIRED	5 uSec Later	4 uSec Later	3 uSec Later	2 usec Later	1 uSec Later	No Adjust Req'd.	1 uSec Earlier	2 uSec Earlier	3 uSec Earlier	4 uSec Earlier	5 uSec Earlier

Table 2.12. Tap Setting Adjustment
(See Paragraph 2.7.1.2)

PRESENT TAP SETTINGS			TAP SETTINGS FOR REQUIRED AMOUNT OF ADJUSTMENT																	
			1 uSec LATER		2 uSec LATER		3 uSec LATER		4 uSec LATER		5 uSec LATER		5 uSec EARLIER		4 uSec EARLIER		3 uSec EARLIER		2 uSec EARLIER		1 uSec EARLIER	
10	8		10	8	10	8	10	8	10	8	10	8	10	8	10	8	10	8	10	8	10	8
81	69		65	68	67	77	69	75	68	73	77	79	77	79	75	71	73	81	79	65	71	67
65	68		67	77	69	75	68	73	77	79	75	71	75	71	73	81	79	65	71	67	81	69
67	77		69	75	68	73	77	79	75	71	73	81	73	81	79	65	71	67	81	69	65	68
69	75		68	73	77	79	75	71	73	81	79	65	79	65	71	67	81	69	65	68	67	77
68	73		77	79	75	71	73	81	79	65	71	67	71	67	81	69	65	68	67	77	69	75
77	79		75	71	73	81	79	65	71	67	81	69	81	69	65	68	67	77	69	75	68	73
75	71		73	81	79	65	71	67	81	69	65	68	65	68	67	77	69	75	68	73	77	79
73	81		79	65	71	67	81	69	65	68	67	77	67	77	69	75	68	73	77	79	75	71
79	65		71	67	81	69	65	68	67	77	69	75	69	75	68	73	77	79	75	71	73	81
71	67		81	69	65	68	67	77	69	75	68	73	68	73	77	79	75	71	73	81	79	65

NOTE: Numbers represent pin numbers for DRRG (E, F, G) connector pins.
Pins 10 and 8 represent start/stop connections.

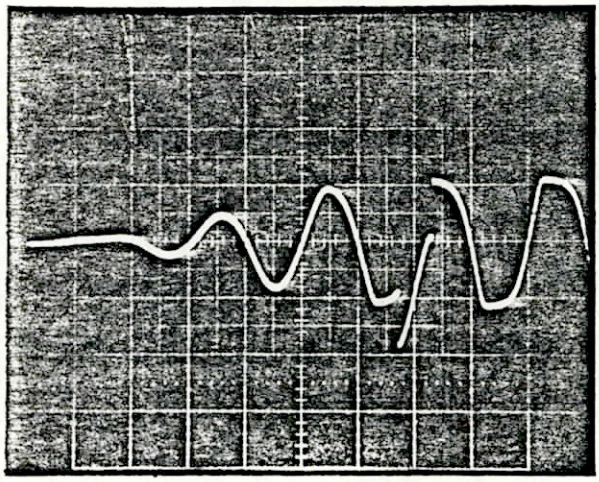


SIGNAL AND SOURCE	SETTINGS
	TRIGGER
Channel A: TP5 (Yellow) ERROR SENSE module (M) Reference Strobe	(-) External
Channel B: TP4 (Blue) ERROR SENSE module (M) Reference Select Gate	MODE Delayed Sweep
Trigger: TP7 (RED) any DRRG module (E,F,G) Vertical Mode: A&B ADDED	HORIZONTAL: 2 uSec/Div Main Sweep 0.5 mSec/Div
X10 Scope Probes	VERTICAL: 2 V/Div

Figure 2.14. Fine Positioning of the Reference Strobe

Coarse and Fine adjustment procedures until the Reclock Pulse Width is 5 uSec, $\pm$.5 uSec. As a final check to insure that the Reference Strobe has settled on the third positive zero crossover point, use an oscilloscope as outlined in Figure 2.15 after the Cycle Comp has settled, and insure that it is sampling on the third positive zero crossover. When the above procedure is followed with either Loran Timer and either transmitter, the station's Cycle Comp Jump Point has been properly calibrated. The second Loran Timer backplane can simply be wired to agree with the tap settings in the first Loran Timer. Check the coarse adjustment as outlined in Figure 2.13, and the fine adjustment as outlined in paragraph 2.7.1.2 to insure that all conditions are met. A transmitter switch will not materially change the Cycle Comp Jump Point. If both transmitters are equally "healthy", the Reclock Pulse Width on the DRINT/CP module should change less than 100 nSec with a transmitter switch.

Future changes in the adjustment of the Cycle Comp Jump Point will be necessary only if major changes are made in the station configuration (e.g., change transmitter type, relocate signal power building, reroute transmission lines, etc.). The coarse calibration procedure (Figure 2.13) must always be carried out, however, whenever an ERR SNS module or PC/MPT module is replaced.



SIGNAL AND SOURCE	SETTINGS
	TRIGGER
Channel A: TP5 (Yellow) ERROR SENSE Module (M) Reference Strobe	(-) External
Channel B: TP2 (Orange) ERROR SENSE module (M) Limited Operate RF	MODE Delayed Sweep
Trigger: TP7 (RED) any DRRG module (E,F,G)	HORIZONTAL: 5 uSec/Div (Main Sweep 0.5 mSec/Div
Channel A & B, ADDED	VERTICAL: 2 V/Div

Figure 2.15. Reference Strobe Sampling Point

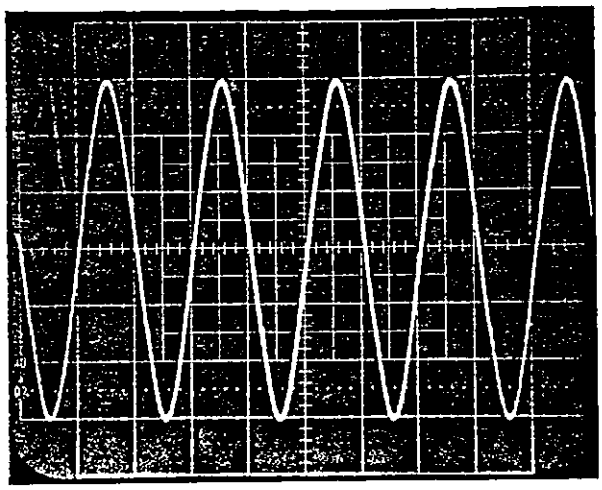
NOTE

Performing the Fine Cycle Comp Jump Point adjustment will have the same effect on timing as inserting an LPA (i.e., selecting DRRG taps to make a "1 uSec later" change will shift the Loran Timer reference the same as inserting a +1 uSec LPA). When this occurs, insert an LPA of the appropriate magnitude and direction to compensate for the change.

2.8. 100 kHz Output Signal Adjustment. Use an oscilloscope as outlined in Figure 2.16. Adjust potentiometer, R6, on the Interface module (R card) to obtain a 12 Vpp waveform.

NOTE

At tube transmitter stations, if all other gain adjustments for the transmitted Loran signal are at maximum, and higher radiated power is required, the observed waveform may be adjusted to levels higher than 12 Vpp in accordance with station drawings. However, higher levels will cause changes in the transmitting equipment jump points.



SIGNAL AND SOURCE	SETTINGS
	TRIGGER
Channel A: TP1 (Red) INTERFACE module (R) 100 kHz	(-) Internal
Ground reference is 0.4 divisions below center	MODE MAIN
Nominal level is 12 Vpp	HORIZONTAL: 5 uSec/Div
	VERTICAL: 2 V/Div

Figure 2.16. 100 kHz Output Signal Adjustment

2.9. LTS Input/Output Signals. Table 2.13 lists the input signals to, and Table 2.14 lists the output signals from, the Loran-C Timer Sets.

2.10. De-installation and Shipping.

2.10.1. The following procedure should be followed when replacing LTS units:

a. Order a replacement unit.

b. When replacement unit arrives, disconnect cables from defective unit and remove it from the cabinet.

c. Install new unit and connect cables.

d. Pack defective unit in same shipping container and return as specified in original shipping documentation.

Table 2.13. LTS Signal Input List for AN/FPN-54A and AN/FPN-65 Loran-C Timer Sets

	EQUIPMENT	JACK OR TERMINAL	SIGNAL
INPUTS TO LTS	LORAN TIMER 1A1	J2 J3 J6	Loran-C Communications Signals Remote Control Signals Cross-Rate Blanking
	LORAN TIMER 1A3	J2 J3 J6	Loran-C Communications Signals Remote Control Signals Cross-Rate Blanking
	TIMER SET CONTROL 1A2	J14 J26 J27	Operate RF 5 MHz (From Operate Frequency Standard) 5 MHz (From Standby Frequency Standard)

Table 2.14. LTS Signal Output List for AN/FPN-54A and AN/FPN-65 Loran-C Timer Sets

	EQUIPMENT	JACK OR TERMINAL	SIGNAL
	TIMER 1A1	J2 J3	Loran-C Communications Synchronizing Signals Remote Indications
	TIMER 1A3	J2 J3	Loran-C Communications Synchronizing Signals Remote Indications
OUTPUTS OF LTS	TIMER SET CONTROL 1A2	J7 J8 J9 J10 J11 J13 J20 J21 J22 J23 J24 J30 J31 J7 J24 J33 J32	* Early Triggers and Early MPT (OPERATE) Phase Code Reset (OPERATE) Phase Code Set (OPERATE) MPT (OPERATE) *** 100 kHz (OPERATE) Phase Code Interval 100 kHz (STANDBY) MPT (STANDBY) Phase Code Set (STANDBY) Phase Code Reset (STANDBY) * Early Triggers and Early MPT (STANDBY) Local Interval (STANDBY) Local Interval (OPERATE) ** 5 MHz (OPERATE) ** 5 MHz (STANDBY) Cycle Compensation Loop Recorder Drive 1 MHz to Timing Receiver

* Outputs of AN/FPN-54A LTS only.
** Outputs of AN/FPN-65 LTS only.
*** Not used with SSX, but still present at J11.

3. OPERATION.

3.1. Introduction. The AN/FPN-54A Loran-C Timer Set (LTS) and the AN/FPN-60 Transmitter Control Set (TCS) are used with Tube Transmitters. The AN/FPN-54A LTS consists of two TD-989A/FPN-54A Loran Timers, one C-8621A/FPN Timer Set Control (TSC), and one PP-7839/G Backup Power Supply. The AN/FPN-65 LTS and the AN/FSN-3 Local Status Monitor Set (LSM) are used with the Solid-State Transmitter (SSX). The AN/FPN-65 LTS consists of two TD-1365/FPN-65 Loran Timers, one C-8621A/FPN Timer Set Control (TSC), and one PP-7839/G Backup Power Supply. The Loran Timers are semi-automatic, and each Loran Timer monitors its own operation and some aspects of the other Loran Timer. The AN/FPN-54A LTS and the AN/FPN-65 LTS can be operated in either LOCAL or REMOTE control mode.

3.2. Loran Timer. The Loran Timer develops Loran-C timing waveforms, and makes adjustments to the local radiated Loran-C pulse. Equipment turn-on procedures are discussed in paragraph 3.6.1. DRRG control is automatic and DRRG status is displayed on the Timer front panel. The Loran Timer uses a local path servo mechanism, and servo activity is monitored using a DC voltage for chart recorder display. The Loran Timer may be placed in either OPERATE or STANDBY operation, and has either LOCAL control or REMOTE control modes of operation.

3.2.1. LOCAL Operating Mode. In the LOCAL mode of operation, the following functions of the Loran Timer are accessible via front panel indicator/switches:

a. Insertion of Local Phase Adjustments (LPAs). LPAs are entered in numeric form via front panel switches, and executed upon operator command. Refer to paragraph 3.7.

b. Insertion of Envelope Timing Adjustments (ETAs). Positioning the ETA thumbwheel switch determines and indicates the ETA number. Refer to paragraph 3.8.

c. Start/Stop Blink. Illumination of the indicator(s) indicates BLINK mode. Refer to paragraph 3.9.

3.2.2. REMOTE Operating Mode. REMOTE Timer operation can be selected by a front panel REMOTE/LOCAL indicator/switch. Switching to REMOTE causes electrical transfer of the inputs to the ETA and BLINK modules from the front panel controls to the rear panel connector. The Coding Delay Adjustment (CDA) module is installed in duplicate and REMOTE operation transfers control from the local CDA module to the remote CDA module. While in the REMOTE mode, operational functions must be performed by an operator (usually located at some remote site) via the Remote Control Interface (RCI) and some communications medium [i.e., teletype (TTY) link or Two Pulse Communications (TPC)]. REMOTE Timer operation would be accomplished as follows:

a. Local station code is received via TTY and activates the RCI temporary registers.

b. The message is stored in an RCI transient register.

c. The message in the register is sent to the sender via the TTY.

d. The sender verifies the message and sends the EXECUTE command.

e. The RCI transfers the message data in the temporary register to the appropriate active control register and generates the EXECUTE command.

f. When in the REMOTE control mode of operation, the following front panel switches do not control the Loran Timer:

(1) W, X, Y, and Z BLINK SELECTION indicator/switches.

(2) CLEAR, LOAD, and EXECUTE indicator/switches.

(3) The LPA and ETA thumbwheel switches.

3.2.3. Indicator Lamps. The front panel is equipped with a LAMP TEST switch which will light most front panel lamps when activated. Some indicator/switches are covered with a guard door which must be lifted before the switch can be depressed. The indicator lamps are color-coded with the following designations:

a. Green or White - indicates normal operation

b. Amber - indicates normal operation of a manually initiated action, or a condition which may require manual intervention.

c. Red - indicates a malfunction or an abnormal condition. A malfunction in either Loran Timer causing a red indicator to illuminate will also sound the audio alarm located in the C-8621A/FPN Timer Set Control.

3.3. Timer Set Control (TSC). The C-8621A/FPN Timer Set Control performs the following four basic functions:

a. Selects the OPERATE or STANDBY Loran Timer. The position of the TRANSMITTER DRIVE SELECTOR toggle switch determines which Loran Timer is the OPERATE Timer. This Loran Timer provides signals to the Transmitter Control Set (TCS) or Local Status Monitor (LSM), and controls the transmitted signal.

b. Controls electrical power to the Loran Timers. Each Loran Timer is electrically isolated from the other beyond the Timer Set Control. The 115 VAC lines for each Loran Timer are controlled by the circuit breaker and indicators on the TSC. The indicator will light when power is applied to the Loran Timer. DC backup power is individually fused for each Loran Timer. The front panel meters for each Loran Timer indicate the DC backup voltage available. This should be 28 Volts. In the event of a 115 VAC power loss, the timing reference section of each Loran Timer will automatically draw power from the DC Backup Power Supply until 115 VAC is restored. Securing power to the Loran Timers requires manual trip of the circuit breaker and removal of the DC power fuses.

c. Houses audio alarms. The TSC houses the Loran-C Timer Set audio alarms. The audio alarms are energized whenever there is a Loran Timer malfunction. Both alarms are driven when a malfunction occurs in either Loran Timer. The audio alarms can be inhibited by depressing the AUDIO ALARM INHIBIT switch. The indicator/switch lamp will illuminate whenever the alarms are inhibited.

d. Distributes signal inputs and outputs. The Timer Set Control distributes signals to and from the Loran Timers as follows (refer to Figure 2.5 for a diagram of the Timer Set Control rear apron):

(1) Loran Timer. All signal inputs to the Loran-C Timer, except Cross-Rate blanking, and outputs from the Loran-C Timer are provided through the multi-conductor jacks. The Timers must be provided 5 MHz and OPERATE RF signals at the jacks indicated (see Figure 2.7).

(2) Transmitter Drive and Local Interval. Appropriate transmitter signal and timing monitor signal outputs are provided by the coaxial and twin axial connectors.

(3) Cycle Compensation Loop. An analog output signal representing cycle compensation servo loop activity is available at the Timer Set Control, and is routed to a chart recorder. Full scale deflection of the readout is 1.0 uSec and a normal recording will show a steady track with less than 100 nSec variation. Rapid slewing of the recorder in excess of 100 nSec indicates transmitting equipment malfunction (i.e., Loran Timer, Transmitter, or Antenna).

3.4. Backup Power Supply. The TRACOR 312 (D) Backup Power Supply automatically provides uninterruptible 28 VDC backup power. The backup voltage is derived from an internal battery pack in which the battery charge is maintained by a trickle charge. The internal battery pack consists of sealed lead acid (gelled electrolyte) that provide up to 20 ampere-hours of backup power. The TRACOR 312 (D) will provide the following:

a. A trickle charge to maintain the battery pack charge with full AC power applied to the Loran Timer.

b. Full DC backup to the Timing Reference Section in the event of loss of AC power to the Loran Timer.

3.5. Controls and Indicators.

3.5.1. Loran Timer. The Loran-C Timer (see Figure 3.1) contains the following controls and indicators:

REFERENCE	DESIGNATION	DESCRIPTION
1	OPERATE/STANDBY Indicator	This split display indicator is part of the Loran-C Timer status group of indicators. The top half of the indicator is green and will light when the Loran-C Timer is controlling the On-Air signal (OPERATE mode). The bottom half of the indicator is white and will light when the Loran-C Timer is in the STANDBY mode.

REFERENCE	DESIGNATION	DESCRIPTION
2	LOCAL/REMOTE Indicator/Switch	This is an indicator/switch device. When this switch is depressed, it will alternate between LOCAL and REMOTE operating mode. The indicator will light indicating which mode is selected; green for REMOTE and amber for LOCAL.
3	NO EXTERNAL AGREEMENT Indicator	This red indicator will illuminate, and enable Loran-C Timer alarms (if these audio alarms have not been inhibited) when the timing references of the two Timers disagree by more than 150 nSec.
4	LOCAL PHASE ADJUSTMENT (LPA Switches)	These switches are used in conjunction with the LOAD, CLEAR, and EXECUTE indicator/switches to adjust the timing reference. The assembly consists of eight thumbwheel switches, each one selectable from 0 through 9, and one thumbwheel switch that selects positive or negative (+ or -).
5	CLEAR Indicator/Switch	When this green indicator is illuminated, there are no LPAs being entered into the Loran Timer and none pending. If the LPA circuitry has been armed with an LPA, but the LPA has not been executed, depressing the CLEAR switch will disarm the LPA circuitry.
6	LOAD Indicator/Switch	Depressing the LOAD switch illuminates the amber indicator, and stores the LPA selected, prior to actually inserting it. When illuminated, changes in the LPA switch settings will be reflected in the LPA LOADed.
7	EXECUTE Indicator/Switch	When the LOAD indicator is illuminated, depressing this switch will cause the LPA that was LOADed (see above) to be entered. When the EXECUTE indicator (amber) illuminates, the LOAD indicator will extinguish. When the entire LPA insertion is complete, the EXECUTE indicator extinguishes and the CLEAR indicator (green) will illuminate.
8, 9, 10	DRRG 1, 2, 3 Indicators	When any DRRG disagrees with the other two, its light (red) comes on until that DRRG is reset to agree with the majority. The reset operation is automatic unless the DRRG has failed. When no two DRRGs agree, all DRRG lights are illuminated.

REFERENCE	DESIGNATION	DESCRIPTION
11	CHECK TIMING Indicator/Switch	This indicator, when illuminated (red), indicates that the timing reference may be in error by a multiple of 200 nSec (a no majority agreement condition existed among the three DRRGs), and should be checked. Depressing the switch resets the circuit, and the indicator will extinguish if two or more DRRGs are in agreement.
12	RESET TO EXTERNAL Indicator/Switch	Depressing the RESET TO EXTERNAL switch synchronizes the timing reference to that of the other Loran-C Timer in the Loran-C Timer Set.
13, 14, 15, 16	BLINK SELECTION W, X, Y, Z Indicator/Switches	Depressing any one of these switches causes the indicator to illuminate (amber) and sends an appropriate blink command to the Loran-C Timer.
17	BLINK Indicator	The BLINK light (amber) flashes in time with a portion of the blink code.
18	ETA Switches	The ETA switches control the position of the transmitter trigger by selecting a trigger delay from 0.0 to 9.9 uSec in 0.1 uSec increments.
19	NO TRANSMITTER DRIVE Indicator	The indicator is illuminated (red) when any of the transmitter driving waveforms are absent. (i.e., 100 kHz, MPT, Phase Code, or Early Triggers/Early MPT.)
20	LAMP TEST Switch	The LAMP TEST switch activates the front panel indicators (red), except BLINK SELECTION W, X, Y, Z and OPERATE/STANDBY, while depressed. The indicators, in turn, will cause the Loran-C Timer alarm to sound.

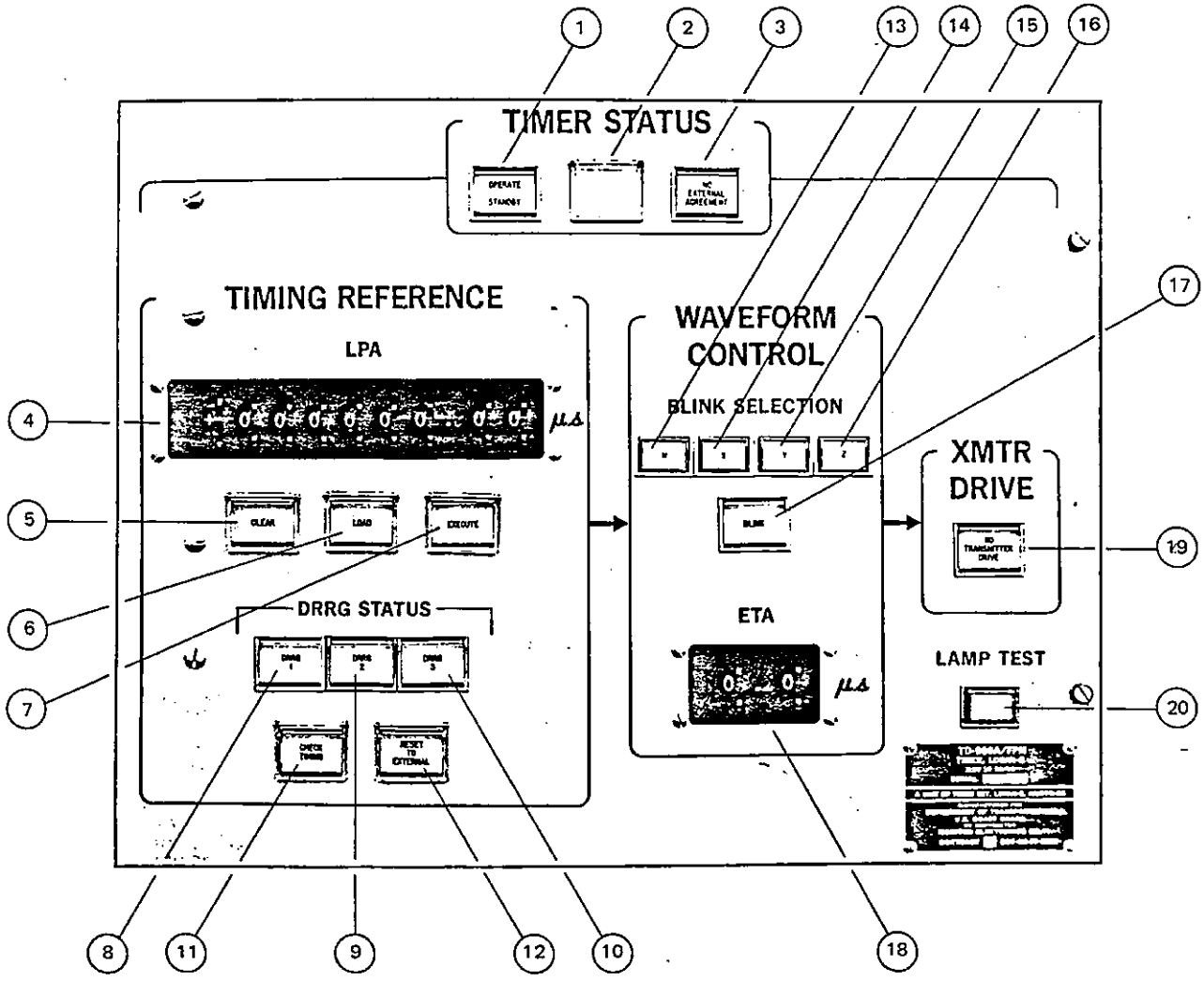


Figure 3.1. Loran-C Timer

3.5.1.1. Loran Timer Rear Panel Connectors. The Loran Timers contain the following rear panel connectors (refer to Figure 2.7):

CONNECTOR	DESCRIPTION
A3J1	Multipin connector accepts Signal Interconnect Harness W486-24 (Cable W104).
A3J2	Multipin connector accepts Communications Harness (Cable W107).
A3J3	Multipin connector accepts Remote Interface Harness (Cable W106).
A3J4	115 VAC Power connector.
A3J5	28 VDC Power connector.
A3J6	Coaxial connector accepts Blanking Signals (at dual-rated stations).

3.5.2. Timer Set Control. The Timer Set Control (see Figure 3.2) contains the following controls and indicators:

REFERENCE	DESIGNATION	DESCRIPTION
1	AUDIO ALARM INHIBIT Indicator/Switch	This switch will inhibit the audio TIMER ALARM for both Loran Timers. When pressed, the indicator will illuminate (red) indicating that the audio alarms are inhibited and will not sound in the event of a malfunction.
2, 8	TIMER ALARM Audio Alarms	Should a malfunction (red alarm) occur in either Loran Timer, both audio alarms will sound to alert the operator.
3, 7	BATTERY VOLTAGE Analog Meters	These are analog meters that monitor the DC voltage available from the Backup Power Supply. Reference item 3 indicates the backup power applied to Timer 1A1 and reference item 7 indicates the backup power applied to Loran Timer 1A3.
4	TIMER 1 115 VAC Indicator/Switch	When depressed, the switch will alternately apply and remove 115 VAC to Timer Number 1. The indicator will illuminate (amber), when 115 VAC is applied to the output jack of the Timer Set Control for Timer Number 1.
5	TRANSMITTER DRIVE SELECTOR Switch	Designates the OPERATE Timer that will provide signals to operate the transmitting equipment. The other Loran Timer will become the STANDBY Timer.

REFERENCE	DESIGNATION	DESCRIPTION
6	TIMER 2 115 VAC Indicator/Switch	When depressed, the switch will alternately apply and remove 115 VAC to Timer Number 2. The indicator will illuminate (amber) when 115 VAC is applied to the output jack of the Timer Set Control for Timer Number 2.
9,12	F1 and F2 Fuses	These are 2 amp fuses that are in series with the Backup Power Supply and each Loran Timer.
10, 11	F3 and F4 Spare Fuses	These fuse holders contain spares for F1 and F2.

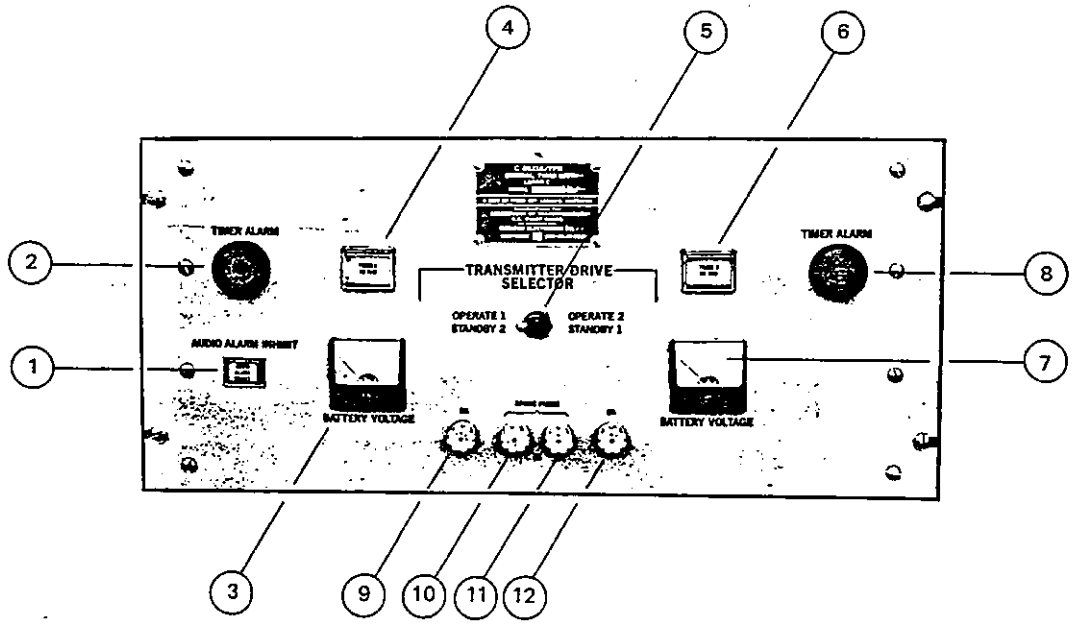


Figure 3.2. Timer Set Control

3.5.2.1. Timer Set Control Rear Panel Connectors. The Timer Set Control (1A2) rear panel contains the following connectors (refer to Figure 2.4):

CONNECTOR	DESCRIPTION
A8J1	55-pin MS connector for Signal Interconnect harness W486-24 (Cable W104) to Timer 1.
A8J2	55-pin MS connector for Signal Interconnect harness W486-24 (Cable W104) to Timer 2.
A8J3	28 VDC Output connector to Timer 1 (1A1).
A8J4	Multipulse Triggers OPERATE Timer - This connector is a non-polarized twin-axial connector in parallel with connector A8J10.
A8J5	OPERATE Timer 100 kHz Output - This connector is a non-polarized twin-axial connector in parallel with connector A8J11.
A8J6	115 VAC Output to Timer 1 (1A1).
A8J7	ET/EMPT Output from OPERATE TD-989A/FPN-54A Loran Timer. 5-MHz Output from OPERATE TD-1365/FPN-65 Loran Timer .
A8J8	Phase Code Reset OPERATE Timer.
A8J9	Phase Code Set OPERATE Timer.
A8J10	Multipulse Triggers OPERATE Timer - This connector is a polarized twin-axial connector in parallel with connector A8J4.
A8J11	100 kHz Output OPERATE Timer - This connector is a polarized twin-axial connector in parallel with connector A8J5.
A8J12	28 VDC Input.
A8J13	OPERATE Timer Phase Code Interval Output.
A8J14	OPERATE RF Input.
A8J15	115 VAC Input for Timer 1 (1A1).
A8J16	115 VAC Output to Timer 2 (1A3).
A8J17	STANDBY Timer 100 kHz Output - This connector is a non-polarized twin-axial connector in parallel with connector A8J20.
A8J18	Multipulse Triggers STANDBY Timer - This connector is a non-polarized twin-axial connector in parallel with connector A8J21.
A8J19	28 VDC Output connector for Timer 2 (1A3).
A8J20	100 kHz Output STANDBY Timer - This connector is a polarized twin-axial connector in parallel with connector A8J17.

CONNECTOR	DESCRIPTION
A8J21	Multipulse Triggers STANDBY Timer - This connector is a polarized twin-axial connector in parallel with connector A8J18.
A8J22	Phase Code Set STANDBY Timer.
A8J23	Phase Code Reset STANDBY Timer.
A8J24	ET/EMPT Output from STANDBY TD-989A/FPN-54A Loran Timer. 5-MHz Output from STANDBY TD-1365/FPN-65 Loran Timer.
A8J25	115 VAC Input for Timer 2 (1A3).
A8J26	5-MHz Input for Timer 1 (1A1).
A8J27	5-MHz Input for Timer 2 (1A3).
A8J28	STANDBY Timer 1 MHz output.
A8J29	STANDBY Timer Recorder output.
A8J30	STANDBY Timer Local Interval output.
A8J31	OPERATE Timer Local Interval output.
A8J32	OPERATE Timer 1 MHz output.
A8J33	OPERATE Timer Recorder output.

3.5.3. Backup Power Supply. The Power Supply (see Figure 3.3) contains the following controls and indicators:

REFERENCE	DESIGNATION	DESCRIPTION
1	AC Switch	Applies 115 VAC to the battery charging circuit to charge the battery pack.
2	AC ON Indicator	When illuminated, indicates that 115 VAC is applied to the battery charging circuit.
3	BATTERY Switch	When in the ON position, applies battery voltage to the output connector.
4	BATTERY ON Lamp	When illuminated, indicates that both battery fuses are operational, and battery voltage is available at the output connector.
5	BATTERY VOLTAGE Meter	Meter indicates DC voltage across the battery.

REFERENCE	DESIGNATION	DESCRIPTION
6	INITIATE/OFF/INTERRUPT Switch	This SPDT momentary contact switch controls two actions. When placed briefly in the INITIATE position, it connects the battery to the internal load, thereby initiating the fast discharge mode. When placed briefly in the INTERRUPT position, it stops the fast discharge and returns the unit to its normal operation.
7	FAST DISCHARGE Lamp	When illuminated, it indicates the unit is in the fast discharge mode.
8, 9	F2 and F3 Indicator Type Fuse Holders	These 8 amp fuses protect the positive and negative DC output connections of the power supply. A blown fuse is indicated when illuminated.
10	F1 Indicator Type Fuse Holder	This one amp fuse protects the battery charging circuit. A blown fuse is indicated when illuminated.

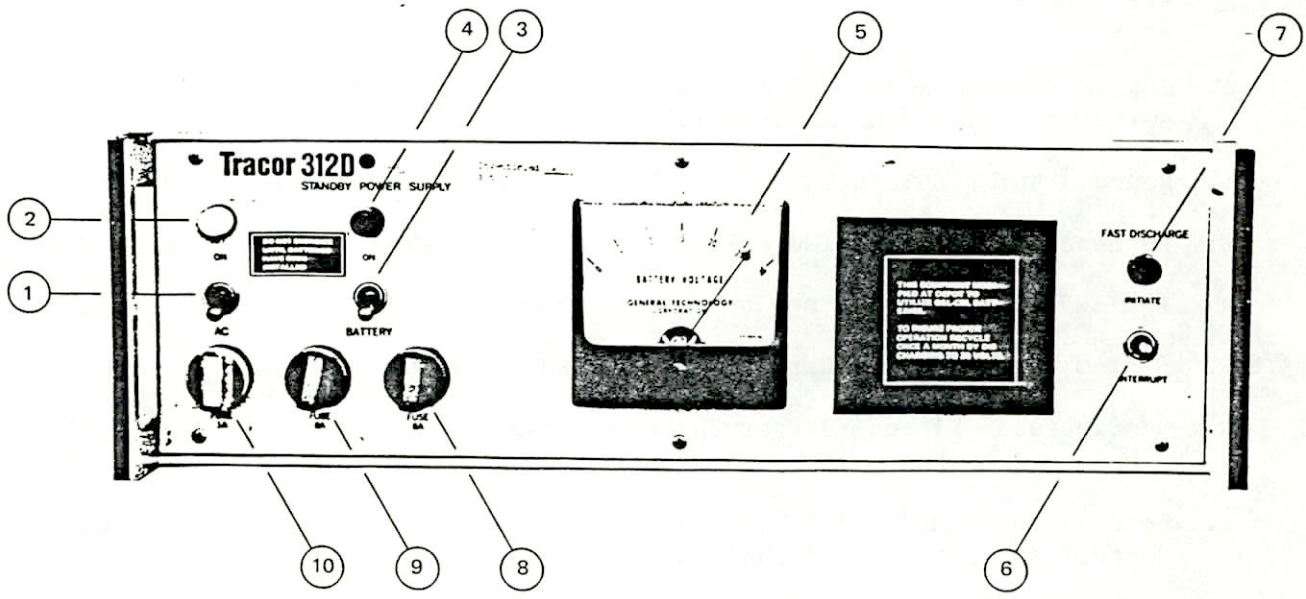


Figure 3.3. Backup Power Supply

3.5.3.1. Backup Power Supply Rear Panel Connectors. The Backup Power Supply (1A4) TRACOR 312 (D) contains the following rear panel connectors (refer to Figure 2.6):

a. The AC INPUT connector in the upper right-hand corner of the backplane, as viewed from the rear.

b. The DC OUTPUT connector in the lower right-hand corner of the backplane, as viewed from the rear.

3.6. Operating Procedure. Ensure that all units of the LTS are installed in the equipment cabinet, and that all programming and operational checks have been made prior to performing any steps in the following paragraphs.

3.6.1. System Turn-on. All equipments in the LTS cabinet are wired to the terminal block (1TB1) located in the base of the Equipment Cabinet. Primary power is applied by turning on the circuit breaker at the AC distribution panel external to the equipment cabinet. After turning on the main circuit breaker, apply power to the equipment as follows:

a. Depress the TIMER 1 115 VAC and TIMER 2 115 VAC switches on the Timer Set Control so that the indicator/switches illuminate.

b. Insert fuses F1 and F2 in the Timer Set Control.

c. Turn on the AC and BATTERY switches located on the Backup Power Supply. Both BATTERY VOLTAGE meters on the front panel of the Timer Set Control should indicate approximately 28 VDC. See reference items 3 and 7 on Figure 3.2.

d. Depress the LOCAL/REMOTE switches on both Loran Timers until both indicator switches indicate LOCAL or REMOTE as desired.

e. Depress the RESET TO EXTERNAL switch on either Loran Timer to synchronize.

f. Depress the CHECK TIMING switch on both Loran Timers.

g. All RED lights should now be extinguished.

3.6.2. System Turn-off. To turn the system OFF, use the following procedure:

a. Remove fuses F1 and F2 from the front panel of the Timer Set Control. This removes DC backup power.

b. Depress the TIMER 1 115 VAC and TIMER 2 115 VAC switches on the Timer Set Control so that the indicator switches are extinguished.

c. Turn off the AC and BATTERY switches on the Backup Power Supply (1A4).

d. Turn off the main circuit breaker.

e. Disconnect the UPS 115 VAC, if applicable.

3.6.3. Loran Timer Turn-on. To power ON the Loran Timer, use the following procedure:

a. Depress the TIMER 1 115 VAC or TIMER 2 115 VAC switch, as appropriate.

b. Insert the appropriate fuse on the Timer Set Control front panel.

c. Depress the LOCAL/REMOTE switch on this Timer only, so that LOCAL or REMOTE, as desired, is illuminated.

d. Depress the RESET TO EXTERNAL switch on this Timer only.

e. Depress the CHECK TIMING switch on this Timer only.

f. All RED lights should now be extinguished.

3.6.4. Loran Timer Turn-off. To turn the Loran Timer OFF, use the following procedure:

a. Depress the TIMER 1 115 VAC or TIMER 2 115 VAC switch, as appropriate.

b. Remove the appropriate fuse from the front panel of the Timer Set Control.

WARNING

A potential shock hazard still exists because the circuit breaker only opens one side of the AC line to the Loran Timer, and AC voltage remains on the return line.

3.6.5. Emergency Turn-off. AC power to the LTS Equipment Cabinet can be secured at the main circuit breaker. DC power must be secured by turning OFF the BATTERY switch on the Backup Power Supply (reference item 3 on Figure 3.3).

WARNING

In some configurations, Timer Number 1 is supplied with 115 VAC from a UPS. If so, power must also be secured at the UPS or at the TIMER 1 115 VAC switch.

3.7. Local Phase Adjustment (LPA) Entry Procedure. Entry of an LPA moves the timing reference, hence the time of emission of the local Loran-C pulse. An LPA is entered as follows:

a. Dial the desired LPA into the LPA thumbwheel switches. A plus (+) entry retards the timing reference signals to occur later in time, and a minus (-) entry advances the timing reference signals to occur earlier in time. The amount of movement is variable, from 0.00 to 999,999.98 uSec, in either direction, in 0.02 uSec increments. Odd numbered settings of the .01 uSec thumbwheel switch (i.e., .01, .03, .05, etc.) actually insert an LPA 0.01 uSec less than shown on the switch, and are normally not used.

NOTE

A plus (+) LPA entry at a secondary station would increase the master/secondary time difference. A plus (+) entry at a master station would decrease the master/secondary time difference.

b. Depress the LOAD switch. The LOAD indicator will illuminate and the CLEAR indicator will extinguish, meaning the Loran Timer is prepared to make the adjustment. If the LOAD indicator fails to illuminate, insure that the Loran Timer is in the LOCAL mode, if so, commence routine troubleshooting procedures. If an incorrect number has been LOADed, correct the number by readjusting the thumbwheel switches. If the LOAD switch has been pushed erroneously, depressing the CLEAR switch will disarm all circuits and indicate CLEAR. This means that movement of the thumbwheel switch did not effect Loran Timer operation.

c. Depress the EXECUTE switch. The timing reference now shifts in time by the amount shown on the LPA switches. The EXECUTE indicator illuminates while the LPA is entered. If the CLEAR light does not illuminate after ten seconds, there has been a Loran Timer malfunction, and routine troubleshooting procedures should commence. Depressing the CLEAR switch while the EXECUTE indicator is illuminated will prematurely end the LPA entry with some unknown LPA actually entered.

NOTE

Execution of an LPA takes place at the rate of 35,000 uSec per second. The maximum LPA of 999,999.98 uSec takes approximately 30 seconds. For Solid-State Transmitter (SSX) operation, the multipulse triggers will be blanked while the LPA is being EXECUTEd.

d. An LPA entry into one Loran Timer will illuminate the NO EXTERNAL AGREEMENT indicator on both Loran Timers and sound the audio alarm if not disabled. An identical LPA should now be entered in the other Loran Timer.

3.8. Envelope Timing Adjustment (ETA) Thumbwheel Use. The ETA thumbwheel switches directly control the time relationship between the multipulse triggers and the 100 kHz signals provided to the Transmitter Control Set for all stations except those with the SSX installed (refer to paragraph 3.8.1). The switches are used to change the Envelope-to-Cycle Difference (ECD) of the transmitted Loran signal.

3.8.1. ETA for Solid-State Transmitter. The ETA dial is not used to adjust envelope timing for SSX applications. The proper ETA dial setting is 0.1, and should not be changed because the ETA thumbwheel switches directly control the time

relationship of the timing reference to the multipulse triggers (MPTs) over a range of 10 uSec. They also control the time relationship between the MPTs and the 5-MHz signals provided to the Local Status Monitor (LSM).

3.9. Blink Entry. A BLINK command is accomplished by depressing the W, X, Y, or Z switch, as appropriate. The BLINK mode for Master/Secondary is programmed by jumpers on the PROGRAM module (H card). Depressing any one of the BLINK switches causes the indicator (amber) to illuminate, and if programmed for a Master station, indicates which stations are to be BLINKed. If programmed as a Secondary station, depressing any of the W, X, Y, or Z switches will turn on secondary BLINK, and the BLINK indicator will flash the appropriate code. Depressing the switch a second time will terminate the blink.

3.10. Phase Code Inversion. The Phase Code Interval (PCI) of the Loran Timer can be changed by entering an LPA equal to the chain Group Repetition Interval (e.g., for Loran rate 9930, entering an LPA of +99,300 uSec inverts the Phase Code Interval of the Loran Timer).

3.11. Monitor/Reset Functions. The Loran Timer possesses a number of monitor functions, enabling the operator to be sure all electronic circuits are operating properly. Additionally, a cross-timer reset circuit is configured so that either Timer can have its timing reference synchronized to the other Timer by depressing the RESET TO EXTERNAL switch. The following paragraphs describe the Monitor/Reset functions.

3.11.1. Timer Status.

3.11.1.1. OPERATE/STANDBY. The OPERATE/STANDBY indicator displays the Loran Timer's assignment, and is controlled by the TRANSMITTER DRIVE SELECTOR switch on the Timer Control Unit. The portion illuminated indicates the operational status of the Loran Timer. While in the OPERATE mode, the Loran Timer is controlling the On-Air signal, and only one Loran Timer can be in the OPERATE mode at any one time. The STANDBY mode indicates the Loran Timer is not controlling the On-Air signal.

3.11.1.2. LOCAL/REMOTE. The LOCAL/REMOTE indicator/switch selects and indicates the mode of Timer control. When the Loran Timer is in LOCAL, the front panel controls LPA, ETA, and BLINK selections. When the Loran Timer is in REMOTE, control of LPA, ETA, and BLINK is passed to the Remote Control Interface (RCI). The illuminated segment of the switch indicates the mode of control. Transfer from LOCAL to REMOTE may only be accomplished when the LPA circuitry is in a CLEAR state. Transfer from one mode to the other is made when the LOCAL/REMOTE switch is depressed.

NOTE

Upon application of power, the Timer may assume either the REMOTE or LOCAL state.

3.11.1.3. NO EXTERNAL AGREEMENT. The NO EXTERNAL AGREEMENT alarm indicates that the Loran Timer is not synchronized to the external reference. Each Loran Timer is used as the external reference for the other. Illumination of this indicator, except during insertion of an LPA, means that the Loran Timer or its associated frequency standard has malfunctioned. Normally, when the NO EXTERNAL AGREEMENT indicator illuminates, it will illuminate on both Loran Timers simultaneously.

3.11.1.4. External agreement between Timers occurs when the electronically selected taps on the Ø-SHIFT module (D card) are the same for both Timers, and there is coincidence in the timing reference signals. Finite delays through the coincidence detection circuits can cause abnormal conditions when the difference between the two timing references is between 0.1 and 0.2 uSec. The NO EXTERNAL AGREEMENT indication may illuminate on one Timer only (the direction of the phase difference determines which one). In either case, the RESET TO EXTERNAL command cannot synchronize the Timers, and the NO EXTERNAL AGREEMENT light will not extinguish. This condition is usually caused by a shift of one of the frequency standard signals with respect to the other.

3.11.1.5. An inherent equipment characteristic will sometimes allow a false NO EXTERNAL AGREEMENT indication after the RESET TO EXTERNAL switch is depressed and the Loran Timers have been synchronized. Therefore, it may be necessary to depress this switch a number of times in order to extinguish the NO EXTERNAL AGREEMENT light. Depressing the switch when the Loran Timers are synchronized may also produce a false NO EXTERNAL AGREEMENT indication. This can be corrected by repeatedly depressing the switch until the light is extinguished.

3.11.2. DRRG Status.

3.11.2.1. DRRG 1, 2, or 3. Illumination of any of the three DRRG lamps indicates that the timing reference of the indicated DRRG module is not in coincidence with those of the other two DRRG modules. When no two DRRG timing references are in agreement, all three DRRG lights will illuminate. The illumination of only two DRRG lights will not occur unless there is an alarm circuitry failure.

3.11.2.2. CHECK TIMING. Illumination of the CHECK TIMING light indicates that, at some time, there was no majority among the timing references generated by the three DRRG modules. Normally, in this case, the DRRG modules are automatically reset to each other in an arbitrary sequence, which extinguishes the DRRG lamps. Depressing the CHECK TIMING switch extinguishes the CHECK TIMING light if a timing reference majority has been re-established.

3.11.2.3. RESET TO EXTERNAL. Depressing the RESET TO EXTERNAL switch arms a synchronizing circuit and lights the RESET TO EXTERNAL indicator, then generates a signal that synchronizes the Loran Timer timing reference to the external timing reference pulse provided by the other Loran Timer. In normal operation, the time between arming and reset is too brief to visibly illuminate the RESET TO EXTERNAL indicator. Caution must be taken when using these switches to correct a NO EXTERNAL AGREEMENT condition since the indication will normally be present on both Loran Timers, although only one of the timing references has shifted. Determine which timing reference is desired and depress the RESET TO EXTERNAL switch on the other Loran Timer. The RESET TO EXTERNAL switch may have to be depressed several times before the NO EXTERNAL AGREEMENT indicator is extinguished.

NOTE

If only one Timer is in operation, depressing the RESET TO EXTERNAL switch will shift the timing reference to an unknown point in time.

3.11.2.4. NO TRANSMITTER DRIVE. The NO TRANSMITTER DRIVE light will illuminate if any one, or more, of the Multipulse Trigger, 100 kHz, Local Interval, or Phase Code waveforms are not present at the Timer output terminals. The alarm has a time delay of approximately three seconds and will not be activated during normal cross-rate blanking at dual-rated stations.

NOTE

In the AN/FPN-65 LTS only, during LPA execution, MPTs are inhibited. If an unusually large LPA is executed (about 100,000 uSec), MPTs may be inhibited for enough time to activate this alarm.

3.11.3. LAMP TEST. Depressing the LAMP TEST switch will sound the audio alarms, if not inhibited, and cause most of the Timer front panel indicators to illuminate without affecting Timer operation. The following indicators do not illuminate when the LAMP TEST switch is depressed:

a. W, X, Y, or Z

b. OPERATE or STANDBY (these depend only on the position of the TRANSMITTER DRIVE SELECTOR switch).

4. THEORY OF OPERATION.

4.1. Introduction. The Loran-C Timer Set discussed in this chapter refers to both the AN/FPN-54A LTS and the AN/FPN-65 LTS.

4.1.1. Loran-C Timer Set. The Loran-C Timer Set has been designed to operate within various transmitter control configurations. Both Loran-C Timer Sets provide accurate and reliable timing waveforms which control the time-of-emission of the radiated Loran-C pulses. An additional feature of the Loran-C Timer Set is the capability of modulating the Loran-C signal for communication purposes (e.g., Two Pulse Communications, Clarinet Pilgrim). There is no active synchronization to remote signals within the Loran Timer. There is an active local signal synchronization mechanism called the cycle compensation loop (Cycle Comp). This servo system ensures that the radiated signal time-of-emission does not vary in spite of changes in local signal path delays. The resolution of the Cycle Comp Loop is 20 nSec. Figure 4.1 is a block diagram showing the input and output signals of the Loran-C Timer Set.

4.1.2. Loran Timer. The AN/FPN-54A and AN/FPN-65 Loran Timers have the function of creating the timing signals necessary to drive transmitters and peripheral Loran Timing and Control equipment. Within the station, the Timer is the basic Loran timing reference generator. It provides signals required for local monitoring and generation of transmitter drive waveforms. It also provides a Local Interval signal which is normally used to blank the other rate at a dual-rated station. Figure 4.2 is a Functional Block Diagram of the Loran-C Timer.

4.1.3. Timer Set Control. The C-8621A/FPN Timer Set Control distributes OPERATE RF and 5-MHz signals to the OPERATE and STANDBY Loran Timers in both the AN/FPN-54A and AN/FPN-65 Loran-C Timer Sets. It also allows the operator to select which Timer will control the timing of the transmitted signal, and which Timer will be STANDBY, by selecting the position of a toggle switch on the front panel. The Timer Set Control receives control and alarm signals from each Timer, and sounds an audio alarm in the event of a Timer failure. The Timer Set Control also distributes and provides over-current protection for Timer 115 VAC and 28 VDC inputs. Figure 4.3 is a Functional Block Diagram of the Timer Set Control.

4.1.4. Backup Power Supply. During loss of primary power, the TRACOR-312(D) provides DC power to the Timing Reference Section of the Timers. If AC power is lost completely, the supply provides DC power from an internal battery. For normal operations, the front panel AC and DC switches should remain in the ON position. When the supply and primary equipment are connected, changeover to standby power is automatic. This chapter will discuss the Loran Timers, and Timer Set Control, leaving the details of the Backup Power Supply to the technical manual supplied by the manufacturer.

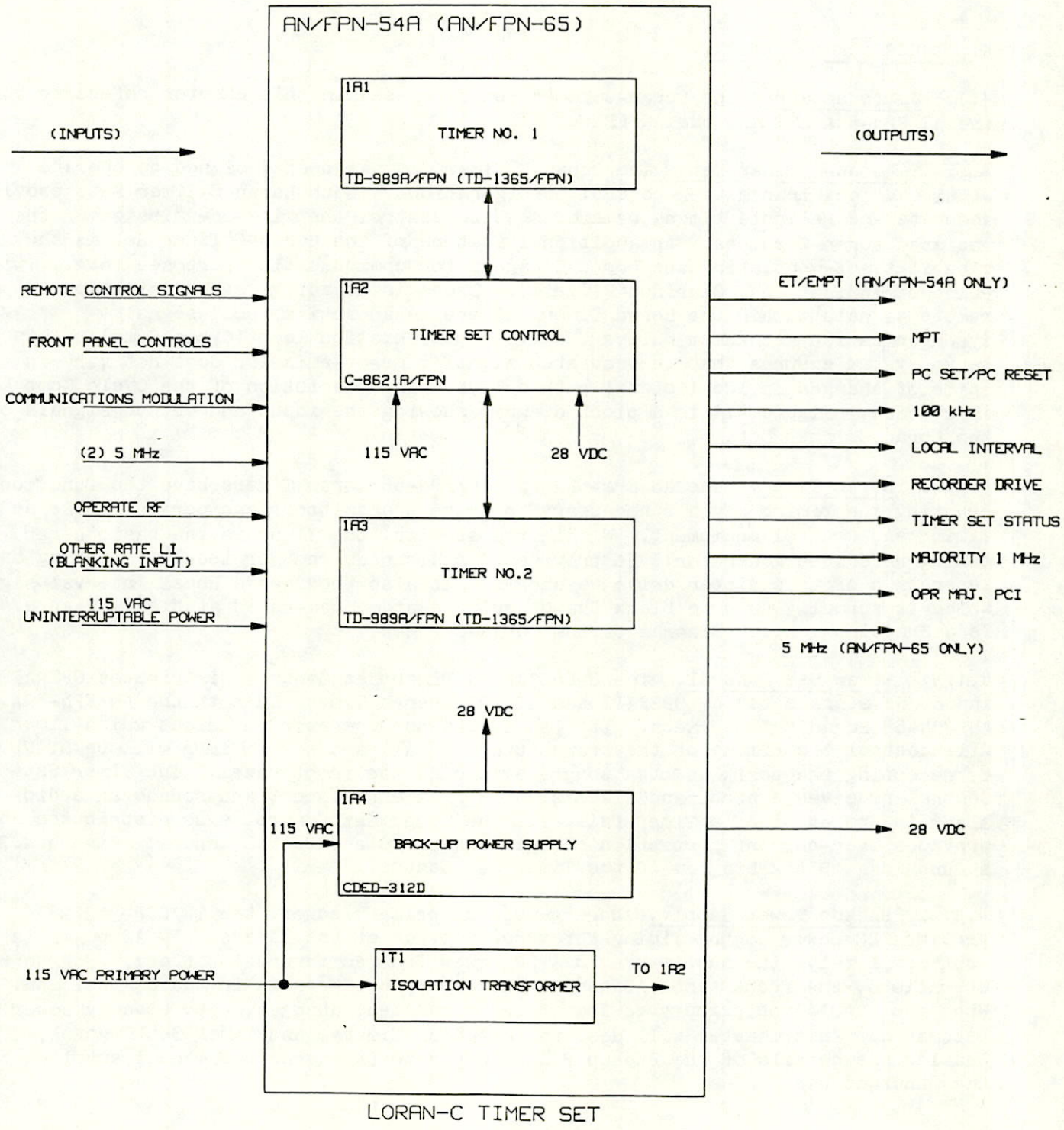


Figure 4.1. Input/Output Signals Of Loran-C Timer Set

has battery power back-up.

1 MHz

E F G P K

LORAN CLOCK CONTROL

The timing of all three DRRG's is monitored. If any single DRRG malfunctions, it is automatically reset to agree with the other two. If no two agree, all three are arbitrarily arbitrarily reset. The majority-vote timing of all three DRRG's and the phase shifter state in the LPA Entry section is checked with the other Timer. Reset of the DRRG's and phase shifter can be commanded from front panel. This section has battery powered back-up.

J

DRRG 1 | DRRG 2 | DRRG 3

CHECK TIMING | RESET TO EXT.

FRONT PANEL DISPLAY AND CONTROL

COMMUNICATION PHASE SHIFT

Enters discrete phase shift, any multiple of 0.2 μs into the 100 kHz for each, or selected,* pulses.

T

Communication Data Entry

ETA ENTRY

Phase shifts the 100 kHz transmitter drive in increments of 0.1 μs. These phase shifts ultimately move the transmitter MPT's in identical increment via reclocking below.

L

100 kHz

100 kHz

Rear Panel Cross-rate Blanking Input

TRIGGER, 5 MHz AND 100 kHz INTERFACE

Reclocks the coarse-timed MPT's to the fine-timed 100 kHz ETA signal. Buffers the 5 MHz output signal. Generates an Early Trigger (ET) at start of Local Interval. Generates Early (ET) and Late (L) fine-timed MPT's. Blanks the MPT's for local station BLINK. Blanks the MPT's for dual-rate interface. Blanks MPT's for LPAs. Blanks the sampling strobes whenever the local signal is blanked. Detects the loss of any drive-signal to the transmitter. Amplifies and impedance matches all transmitter drive signals.

R T

Phase Code
Local Int.
Blink

PCI

1 MHz

100 kHz To Transmitter

MPT's To Transmitter

Local Interval

Phase Code Set

Phase Code Reset

ET + E or LMPT's AN/FPN-54A ONLY

1 MHz

5 MHz AN/FPN-65 ONLY

PCI

NO XMTR DRIVE

5 5

ETA *

FRONT PANEL ETA ENTRY

* ETA dial preset to 0.0 or 0.1 during SSX installation and is not changed thereafter.

Figure 4.2 LORAN-C TIMER Functional Block Diagram

Rear Panel
Remote Blink
Command

LORAN CLOCK AND SIGNAL FORMAT

Three loran clocks or Digital Repitition Rate Generators (DRRG's) maintain time by counting the station's GRI and phase code interval. The DRRG's operate independent of one another, using the input 5 MHz. Majority-vote among the three DRRG's establish the three microsecond sampling strobe for the cycle compensation loop, the local signal phase code, the coarse-timed Multipulse Triggers (MPT's) and the Local Interval waveform.

The Blink code generator develops master and secondary blink waveforms on 12 second time base locked to the 5 MHz oscillator signal. The blink waveforms are synchronized to the local signal MPT's

The LPA entries which phase shift the 5 MHz to the counters likewise shift timing of all

Sample Strobes

MPT's

Phase Code
Local Int.
Blink

5 MHz

TRANSMITTER INTERFACE

CYCLE COMPENSATION SERVO

Position of antenna current third cycle zero crossing is measured with respect to center of 3 µs sampling strobe. If antenna current deviates from this postiion, output 100 kHz phase shifted until zero crossing is centered. This section forms a Type 1 servo loop or regulator which phase locks the antenna current to the center of 3 µs sampling strobe, the loop set point.

M N

Antenna Current Sample

Sample Inhibit

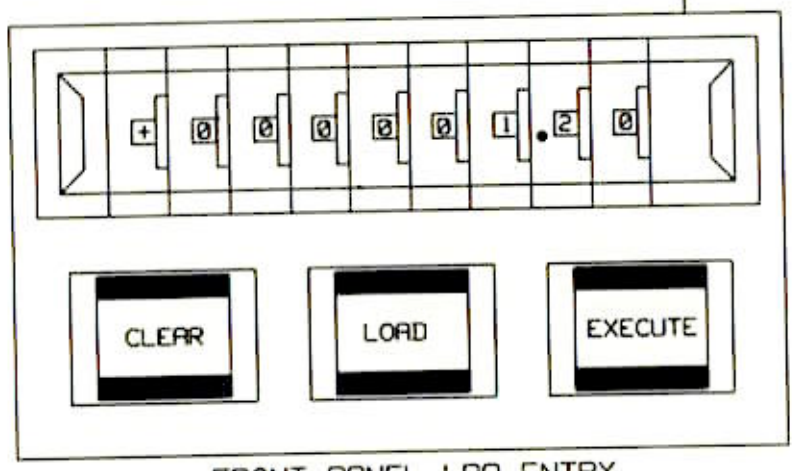
100 kHz

Rear Panel

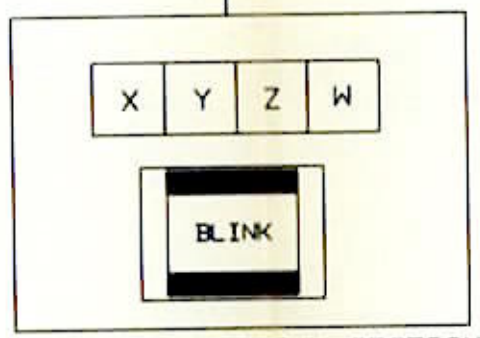
(For AN/FPN-65, MPT's are blanked during execution of an LPA).

B | C | D

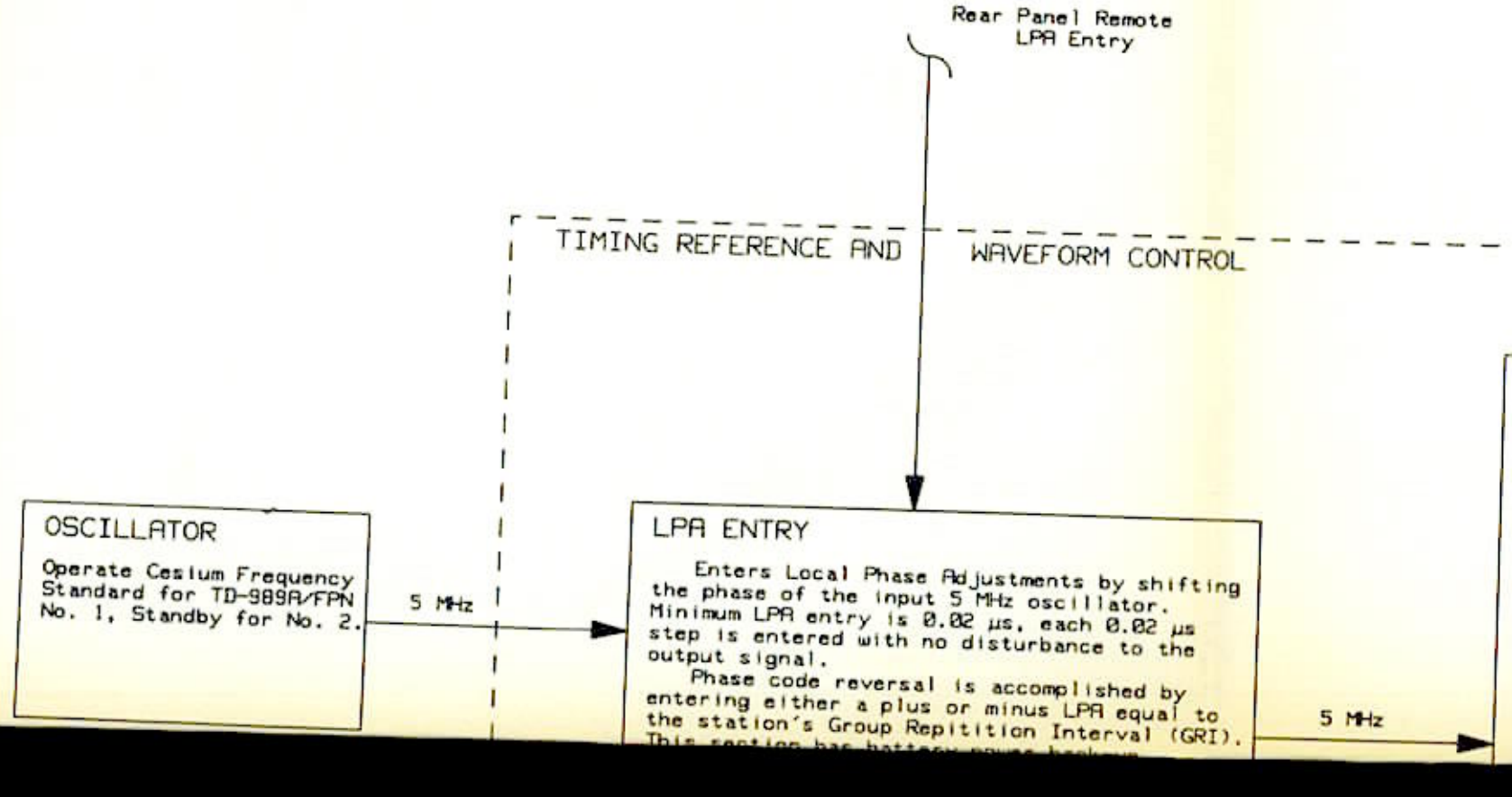
Reset To External



FRONT PANEL LPA ENTRY



FRONT PANEL BLINK SECTION


Rear Panel Remote
LPA Entry
TIMING REFERENCE AND
WAVEFORM CONTROL
OSCILLATOR
Operate Cesium Frequency Standard for TD-989A/FPN No. 1, Standby for No. 2.
5 MHz
LPA ENTRY
Enters Local Phase Adjustments by shifting the phase of the input 5 MHz oscillator. Minimum LPA entry is 0.02 µs, each 0.02 µs step is entered with no disturbance to the output signal.
Phase code reversal is accomplished by entering either a plus or minus LPA equal to the station's Group Repitition Interval (GRI).
5 MHz

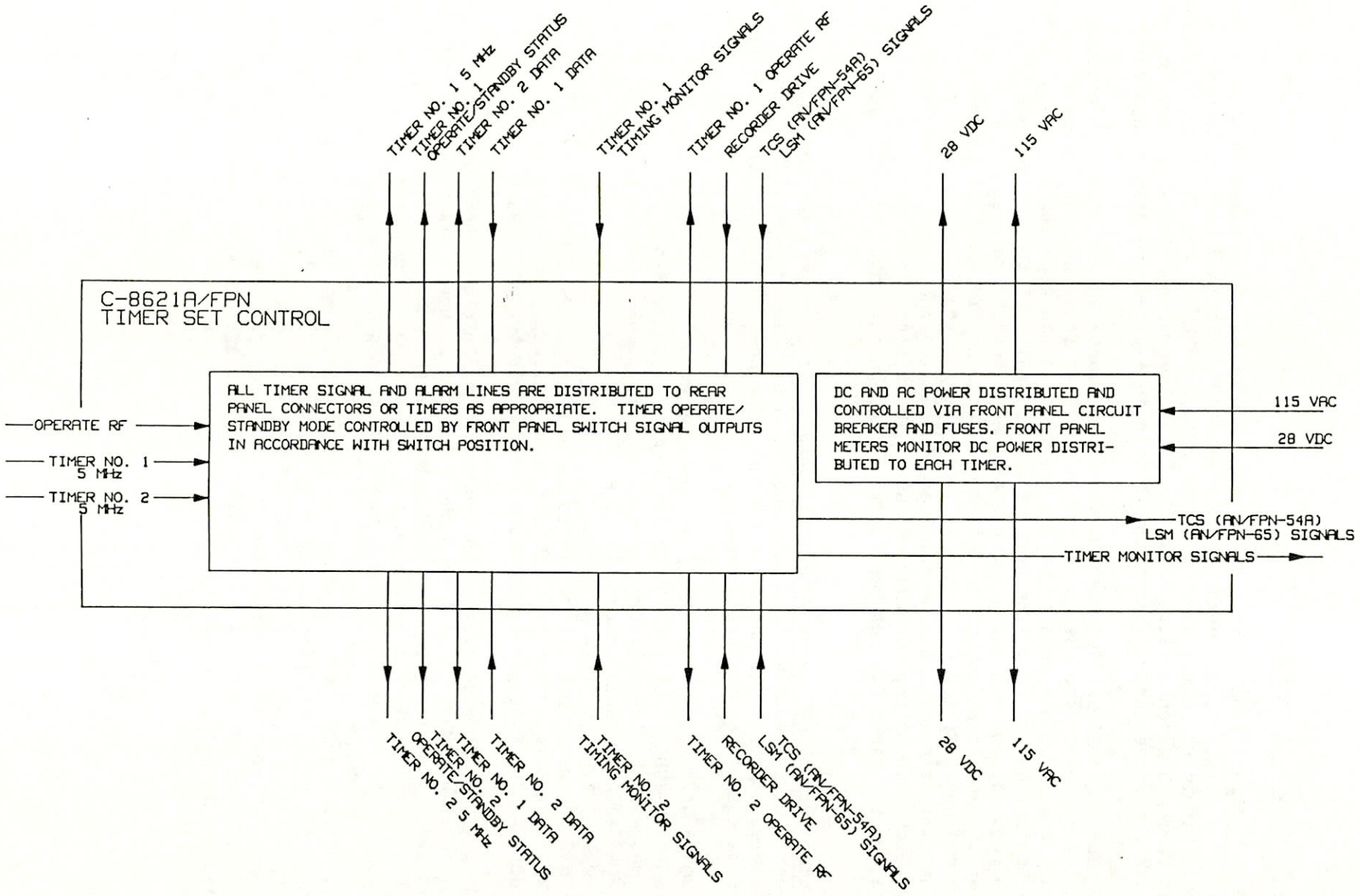


Figure 4.3. Timer Set Control Functional Block Diagram

4.2. Functional Description.

4.2.1. Loran Timer. The Loran-C Timer can be functionally divided into two general subsystems: a fixed time reference subsystem, and a variable time reference subsystem. Within the fixed time reference subsystem there are two major sections: the Loran Timing Reference section and the Control Waveform Generator section. The Transmitter Interface section comprises the variable time reference subsystem.

4.2.1.1. The Loran Timing Reference section represents the "heart" of the Timer. This section may be termed the Loran "clock" because it divides the 5-MHz input from an external frequency standard to obtain the local Group Repetition Interval (GRI), thereby, keeping Loran time. The precise time position of the Loran Timing Reference section represents the local phase zero crossing reference. The succeeding two sections (Control Waveform Generator and Transmitter Interface) condition the Loran Timing Reference data to generate the proper Loran signal format, and maintain a fixed time relationship between the Timer and the transmitter output, thereby, adjusting for changes in the local signal path delay. Additionally, the Timer Set has been designed to accept remote control via 1A1J3 and 1A3J3.

4.2.2. Loran Timing Reference Functional Description. The Loran Timer has independent, triply redundant Digital Repetition Rate Generators (DRRGs) to guarantee time stability of the loran timing reference. The Loran Timing Reference section consists of the following modules:

a. WO486-4A/Ø-SHIFT (Phase Shift) module, D card
b. WO486-5A/CDA (local, Coding Delay Adjust) module, B card
c. WO486-5A/CDA (remote, Coding Delay Adjust) module, C card
d. WO486-12A/CONTROL (Control) module, J card
e. WO486-7/PROGRAM (Program) module, H card
f. WO486-3A/DRRG (Digital Repetition Rate Generator) module, E card.
g. WO486-3A/DRRG (Digital Repetition Rate Generator) module, F card.
h. WO486-3A/DRRG (Digital Repetition Rate Generator) module, G card.

Figure 4.4 is the block diagram of the Loran Timing Reference section. The input to this section is a 5-MHz sinewave from the external frequency standard. A control matrix monitors the timing agreement of all DRRGs and generates (by majority agreement), a reset pulse to automatically correct any one DRRG timing error. Whenever no two DRRG modules agree, a reset (developed from the logical "OR" of all three DRRGs' timing reference) is sent to all DRRGs to attempt to establish a majority. If a majority is not achieved, the CHECK TIMING and DRRG 1, 2, and 3 alarm indicators will illuminate. If a majority is achieved, the DRRG 1, 2, and 3 indicators will extinguish and the CHECK TIMING alarm indicator lights until manually reset. Operator intervention is required to ensure synchronization has not been lost. Timing Reference may be modified by local or remote insertion of Local Phase Adjustments (LPAs). The status of DRRG synchronization is displayed via front panel indicators.

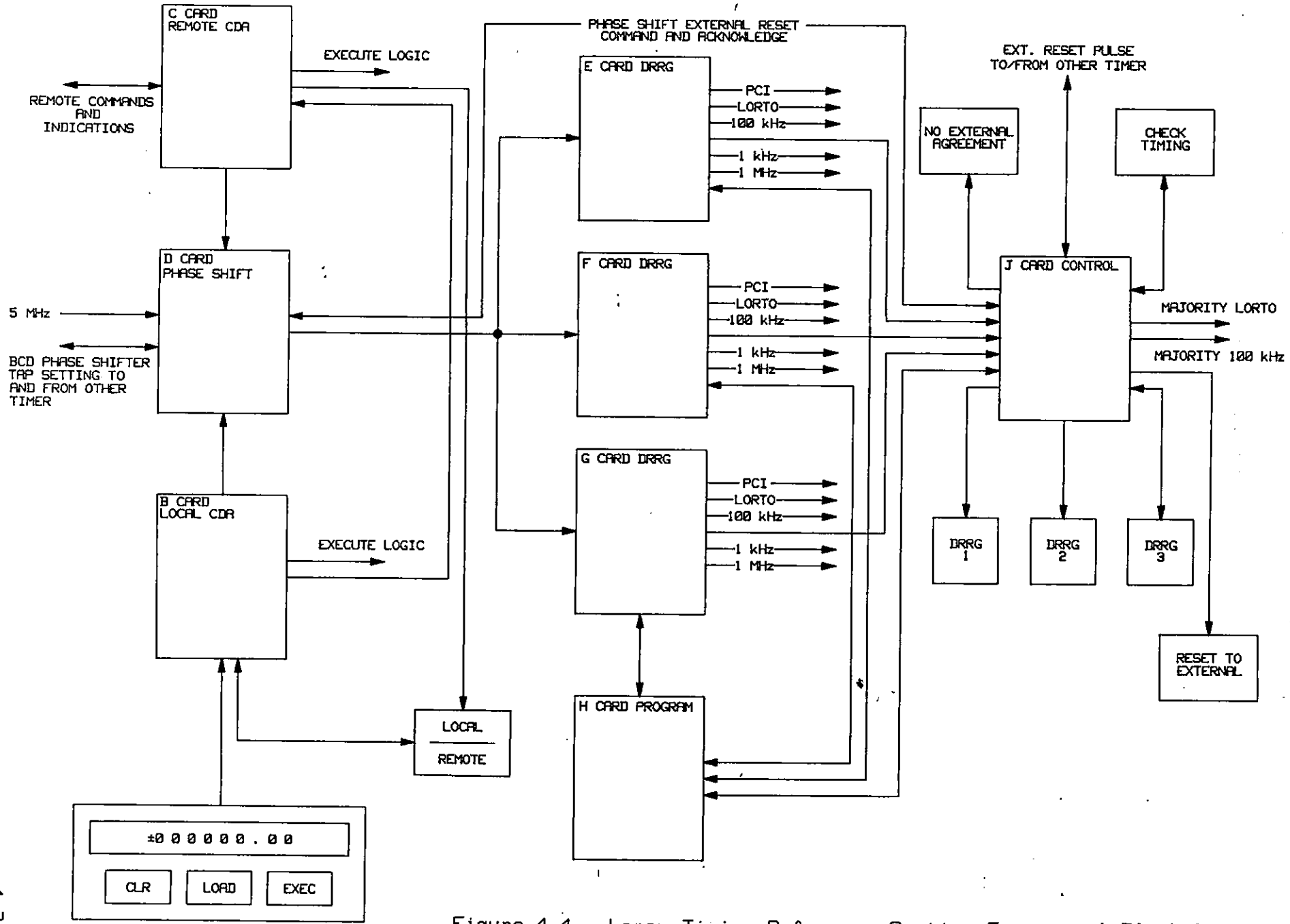


Figure 4.4. Loran Timing Reference Section Functional Block Diagram

4.2.3. Control Waveform Generator Functional Description. The Control Waveform Generator section completes the fixed timing reference portion of the Timer, and consists of the following modules:

a. WO486-30/PC/MPT (Phase Code/Multi-Pulse Trigger) module, K card
b. WO486-6A/BLINK (Blink) module, P card
c. WO486-11/ETA (Envelope Timing Adjust) module, L card

This section generates the required Loran-C transmitter control waveforms from majority agreement of DRRG timing reference, provides local insertion of Envelope Timing Adjustments (ETA) (not used for SSX), and implements BLINK start/stop commands. ETAs are used to adjust the Envelope-to-Cycle Difference (ECD). ECD is the time relationship between the phase of the RF carrier and the time origin of the envelope waveform. The ETA switch does not affect the timing of the emission (i.e., the standard sampling point remains at the same point in time). At dual-rated stations, this section inhibits the generation of certain control waveforms when the other rate's Local Interval blanking signal is connected. The ETA setting and BLINK occurrences are displayed on the front panel. Figure 4.5 is a functional block diagram of the Control Waveform Generator section.

4.2.4. Transmitter Interface Functional Description. The designation, variable timing reference, is used for this section because the timing of the radiated pulses is a function of the cycle comp loop, pulse position modulation (PPM used for loran communications), and various reclocking and timing circuits. The Transmitter Interface section consists of the following modules:

a. WO486-10E/ERR SNS (Error Sense) module, M card
b. WO486-4A/Ø-SHIFT (Phase Shift) module, N card
c. WO486-28B/DRINT/CP (Dual-Rate Interface/Communications Phase Shift) module, T card
d. WO486-8A/INTERFACE (Interface) module, R card

This section provides the necessary signal conditioning and signal amplification to drive the installed Loran-C transmitter. It samples the time position of the local radiated Loran-C pulse, and maintains a fixed time delay between the Timing Reference section signals and the radiated pulse. Figure 4.6 is a functional block diagram of the Transmitter Interface section.

4.2.4.1. An important function in the variable time reference section is the Cycle Comp Loop. The purpose of the Cycle Comp Loop is to control the time of emission of the local signal by keeping it fixed in time with respect to the DRRG timing reference. Because of slight differences between transmitters, and changing impedance characteristics of the antenna system at a Loran station, this requires an active compensation loop. It is necessary that the phase of the radiated signal be fixed in time whether the antenna ground system is covered by snow or is two feet under water. The Cycle Comp Loop works by sampling the radiated signal, hard limiting it, and comparing it with a fixed majority 3 uSec strobe from the ERR SNS module (M card). If the phase zero crossing is centered within the 3 uSec strobe, no correction is necessary. If there is a small phase error, then the Ø-SHIFT module is directed to slew the transmitter drive waveforms in the direction which

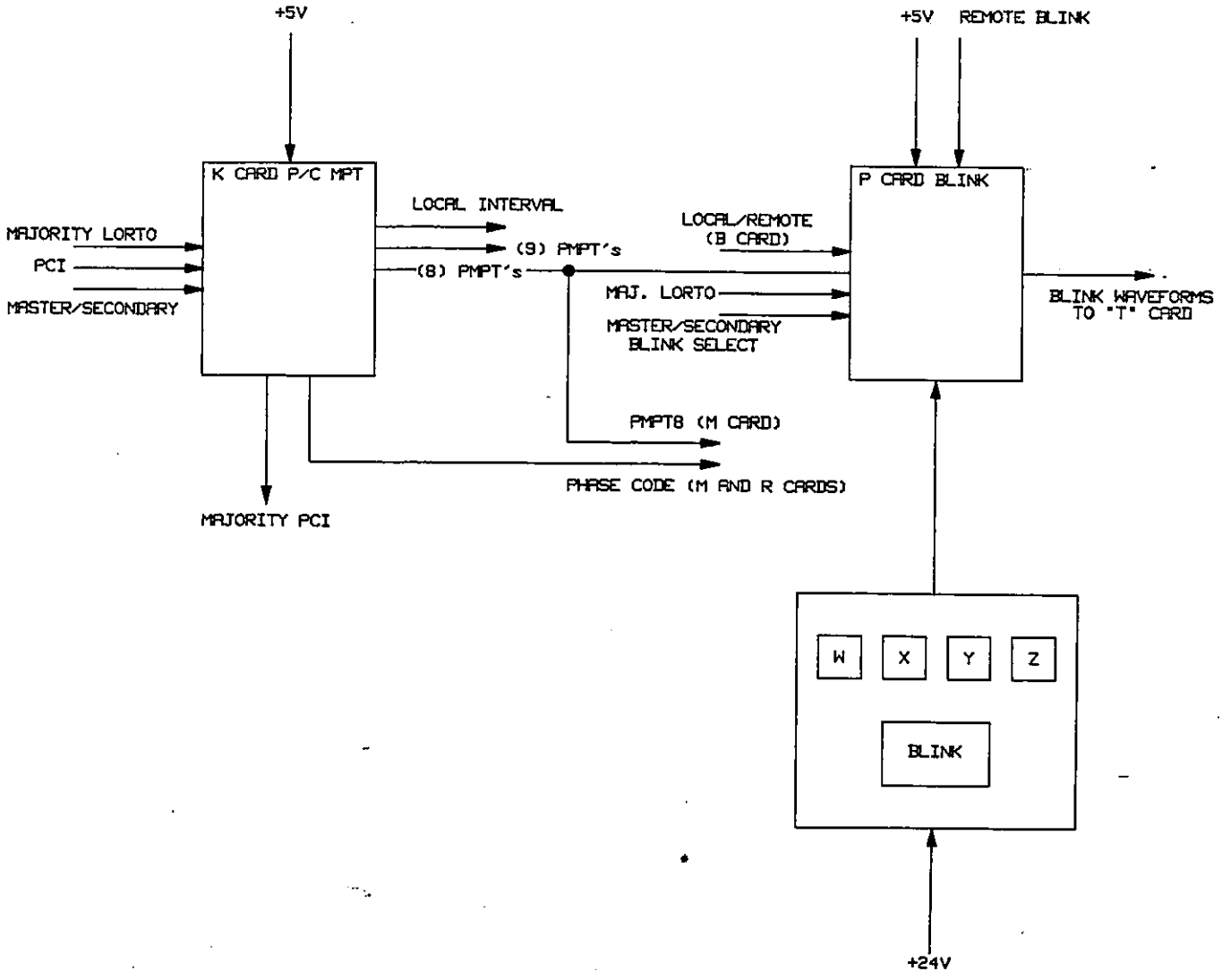


Figure 4.5. Control Waveform Generator Section
Functional Block Diagram

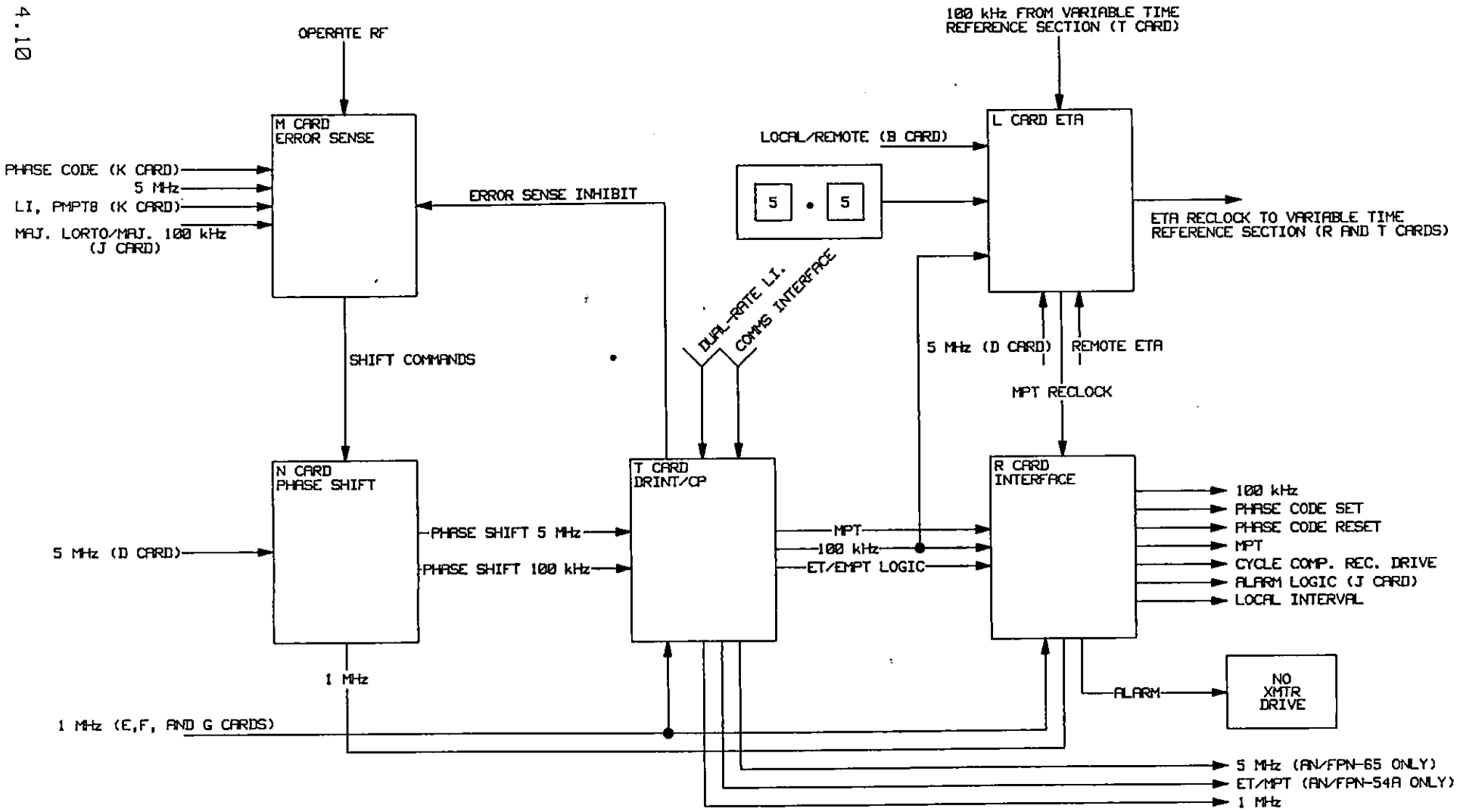


Figure 4.6. Transmitter Interface Section Functional Block Diagram

will remove the error. If there is no hard limited zero crossing within the 3 uSec strobe, the Cycle Comp Loop goes into a super slew mode. A 20 nSec phase shift is ordered every GRI in super slew mode, whereas, in regular or slow slew, a 20 nSec phase shift occurs approximately every 120 GRI.

4.3. Loran Timer Unit Description. In the following discussions of the modules in the Loran Timer, the modules will be referred to by deleting the "WO486-( )/" prefix and by the way they are labeled in the Timer chassis (e.g., Blink module, P card). In the unit descriptions, the modules have been divided into functional sections highlighting major signal flow and corresponding circuits.

4.3.1. Loran Timing Reference Modules Description.

4.3.1.1. WO486-5A/CDA Module (B or C card). There are two CDA modules in each Loran Timer. The B card controls LPA insertions when the Timer is in the LOCAL mode, while the C card controls LPA insertions when the Timer is in the REMOTE mode. LOCAL/REMOTE mode selection is performed using the Timer Front Panel LOCAL/REMOTE indicator/switch and is always controlled by the B card. The B card input signals come from the LPA thumbwheel switches, the CLEAR, LOAD, and EXECUTE indicator/switches and the LOCAL/REMOTE indicator/switch. All of these switches are located on the Timer Front Panel. The LPA-related data to the C card do not come from Front Panel switches, but come from a peripheral device called the Remote Control Interface (RCI). In either mode of operation, the minimum non-zero LPA entry is .02 uSec, and the maximum entry is $\pm$999,999.98 uSec ($\pm$9.98 uSec using RCI). The primary outputs of the CDA cards are Slew and Direction signals to the Ø Shift Module (D card) and LOCAL/REMOTE mode information. LOCAL/REMOTE mode information comes from the B card and is transmitted to the C, L, and P cards. The Slew and Direction signals control the amount and direction of LPAs. The following is a description of the sections in the CDA module:

a. Shift Control Logic Section. This section receives control signals from the CLEAR, LOAD, AND EXECUTE indicator switches on the Timer Front Panel. It provides a Start/Stop signal to the Shift Pulse Generator Section that effectively starts and stops an LPA. The LPA is started on receipt of an EXECUTE command, and stopped on receipt of an Overflow signal from the Pulse Counter Section. An LPA can be stopped prematurely on receipt of a CLEAR command. The LOAD command inputs data to the Pulse Counter Section, and provides logic and lamp driver outputs to the Timer front panel. The Shift Control Logic Section also provides appropriate output signals to control the CLEAR, LOAD, and EXECUTE Front Panel indicator/switch lamps.

b. Shift Direction Latch Section. This latch takes its input from the polarity segment of the LPA thumbwheel switch (S99-9). Using this input, it produces the corresponding Direction signal that is sent to the Ø Shift module (D card).

c. Pulse Counter Section. When the Front Panel LOAD command is EXECUTEd, this digital counter is set to the 9's complement of the value indicated on the LPA thumbwheel switch setting. The counter then counts up one count for each shift pulse (Slew signal) received from the Shift Pulse Generator Section. When the counter "overflows" (that is, the correct number of shift pulses have been received for the particular value of LPA involved), an Overflow signal (Terminal Count) is sent to the Shift Control Logic Section.

d. Shift Pulse Generator Section. The operation of this section is controlled by a Start/Stop signal from the Shift Control Logic section. On receipt of the Start signal (when an LPA is EXECUTEd) the Shift Pulse Generator transmits shift pulses (the SLEW signal) at a frequency of 2 MHz to the Pulse Counter Section and the Ø Shift module (D card). The Slew signal causes the Preset Counter to count up from the preset value. When the Preset Counter "overflows", it transmits the Overflow signal to the Shift Control Logic section which, in turn, transmits a Stop signal to the Shift Pulse Generator. The Shift Pulse Generator then stops sending shift pulses to both the Preset Counter and the Ø Shift module (D card). At this point the LPA process is complete.

e. Local/Remote Latch Section. The Local/Remote Latch is controlled by the Timer's Front Panel LOCAL/REMOTE indicator switch. Based on the input signal from that switch, it transmits corresponding LOCAL/REMOTE mode information to the remote CDA module (C card), as well as to the ETA module (L card), and BLINK module (P card). The LOCAL/REMOTE information determines whether the B card or the C card will control LPAs. It also determines whether the ETAs and BLINK commands are controlled by the Timer Front Panel or the RCI. The Latch also provides the signal that controls the lamps in the LOCAL/REMOTE indicator/switch.

4.3.1.2. WO486-4A/Ø-SHIFT Module (D card). There are two Ø SHIFT modules in each Timer. The D card is in the Loran Timing Reference section, and the N card is in the Transmitter Interface section. The modules are identical and interchangeable. The D card receives a 5-MHz input signal from a frequency standard, and functions as a digital phase shifter for LPA commands. It provides various signals to other modules in the Timer. The following is a description of the sections in the Ø-SHIFT module:

a. 5 MHz Squarer Level Converter Section. This section receives a 5-MHz low level sinewave from the frequency standard and converts it into a logic level squarewave that is compatible with digital logic elements. Input overload protection is provided by a limiter circuit. The Squarer section provides a Phase 1 (Ø1) 5-MHz squarewave output to the tapped delay line in the Digital Phase Shifter section.

b. Digital Phase Shifter Section. This section receives a 5-MHz squarewave from the Squarer section, and generates a digital-controlled phase shift of the 5-MHz squarewave determined by the state of a synchronized counter (described below). The digital phase shifter is a ten-tap delay line which generates ten phases of the input 5-MHz signal. Changing the phase shift of the 5-MHz signal is accomplished by selecting taps on the delay line. A synchronized counter selects the delay line tap based on LPA commands received from the Local CDA module (B card) or Remote CDA module (C card), and RESET TO EXTERNAL commands from the Control module (J card). When an LPA is EXECUTEd, shift pulse (SP) and shift direction (SD) inputs are received from either the B or C CDA cards. The selection process is synchronized with the output 5-MHz signal to ensure that no spurious transients occur during phase change. The phase shift is variable in discrete steps of 20 nSec. The phase shifted 5-MHz signal is buffered sufficiently to drive DRRG modules 1, 2, and 3 (E, F, and G cards), as well as the Ø-SHIFT module (N card), the CONTROL module (J card), the ETA module (L card), and the ERR SNS module (M card). This section also sends and

receives delay line tap setting information in BCD format to and from the other Timer. If the two BCD states are in agreement, a "Ø-Shift BCD Agreement" signal is sent to the CONTROL module (J card). If the information is not in agreement, NO EXTERNAL AGREEMENT is illuminated and alarms are sounded. When RESET TO EXTERNAL is depressed, the counter is preset to the BCD state of the other Timer's Ø-SHIFT module.

c. Frequency Divider Section. This section receives the phase shifted 5-MHz signal from the Digital Phase Shifter section. The 5-MHz signal is synchronously divided to produce 1-MHz and 100-kHz waveforms.

4.3.1.3. WO486-3A/DRRG Module (E, F, and G cards). The three Digital Repetition Rate Generator (DRRG) modules (E, F, and G cards) form the heart of the Loran Timing Reference subsystem, and are identical and interchangeable. The DRRG modules are operated in triply redundant mode, with self-checking and correction to provide loran timing stability. The DRRG module is a conventional preset synchronous counter, which divides the 5-MHz signal from the Ø-SHIFT module (D card) to generate the desired Loran-C rate. The actual rate selection programming is done on the PROGRAM module (H card). The DRRG module also generates the Loran Interval Time Zero (LORTO) signal, and sends it to the CONTROL module (J card). The following is a description of the sections in the DRRG modules (E, F, and G cards):

a. Synchronous Six-Decade Divider Section. This section receives the phase shifted 5-MHz output from the Ø-SHIFT module (D card), and generates Phase Code Interval (PCI) and divider reset (LORTO) signals. This is done by using a synchronous six-decade programmable counter. Each decade counter operates in BCD format, and is continuously decoded into its decimal state. Programmable division (i.e., generation of the Loran rate) is done by routing decoded decimal outputs to the DRRG Coincidence Logic Section via the PROGRAM module (H card, see Programming instructions in Chapter 2). The decade counter is reset by using reset coincidence logic which "AND"s selected outputs from the PROGRAM module (H card). The output of the "AND" gate determines the counter reset pulse (LORTO).

b. Coincidence Logic Section. This section monitors the timing agreement of this and one other DRRG module. This is done by the coincidence logic circuit, by logically "AND"ing the reset pulse (LORTO) with the LORTO signal from one other DRRG module. If they are in coincidence, a signal is sent to the CONTROL module (J card). If they are not in coincidence, a signal is sent to the Majority Detector and Reset Section on the CONTROL module (J card) for further processing. This section also divides reset triggers by two, to define phase code interval A and B for Loran-C applications.

4.3.1.4. WO486-7/PROGRAM Module (H card). The PROGRAM module (H card) is a multi-functional programmable printed circuit board that has no active components. Hardwire connections are made on this module which determine the loran repetition interval. The PROGRAM module provides hardwire programming to select the master or secondary blink codes and sends them to the BLINK module (P card). Local Interval Reset and Phase Code Control signals may be programmed for master or secondary operation and are sent to the PC/MPT module (K card).

4.3.1.5. WO486-12A/CONTROL Module (J card). The CONTROL module (J card) is designed for majority type control of DRRG modules (E, F, and G cards). This module has all logic necessary for this control and respective front panel status display. The basic concept of this module is the comparison of three signals representing the agreement of the three DRRG modules taken two at a time. Also, external reset logic is provided to synchronize the DRRG modules to an external pulse signal or an external phase shifter. The CONTROL module provides majority LORTO and 100-kHz signals from the three DRRG modules to all system modules. The Majority LORTO signal is sent to the PC/MPT module (K card), and Majority LORTO and Majority 100-kHz signals are sent to the Blink module (P card). If majority timing is lost, the CHECK TIMING indicator will light. Majority LORTO signals from both Timers are compared, as well as the tapped delay line Ø-Shift BCD from the Ø-SHIFT module (D card) of both Timers, and if agreement is lost, the NO EXTERNAL AGREEMENT indicator will light. When agreement is lost, it may be regained by depressing the RESET TO EXT switch on the front panel. This enables an internal clock to provide clock pulses to the Ø-SHIFT module (D card) to preset it to the external BCD. The following is a description of the sections in the CONTROL module (J card):

a. Internal Majority Detection and Reset Section. This section contains DRRG error logic that combines loss of coincidence signals from the three DRRG modules (E, F, and G cards) to determine which DRRG module has malfunctioned or that no two of the DRRG modules agree (no majority condition). DRRG modules are reset arbitrarily to the next occurring reset pulse (LORTO), if no majority exists (e.g., if DRRG 1 module (E card) malfunctions, then the DRRG 1 Front Panel lamp lights, and this section provides a majority reset signal to reset the faulty DRRG). This section also receives Interval LORTO signals from the three DRRG modules (E, F, and G cards). The LORTO majority gate provides a Majority Interval LORTO pulse that occurs once per PCI. The Majority Interval LORTO signal is sent to the other Timer, and it functions as a reset operation that corrects phase code jumps, as well as time jumps among the DRRG modules. This section receives error logic signals from the DRRG modules (E, F, and G cards) and signals from the External Agreement Detector and Reset Section of this module to select individual DRRG reset pulses or a No Majority reset pulse. The No Majority reset circuit is inhibited the appropriate amount of time to allow the DRRG pulse loss indicators to determine if a majority agreement has been achieved. At the end of the allotted time period, another reset attempt will be made if the No Majority condition persists. This section receives standard frequency squarewave 100-kHz signals from the three DRRG modules. These signals are sent to a majority gate that generates local majority 100-kHz signals and sends them to the ERROR SENSE module (M card).

b. External Agreement Detection and Reset Section. This section provides Reset to External logic. This logic receives signals from the front panel, remote interface, and Ø-SHIFT module. These signals will slew an internal phase shifter to agree with an external phase shifter, and reset the dynamic DRRG elements. Actuation of the front panel RESET TO EXTERNAL switch, enables the phase shifter reset mechanism. This output inhibits the DRRG dividers until the 5-MHz clock and the external Interval Majority LORTO signal produces a reset pulse. The divider is re-started precisely in time with the local 5-MHz signal, and coarsely timed to the external Majority pulse. The external agreement logic determines if the local LORTO signal agrees with the external LORTO signal. In the event that no local majority exists,

all external reset logic is inhibited to prevent cold start lockup between two timing systems. The External Agreement circuitry in this section receives External Majority LORTO from the other Timer and External Ø-Shifter agreement from the Ø-SHIFT module of this Timer to determine if the local LORTO agrees with the external LORTO. The results of the agreement logic are sent to the front panel indicators.

4.3.2. Control Waveform Generator Modules Description.

4.3.2.1. W0486-30/PC/MPT Module (K card). This module generates Phase Code (PC), Multipulse Triggers (MPTs), and Local Interval (LI) waveforms. These timing waveforms format Master or Secondary pulse groups with programmable delays. This module may be used with either vacuum tube or solid state transmitter by using the TUBE/SSX switch (S-4) on the printed circuit board. Three thumbwheel switches (S-1, S-2 and S-3) located on the printed circuit board are used to set the delay from the Coarse MPT to the location of the Reference Select Gate (TP4, Blue on the ERROR SENSE module, M card). The following is a description of the sections on the 30/PC/MPT module:

a. 1 kHz Majority Selector Gate Section. This section receives Phase 5 and Phase 9 inputs from three DRRG modules (E, F, and G cards) to form Majority Phase 5 and Majority Phase 9 signals. This section has a single pole double throw TUBE/SSX switch (S-4). When in the "TUBE" position, a multiplexer sends Majority Phase 5 and Majority Phase 9 signals to the Phase Code Generator Section. When switch (S-4) is in the "SSX" position, the Majority Phase 5 and Majority Phase 9 signals are interchanged, delaying the PMPT by 400 uSec.

b. 5 MHz Oscillator Section. This section has a 5-MHz crystal controlled oscillator that is asynchronous with respect to the system 5-MHz frequency standard. This section provides 5 MHz to the counter chain logic in the Reference Strobe Generator Section.

c. Phase Code Generator Section. This section receives Majority Phase 5 and Majority Phase 9 signals from the 1 kHz Majority Selector Gate Section. These signals are used to clock PMPT9 and positive LI and negative LI signals as outputs to the DRINT/CP module (T card). This section contains a waveform control PROM and also receives the following inputs:

(1) TUBE/SSX signal from switch (S-4) in the 1 kHz Majority Selector Gate Section.

(2) Majority PCI signal from the PCI Majority Selector Gate Section.

(3) MASTER/SECONDARY signal from the PROGRAM module (H card).

(4) Delayed PMPT8 signal from the counter chain in the Reference Strobe Generator Section.

The waveform control PROM has the following outputs:

(1) An MPT Gate Control signal is combined with Majority Phase 5 or Majority Phase 9 signals from the 1 kHz Majority Selector Gate Section to develop the PMPT9 signal. The PMPT9 signal is sent to the DRINT/CP module (T card).

(2) A Local Control signal is sent to the Local Interval generator in this section. Positive LI and negative LI signals are developed and sent to the DRINT/CP module (T card). A LORTO signal from the CONTROL module (J card) triggers the start of LI.

(3) A Phase Code Latch signal is clocked by the counter chain logic in the Reference Strobe Generator Section to develop Phase Code (PC) signals. Both positive PC and negative PC signals are developed and sent to the ERROR SENSE module (M card).

(4) A PMPT8 Gate Control signal is combined with counter chain logic signals from the Reference Strobe Generator Section to develop the PMPT8 signal. The PMPT8 signal is sent to the ERROR SENSE module (M card).

d. Reference Strobe Generator Section. This section has a counter chain that is clocked with 5 MHz from the 5-MHz Oscillator Section. The counter chain sets the delay from PMPT9 to PMPT8 by programming thumbwheel switches (S-1, S-2, and S-3 on the 30/PC/MPT module). The switches are read from top to bottom in microseconds: the top thumbwheel switch (S-3) sets the hundreds digit, the next switch down (S-2) sets the tens digit, and the bottom switch (S-1) sets the units digit. This delay was previously controlled by R13 and A5 on the ERROR SENSE module (M card). The digitally generated delay of the 30/PC/MPT module is locked to the same time base (DRRG) as the 3 uSec Reference Strobe. There is no temperature dependence, therefore, the 1 uSec resolution provided is sufficient for stable Reference Gate selection. When the counter state agrees with the state of the thumbwheel switches, an output pulse is sent to the Phase Code Generator Section, and can be varied from 1 to 800 uSec in 1 uSec steps. The counter chain also sends control signals to the Phase Code Generator Section.

e. PCI Majority Selector Gate Section. This section receives PCI signals from the three DRRG modules (E, F, and G cards). It develops a Majority PCI signal and sends it to the control PROM in the Phase Code Generator Section. A Majority PCI signal is also sent to the DRINT/CP module (T card).

4.3.2.2. WO486-11/ETA Module (L card). The Envelope Timing Adjustment Control module (L card) generates a 100-kHz pulse train that is synchronized to the 100-kHz signal from the DRINT/CP module (T card). The output pulse train is offset an integral number of 100 nSec increments as indicated by the front panel ETA thumbwheel switches. These thumbwheel switches directly control the position of the transmitter trigger by delaying the trigger from 0.0 through 9.9 uSec in 100 nSec increments. The output of the module is sent to the INTERFACE module (R card) as a reclock multipulse trigger. The following is a description of the sections in the ETA module (L card):

a. Local/Remote Select Gate Section. This section receives Envelope Timing Adjustment (ETA) control signals from the Timer front panel. These control signals are the 9's complement of the strobe delay in BCD format selected from the front panel ETA thumbwheel switch or J3 (Remote Input). The select gates in this section act as an eight-pole double throw switch, and send the desired delay (in microseconds) to the Preset Counter Section.

b. Preset Counter Section. This section has two BCD counters that receive ETA control signals from the Local/Remote Select Gate Section. The BCD counters are preset to the 9's complement of the desired delay (in 0.1 increments), and enabled by a preset pulse from the Majority Gate and Preset Pulse Generator Section. The Preset Counter Section then provides Coarse Strobe Start and Fine Strobe Start signals to the Reclock Strobe Generator Section. Coarse and Fine Strobe width control are selected by making the appropriate Timer backplane jumper connections, and these inputs are also sent to the Reclock Strobe Generator Section.

c. Majority Gate and Preset Pulse Generator Section. This section combines communications shifted 100-kHz signals from the DRINT/CP module (T card), and a phase shifted 5-MHz signal from the Ø-SHIFT module (N card) to produce a 100 nSec preset pulse. This section then generates a 0.1 uSec pulse that is synchronous with the internal 10-MHz clock output of the 10-MHz Clock Section, and sends a counter preset pulse signal to enable the BCD counters in the Preset Counter Section.

d. Reclock Strobe Generator Section. This section receives Coarse Strobe Start, Fine Strobe Start, and Coarse and Fine Strobe Width signals from the Preset Counter Section. The Coarse and Fine Strobe signals are combined to send MPT reclock signals to the Interface module (R card). Delayed 100 nSec TRUE/FALSE strobes are also available as an output of this section.

e. 10 MHz Generator Buffer Section. This section doubles the frequency of the input 5-MHz squarewave from the Ø-SHIFT module (N card). The resulting 10 MHz pulse train provides a 0.1 uSec resolution clock pulse to the BCD counters in the Preset Counter Section.

4.3.2.3. W0486-6A/BLINK Module (P card). The BLINK module (P card) generates coarse timed blink waveforms for both master ninth pulse blink and secondary first two pulse blink. These waveforms are generated by a shift register and repeat every 12 seconds. Each one second period is resolved into alternating 0.2 and 0.3 seconds segments, and these segments are used to define the respective ON or OFF blink periods. The following is a description of the sections in the BLINK module:

a. Blink Code Generator Section. This section receives a majority 100-kHz signal from the CONTROL module (J card), and is divided to generate an internal 2 Hz clock. This output is asymmetric (40% duty cycle) and defines 0.2 and 0.3 second intervals of the basic 0.5 second clock period. The 2 Hz clock signal is processed by a time base shift register to generate the blink time base. This section also receives blink commands from either the front panel controls or the RCI. The blink commands are encoded with the blink time base logic to generate coarse timed blink waveforms for both master and secondary operation. This output is sent to the Master/Secondary Matrix Section.

b. Blink Code Synchronizer Section. This section receives master or secondary program instructions from the PROGRAM module (H card). It has a binary counter that is clocked by MPTs from the PC/MPT module (K card) and cleared by each Majority LORTO input from the CONTROL module (J card). The counter counts multipulse triggers to determine second or eighth triggers for secondary or master operation respectively. Using these signals, this section generates blink synchronizing waveforms, and sends them to the Master/Secondary Matrix Section the appropriate time during ninth pulse transmission for master operation or first two multipulse transmission for secondary operation.

c. Master/Secondary Matrix Section. This section receives a counter reset pulse from the Blink Code Generator Section, and a control waveform signal from the Blink code Synchronizer Section. These waveforms are clocked with the coarse timed blink waveform from the Blink code Generator Section for both master ninth pulse blink and secondary first two multipulse blink. The output of this section (and the BLINK module, P card) is a blink pulse that inhibits MPTs in the correct sequence for a master or secondary station. The blink inhibit signal is sent to the DRINT/CP module (T card), and also controls the BLINK indicator light on the front panel.

d. Blink Lamp Driver Section. This section provides buffer logic to drive Front Panel BLINK indicators.

4.3.3. Transmitter Interface Modules Description.

4.3.3.1. W0486-28B/DRINT/CP Module (T card). The DRINT/CP module (T card) performs the functions of Cross-Rate blanking and interfacing communications equipment (e.g., Two Pulse Communications). At dual-rated stations, the DRINT/CP uses local interval from the other rate Timer to inhibit EMPTs and MPTs during rate coincidence and also generates an Error Sense inhibit waveform for cycle compensation. For communication purposes, it receives a 5-MHz and 100-kHz signals from the Ø-SHIFT module (N card), uses a divider circuit to obtain a 100-kHz signal, and phase-shifts this signal in response to commands from a communications modulator. The shifted 100-kHz signal is then sent to the ETA module (L card) and the INTERFACE module (R card). The following is a description of the sections in the DRINT/CP module (T card):

a. Digital Phase Shifter Section. This section receives phase-shifted 5-MHz and squarewave 100-kHz signals from the Ø-SHIFT module (N card), and advances or retards the 100-kHz and, hence, the reclocked multipulse triggers to the transmitter. The phase-shifted 100-kHz signal can be modulated $\pm$4.8 uSec in 0.2 uSec increments as determined by BCD communications data from the Communications Interface Connector, A3J2. The Phase Shifter logic is reset by a pulse from the Guard Window Generator Section.

b. Buffer Section. This section receives 5-MHz from the Ø-SHIFT module (N card), Majority PCI from the PC/MPT module (K card), and 1-MHz signals from the three DRRG modules (E, F, and G cards). This section contains terminal posts that may be programmed to send buffered 5-MHz signals (inverted and non-inverted) to the AN/FPN-64A(V) transmitter. A buffered PCI signal is sent to the Communications Interface Connector, A3J2, and buffered inverted 1-MHz signals are sent to the INTERFACE module (R card).

c. Trigger Reclock Section. This section reclocks the PMPT9 signal from the PC/MPT module (K card) to the phase shifted 100-kHz signal from the ETA module (L card), and sends Early Trigger Multipulse Triggers to the Trigger Generator Section.

d. Blanking Waveform Generator Section. This section is not used in either the AN/FPN-54A or AN/FPN-65 Loran Timers. It is incorporated to allow use of the DRINT/CP module in systems using transmitted pulses that are not included in the standard Loran-C format. These added pulses are called supernumerary pulses. This section generates a 400 uSec Local Interval signal corresponding to each supernumerary pulse when triggered by a low going signal on the supernumerary trigger input. This signal is sent to the Trigger Reclock Section.

e. Digital Delay Section. This section receives a 100-kHz signal from the ETA module (L card), and reclocked MPTs from the Trigger Reclock Section. It creates a digital delay in the MPT sequence for interface to the AN/FPN-44 transmitter which requires a delayed trigger for operation of the bias pedestals. The exact digital delay may be programmed from 10-160 uSec.

f. Guard Window Generator Section. This section receives EMPTs and MPTs from the Trigger Reclock Section. It has a cross-rate latch that receives a Local Interval input from the back panel BNC, A3J6. The latch is enabled by a pulse from the Guard Window Generator Section, and is combined with a transmit inhibit signal from the BLINK module (P card). The cross-rate blanking inhibits MPTs and EMPTs, and generates an error sense inhibit waveform to the ERR SNS module (M card) when the other Timer has precedence (during Blink and during Local Interval crossing periods).

g. Trigger Generator Section (AN/FPN-54A only). This section is active for the AN/FPN-54A Loran Timer only. It receives Early Multipulse Triggers from the Trigger Reclock Section, and generates 24 volt, high level triggers in a positive direction for the Early Multipulse Triggers. A negative 24 volt trigger is generated for the Early Triggers when so programmed. This section has terminal posts that allow two onboard programming functions: (1) E16 - E17 and E18 - E19 may be connected to route Early Triggers and Multipulse Triggers to tube type transmitters; and (2) E6 - E11 may be removed for high rate on a dual-rated station.

4.3.3.2. DRINT/CP Module (T card) Programming. See Chapter 2, Installation, Table 2.8, for desired programming on this module. The programming is done by positioning jumpers on terminal posts on the module. These jumpers are used to select either an ET/EMPT output (AN/FPN-54A) or a 5-MHz output (AN/FPN-65). Since the same shielded pair in the Signal Harness is used for both of these signals, only one may be selected. To include an Early Trigger (ET) in the Early Multipulse Trigger output signal, a jumper between E6 and E11 is required. A jumper is required in the AN/FPN-54A, except for the high rate Timer, at dual-rated installations. In the AN/FPN-65, the E6 and E11 jumper has no effect on operation. The delay between Early Multipulse Triggers and Multipulse Triggers is programmed by jumpers between E1 through E4 and E7 through E10 (see paragraph 4.3.3.1.e above and Table 2.8).

4.3.3.3. WO486-4A/Ø-SHIFT Module (N card). The Ø-SHIFT module (N card) is identical to and interchangeable with the Ø-SHIFT module (D card). However, the Ø-SHIFT module (N card) receives its slew and direction commands from the ERR SNS module (M card) instead of the CDA modules (B or C cards). The following is a description of the sections in the Ø-SHIFT module:

a. 5 MHz Squarer Level Converter Section. The Squarer Level Converter Section is not used on the N card because the squarewave 5-MHz input signal is received from the other Ø-SHIFT module (D card), and has already been converted to a squarewave.

b. Digital Phase Shifter Section. This section receives a phase shifted 5-MHz signal from the Ø-SHIFT module (D card) and uses a tapped delay line and synchronized selector to shift the phase of the 5-MHz signal in 20 nSec increments. It sends shifted 5-MHz signals to the DRINT/CP module (T card).

c. Frequency Divider Section. This section synchronously divides and gates the 5-MHz output from the Digital Phase Shifter Section to produce 1-MHz and 100-kHz waveforms. It routes the 1 MHz signal to the INTERFACE module (R card), and routes the 100-kHz signal to the DRINT/CP module (T card).

4.3.3.4. WO486-10E/ERR SNS Module (M card). The Error Sense module (M card) measures the error between an input reference waveform derived from the DRRG majority and the local zero crossing and determines emission delays. The output of the module provides slew and direction commands to the Ø-Shift module (N card). The principle feature of this module is that all measurements are made digitally; there are no analog functions. This results in a system that is essentially immune to temperature or voltage fluctuations. The following is a description of the sections in the ERR SNS module:

a. Hard Limiting Zero Crossing Detector Section. This section receives a direct RF local signal (OPERATE RF) from the SIGNAL HARNESS module (S card), and Phase Code signals (PC and $\overline{PC}$) from the PC/MPT module (K card). The OPERATE RF signal is hard limited by a threshold detector, and the phase code is removed. This section sends a hard limited zero crossing of the local radiated carrier or envelope to the Slew Speedup Servo Section and the Zero Crossing Sensor Section. A limited local RF signal is sent to the Lost Signal Detector Section.

b. Lost Signal Detector Section. This section receives a limited local RF signal from the Hard Limiting Zero Crossing Detector Section. It detects the loss of local signal, and disables operation of the ERR SNS module (M card). Lost signal threshold is nominally 6 db below the normal input level.

c. Reference Select Gate Generator Section. This section receives an MPT signal from the PC/MPT module (K card), Majority 100-kHz strobes from the DRRG modules (E, F, or G cards), and a 5-MHz system clock signal from the Ø-SHIFT module (N card). It generates a reference strobe retimed by the 100-kHz strobes, precisely reclocked by the system 5-MHz clock. A reference strobe is sent to the Zero Crossing Sensor and Slew Speedup Servo sections, and an inverted reference strobe is sent to the Slew Speedup Servo Section.

d. Zero Crossing Sensor Section. This section receives the OPERATE RF zero crossing signal from the Hard Limiting Zero Crossing Detector Section. It has sensing logic that determines the position of the OPERATE RF zero crossing (pulses). The pulses are clocked asychronously (8-MHz clock from the Asynchronous Oscillator Section) with a reference strobe from the PC/MPT module (K card) and input to the Digital Integrator Section.

e. Digital Integrator Section. The digital integrator counts up the number of 8-MHz clock pulses that occur within the gate produced from the leading edge of the reference strobe to the zero crossing, and counts down the number of strobes that occur between the zero crossing and trailing edge of the reference strobe. Depending on the number of strobes counted, an overflow (indicating RF zero crossing is to the right of center), or an underflow (indicating RF zero crossing is to the left of center) is produced and sent to the Integrator Reset Section.

f. Integrator Reset Section. This section receives converter overflow and underflow signals from the Digital Integrator Section. The overflow and underflow information is used to generate slew and direction commands signals. Overflow and Underflow points are jumper programmable to select the cycle compensation loop time constant. These signals are sent to the Ø-SHIFT module (N card).

g. Slew Speedup Servo Section. This section receives hard limited zero crossing RF from the Hard Limiting Zero Crossing Detector Section, and reference strobes (inverted and non-inverted) from the Reference Strobe Generator Section. When the zero crossing is entirely outside of the Reference Strobe, the Digital Integrator Section is bypassed and the servo goes into high speed slew (super slew). This provides worst case time of 35 seconds to decrease cycle comp loop error to within $\pm$1.5 uSec. This section is not active when the zero crossing is within the Reference Strobe and has no effect on the cycle comp loop transient response for errors of less than $\pm$1.5 uSec. When active, advance or retard signals are sent to the Integrator Reset Section. The DRINT/CP module (T card) sends a STROBE INHIBIT signal to the Strobe Generator Section. (see paragraph 4.3.3.2 for discussion).

h. Asynchronous Oscillator Section. This section generates clock pulses at an approximately 8-MHz rate. Ideally, this oscillator output has random timing with respect to the Loran-C time base. The clock pulses are sent to the Zero Crossing Sensor Section.

i. Envelope Detector and Deriver Section. This section is not used, but has the capability to demodulate and filter the envelope of the local signal, and generate a second derivative envelope signal. This signal is buffered and is available to drive an output load.

4.3.3.5. WO486-8A/INTERFACE Module (R card). The INTERFACE module (R card) interfaces logic level waveforms with various external equipment, providing logic level shifting, waveshaping, phase coding, and phase comparison functions for Loran Timer elements. The following is a description of the sections in the INTERFACE module:

a. Transmitter Trigger Reclock Section. This section receives a MPT reclock signal from the ETA module (L card). It reclocks the coarse MPT from the DRINT/CP module (T card) to obtain the MPT waveform. This section generates high level 24 volt zero-to-peak transmitter multipulse triggers used for driving 50 ohm or 100 ohm loads. The reclock MPT signal is sent to the Transmitter Trigger Generator Section.

b. Interval Buffer Amplifier Section. This section receives a Local Interval signal from the PC/MPT module (K card), and buffers the Local Interval waveform for external use such as control of receiver blanking. The buffered LI waveform is sent to the Transmitter Drive Loss Alarm Section of this module and to the SIGNAL HARNESS module (S card) for distribution to external equipment.

c. Early Trigger Generator Section. This section receives an Early Trigger signal from the DRINT/CP module (T card). It generates high level fast rising and exponentially decaying Early Triggers. The output pulse characteristics are nominally 24 V peak amplitude and 3 uSec 50% width into a 100-ohm balanced load. The Early Triggers are not used, nor available, as outputs in the AN/FPN-65 Loran Timer. An Early Trigger Monitor signal is developed in this section and sent to the Transmitter Drive Loss Alarm Section.

d. 100 kHz Phase Coder Shaper Driver Section. This section provides gating and filtering of 100-kHz squarewave input signals from the Ø-SHIFT module (N card). This section uses an RC filter to shape the 100-kHz squarewave input signal into a sinewave signal, the sinewave is then amplified by an operational amplifier. The filtered output is a 100-kHz sinewave capable of driving 15 V P-P into a 50 ohm or 100 ohm load. Since, this section is normally within the cycle comp loop, the propagation delay time is uncritical and is not calibrated. The 100-kHz sinewave output level is adjustable by trimmer R6, and is sent to the SIGNAL HARNESS module (S card). 100-kHz sinewave is also sent to the Transmitter Drive Loss Alarm Section.

e. Phase Code Trigger Generator Sections. These sections receive a Phase Code (PC) signal from the PC/MPT module (K card) and generates high level phase code Set and Reset Triggers. Phase Code Set Trigger signals (PC Set and $\overline{\text{PC Set}}$) and Phase Code Reset Trigger signals (PC Reset and $\overline{\text{PC Reset}}$) are sent to the SIGNAL HARNESS module (S card). PC Set Trigger Monitor and PC Reset Trigger Monitor signals are developed to detect loss of Phase Code Triggers and sent to the Transmitter Drive Loss Alarm Section of this module (R card).

f. Recorder Channel 1 Phase Comparator Section. This section receives 1-MHz signal (Reference) from three DRRG modules (E, F, and G cards), and 1-MHz signal (Variable) from the Ø-SHIFT module (N card) to provide phase comparator function. This section provides an analog output for driving either current or voltage type meters (0 - 5V; 0 - 1 mA), or chart recorders. Recorder DC outputs may be shifted by switch S2, an amount equivalent to 200 nSec for best chart centering. The output DC voltage is proportional to the phase difference between the Variable input from the Ø-SHIFT module (N card) and the Reference (Majority) input from the DRRG modules (E, F, and G cards). The comparator is used to monitor local

compensation loop activity. (NOTE: The INTERFACE module (R card) has a second Phase Comparator Section for Recorder Channel 2.)

g. Transmitter Drive Loss Alarm Section. This section monitors the remaining sections in the INTERFACE module, and indicates loss of any of these outputs by operating a lamp driver and setting a logic level output. It senses loss of 100-kHz output, Local Interval, early triggers, transmitter triggers, or phase code triggers. The output driver of this section provides alarm signals to the front panel indicator.

h. Transmitter Trigger Generator Section. This section receives reclocked MPT signals from the Transmitter Trigger Reclock Section. It then generates reclocked MPT signals and high level transmitter MPT for driving 50 ohm and 100 ohm loads. The trigger generator is inhibited during execution of an LPA entry in the AN/FPN-65.

5. MAINTENANCE.

5.1. Maintenance Philosophy. Organizational-level maintenance is limited to replacing modules, subassemblies, and main-frame components. Backplane wiring and XB designated material shall not be repaired at the unit level. If for any reason, required maintenance to the equipment exceeds the capabilities of the unit level, assistance shall be requested from the next higher organizational level (e.g., Section, Activity, or District Office). All defective XB material is to be returned to the Inventory Control Point (ICP), or as ICP may direct, for depot level repairs in accordance with E/GICPINST 4408.1 series.

5.1.1. This manual contains information for organizational-level maintenance. Allowance Parts List (APL) identification and Electronics Repair Parts Allowance List (ERPAL) support is limited to replaceable modules and subassemblies which are authorized to be replaced locally. XB designated items are listed in the APL without a breakdown of subassemblies or component parts. A complete set of XB modules is provided to the unit for support of this equipment.

5.2. Maintenance Policy. The Inventory Control Point (ICP) designates the maintenance policy which is found in E/GICPINST 4408.1 series.

NOTE

Ensure that proper care is taken while performing any checks, measurements, or adjustments. Improper procedures may cause an OFF-AIR or OUT-OF-TOLERANCE condition.

5.3. Loran Timer Set Preventive Maintenance Schedule.

5.3.1. Introduction. A local maintenance procedure should be developed which follows a logical progression (e.g., switch Timers only one time for routine maintenance) so that station operation is minimally effected.

NOTE

Ensure that all equipment maintenance is done when the Loran Timer is in the STANDBY mode, unless specifically directed to perform maintenance or adjustments to the OPERATE Timer. Follow Clean Timer Switch procedure in paragraph 5.8 when routinely switching Timers.

5.3.2. Weekly Maintenance. The following should be accomplished weekly on both Timers:

a. Front Panel Lamp Test. Refer to paragraph 5.4.

b. Timer Set Equipment Cleaning. Refer to paragraph 5.5.

c. Cycle Compensation Loop Check/Adjustment. Refer to paragraph 5.6.

d. 100-kHz Output Signal Adjustment. Refer to paragraph 5.7.

e. Clean Timer Switch. Refer to paragraph 5.8.

5.3.3. Monthly Maintenance. The following should be accomplished monthly:

a. DRRG Alarm Check. Refer to paragraph 5.9.

b. DC Power Supply Checks. Refer to paragraph 5.10.

c. MPT Movement (ETA Dial) Check (AN/FPN-54A only). Refer to paragraph 5.11.

d. Backup Power Supply CDED-312( ) Check. To insure proper operation, exercise every month by placing the Initiate/Interrupt switch (Item 6 on Figure 3.3) momentarily to the Initiate position. This initiates a discharge cycle of the battery. Voltage will decrease until automatically interrupted. Momentarily placing the switch to the Interrupt position will also stop the discharge cycle.

NOTE

This procedure will result in a temporary loss of back-up capability until battery is fully recharged.

5.3.4. Quarterly Maintenance. Perform the following quarterly:

a. Inspect for frayed, damaged, or broken wires or cables. Repair or replace as necessary.

b. Inspect for broken or corroded ground system connections. Repair or replace as necessary.

c. Inspect the cabinet AC power cable to ensure that it is in good condition.

WARNING

A non-conducting vacuum cleaner nozzle should be used to avoid shock hazard.

CAUTION

Exercise care to avoid damaging components and wiring.

NOTE

At no time should compressed or forced air be used to perform any cleaning or maintenance.

d. When the Timer is in STANDBY mode, pull the chassis out to the chassis slide stops. Clean and vacuum the inside of the Timer as necessary to remove accumulated dust and dirt. Care must be exercised when cleaning near the backplane wiring of the card file.

5.4. Front Panel Lamp Test.

a. On the front panel of the STANDBY Timer, depress the LAMP TEST switch while observing the front panel indicators. Ensure that all lamps respond as indicated in Figure 5.1 (i.e., White/Green for normal operation, Amber for attention, and Red for malfunction). All lamps should illuminate with the exception of the BLINK SELECTION W, X, Y, Z, and OPERATE/STANDBY.

b. On the STANDBY Timer, depress the BLINK SELECTION indicator/switches W, X, Y, and Z, respectively. All four lamps should light and the BLINK indicator should flash. Push W, X, Y, and Z indicator/switches again and all lamps should extinguish.

c. When the other Timer is placed in STANDBY mode for maintenance, perform the front panel lamp test as described above.

d. Place the Timer in STANDBY mode before changing burned out lamps to avoid the possibility of an out-of-tolerance condition. Replace all burned out lamps with Type 387 lamps. The lamp replacement procedure is found in paragraph 5.4.1.

CAUTION
No substitute lamps are permitted. Use of substitute lamps may result in damage to the equipment.

5.4.1. Front Panel Relamping Procedure. To replace any lamp on the Loran Timer Set with the exception of BLINK SELECT W, X, Y, Z, LAMP TEST, and AUDIO ALARM INHIBIT lamps (for relamping procedure of those lamps, see paragraph 5.4.2), refer to Figure 5.2 and proceed as follows:

a. Pull out the appropriate indicator by using fingernail notches provided on the indicator (do not pull on the metal frame).

b. Twist the indicator one quarter turn in either direction. Push in slightly, then pull out until the lamp assembly clears the front panel. Allow the lamp assembly and indicator to swing down on the hinges.

c. Push the plastic hinges towards each other until the hinges clear the tracks. Remove the unit.

d. Install the lamps from the rear of the lamp assembly by pulling the defective lamps straight out and pushing the new lamps straight in. Replace colored plastic caps on new lamps.

e. Install the unit by reversing the above procedure. Note, that when installing the unit, before rotating one quarter turn, it is not necessary to pull out slightly. Simply push in hard enough so that little effort is required to rotate the unit.

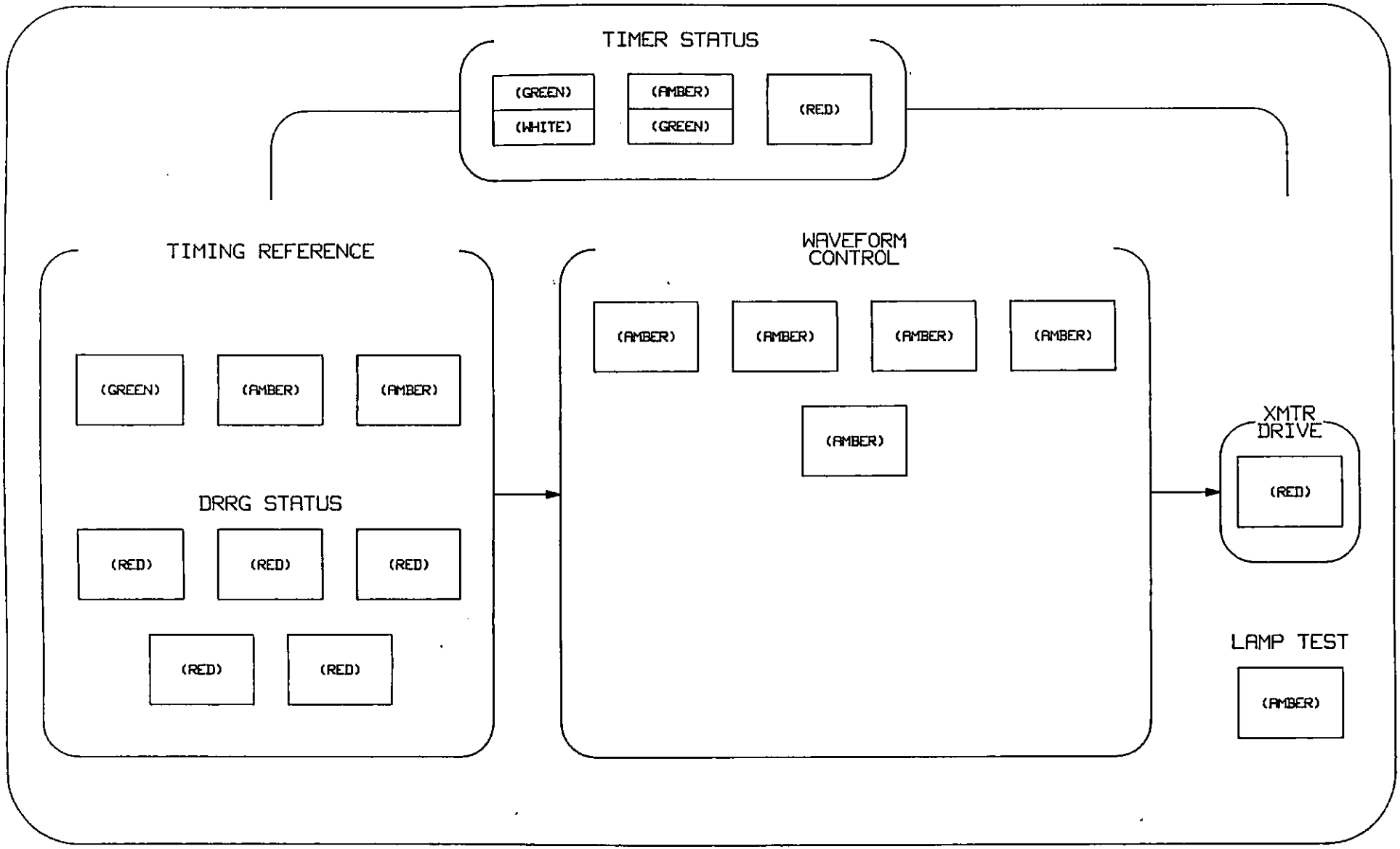


Figure 5.1. Loran-C Timer Front Panel Lamps

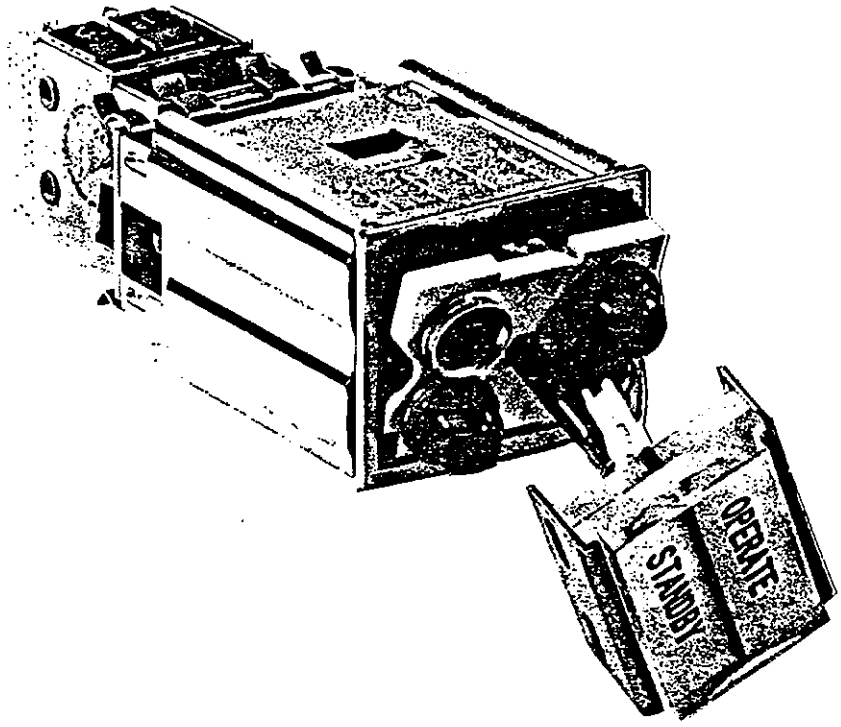


Figure 5.2. Front Panel Lamp Assembly

5.4.2. To relamp the BLINK SELECT W, X, Y, Z, LAMP TEST, and AUDIO ALARM INHIBIT lamps, use the following procedure:

a. Follow the procedures outlined in sections 'a' and 'd' of paragraph 5.4.1 above.

b. To install the unit after replacing the lamp, simply push the assembly into position.

5.5. Timer Set Equipment Cleaning. Clean the Loran Timer Set as follows:

a. Clean and dust the outside of the equipment cabinet.

b. Vacuum or clean the bottom of the equipment cabinet.

WARNING

A non-conducting vacuum cleaner nozzle should be used to avoid shock hazard.

CAUTION

Exercise care to avoid damaging components and wiring.

NOTE

At no time should compressed or forced air be used to perform any cleaning or maintenance.

5.6. Cycle Compensation Loop Check/Adjustment.

5.6.1. This procedure ensures that the Timer is sampling the proper zero crossover point, and that both Timers are sampling the same zero crossover point.

5.6.2. This adjustment procedure is performed in two steps. Step 1 is the "Coarse Adjustment", and step 2 is the "Fine Adjustment".

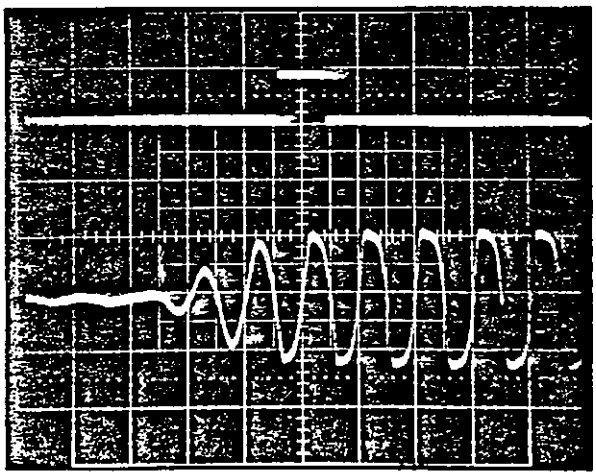
a. All test points are located on the ERR SNS module (M card) and all adjustments are performed on the 30/PC/MPT module (K card).

NOTE

This adjustment is performed only on the STANDBY Loran Timer. An OUT-OF-TOLERANCE condition may occur if the adjustment is done to the OPERATE Timer.

b. Ensure that all front panel indicators on the Timer are normal and that the transmitter is radiating a correct Loran signal. The Cycle Comp Reference Strobe is inhibited whenever the local signal is absent (below 5 Vp-p).

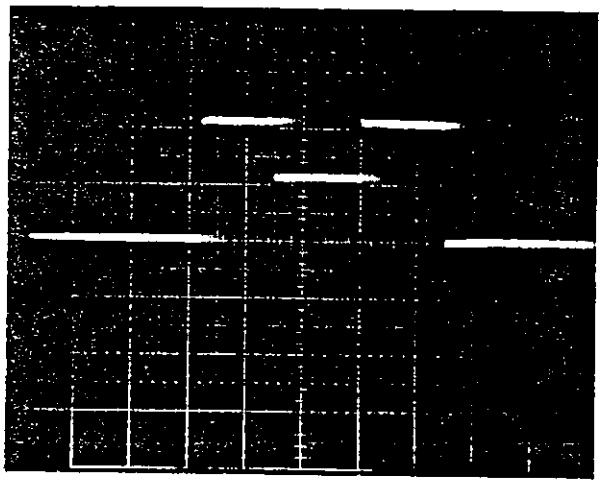
c. Coarse Positioning of the Reference Strobe. Using a calibrated dual trace oscilloscope with X10 probes, monitor the Reference Select Gate (8 uSec pulse, channel A) and the Buffered Local Signal (channel B) waveforms as shown in Figure 5.3. Adjust thumbwheel switches S1, S2, and S3 on the 30/PC/MPT module (K card) to achieve coarse positioning of the Reference Select Gate as shown in Figure 5.3. Ensure that the Reference Select Gate is centered on the third positive zero crossover point and not the second or fourth. Care must be exercised when determining which crossover is being used.



SIGNAL AND SOURCE	SETTINGS
	TRIGGER:
Channel A: TP4 (Blue) ERROR SENSE Module (M) Reference Select Gate	(-) External
Channel B: TP2 (Orange) ERROR SENSE Module (M) Limited Operate RF	MODE: Delayed Sweep
Trigger: TP7 (Red any DRRG Module (E,F,G)	HORIZONTAL: 10 uSec/Div (Main Sweep 0.5 ms/Div)
	VERTICAL: 5 V/Div

Figure 5.3. Coarse Positioning of the Reference Strobe

d. Fine Positioning of the Reference Select Gate. Connect an oscilloscope as shown in Figure 5.4. Bracket the Reference Strobe with the Reference Select Gate, and use the adjustment thumbwheel switch S1 on the 30/PC/MPT module to achieve fine positioning of the Reference Select Gate (8 uSec pulse) so that the Reference Strobe (3 uSec pulse) is located approximately in the center of the Reference Select Gate as shown in Figure 5.4.



SIGNAL AND SOURCE	SETTINGS
	TRIGGER:
Channel A: TP5 (Yellow) ERROR SENSE Module (M) Reference Strobe	(-) External
Channel B: TP4 (Blue) ERROR SENSE Module (M) Reference Select Gate	MODE Delayed Sweep
Trigger: TP7 (Red any DRRG Module (E,F,G)	HORIZONTAL: 2 uSec/Div (Main Sweep 0.5 ms/Div)
Channel A & B, ADDED	VERTICAL: 2 V/Div

Figure 5.4. Fine Positioning of the Reference Strobe

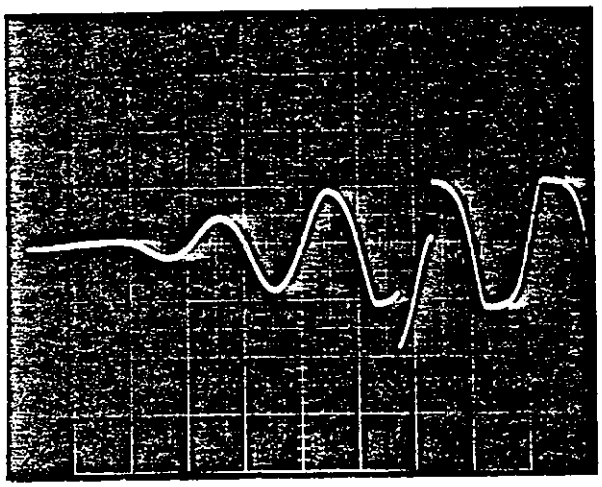
e. It is imperative that both Timers be adjusted to track at the same zero crossing. Perform a clean Timer switch. A small error, due to phase modulation, may have to be removed by inserting LPAs if the now STANDBY Timer Reference Select Gate has been changed to a new zero crossing point. Connect an oscilloscope as shown in Figure 5.5 to the now OPERATE Timer. Allow sufficient time for the Cycle Comp on the OPERATE timer to settle (approximately five minutes). View the waveform on the oscilloscope (Figure 5.5) and ensure that the Reference Strobe is in fact sampling the third positive zero crossover point. Correct the Cycle Comp adjustment on the now STANDBY Timer as outlined above. Perform a clean Timer switch to return to original configuration. When the Cycle Comp adjustment is made after replacement of a failed module (ERR SNS or 30/PC/MPT), the adjustment should be checked approximately two hours, and again twenty-four hours after the installation, to verify stable operation.

5.7. 100-kHz Output Signal Adjustment. This adjustment should be done when the Timer is in the OPERATE mode due to the effects of loading. Perform the following steps to adjust the 100 kHz signal output:

a. Connect an oscilloscope as shown in Figure 5.6, and adjust potentiometer R6 on the INTERFACE module (R card) to obtain a peak-to-peak signal of 12 volts $\pm$ 0.1 volts.

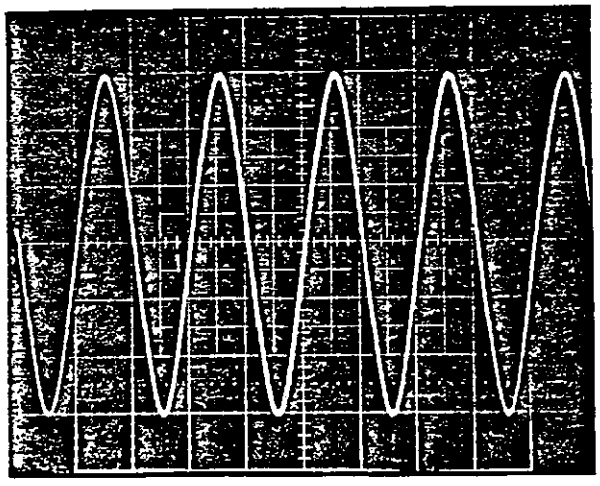
NOTE

It is imperative that both Timers be adjusted to the same level, otherwise Transmitter Drive Waveform amplitude changes may occur during Timer switches.



SIGNAL AND SOURCE	SETTINGS
	TRIGGER:
Channel A: TP5 (Yellow) ERROR SENSE Module (M) Reference Strobe	(-) External
Channel B: TP2 (Orange) ERROR SENSE Module (M) Limited Operate RF	MODE Delayed Sweep
Trigger: TP7 (Red any DRRG Module (E,F,G) Channel A & B, ADDED	HORIZONTAL: 5 uSec/Div (Main Sweep 0.5 ms/Div)
	VERTICAL: 2 V/Div

Figure 5.5. Reference Strobe Sampling Point



SIGNAL AND SOURCE	SETTINGS
	TRIGGER:
Channel A: TP1 (Red) INTERFACE Module (R) 100 kHz	(-) Internal
Ground Reference is center line	MODE Main
Nominal level is 12 Vp-p	HORIZONTAL: 5 uSec/Div
	VERTICAL: 2 V/Div

Figure 5.6. 100-kHz Output Signal Adjustment

5.8. Clean Timer Switch. This procedure may be performed to ensure that both Timers are in Cycle Comp agreement when doing a routine Timer switch to prevent a possible OUT-OF-TOLERANCE condition. The OPERATE Timer's Cycle Comp loop will be actively controlling the transmitter, and will normally vary from its quiescent point by 20 to 40 nSec. In the STANDBY Timer, the Cycle Comp path is broken and the 100 kHz will drift with respect to the OPERATE Timer. Alignment of the 100-kHz waveforms is necessary for a Clean Timer Switch. The following procedure is used to synchronize the Operate and Standby 100-kHz waveforms, and switch Timers when they are in phase agreement.

NOTE

Before performing the Clean Timer Switch procedure outlined below, ensure that the Cycle Compensation Loop in the STANDBY Timer has been properly adjusted, as outlined in paragraph 5.6. Also, ensure that the 100-kHz Output Signal from the STANDBY Timer has been properly adjusted to 12 volts peak-to-peak as outlined in paragraph 5.7.

5.8.1. The following procedure may be used for aligning the Cycle Comp loop circuitry for a Clean Timer Switch using 100-kHz Squarewave Signals:

a. Use a calibrated dual trace oscilloscope with two X10 probes and one X1 probe.

b. Calibrate the two X10 probes.

c. Using the X1 probe, trigger the oscilloscope with the waveform at TP7 (Red) on any DRRG module (E, F, or G card) of the OPERATE Timer.

d. Connect a calibrated X10 probe from the left vertical channel (A) on the oscilloscope to TP2 (Blue) (100-kHz squarewave) on the INTERFACE module (R card) of the OPERATE Timer.

e. Connet a calibrated X10 probe from the right vertical channel (B) on the oscilloscope to TP2 (Blue) (100-kHz squarewave) on the INTERFACE module (R card) of the STANDBY Timer.

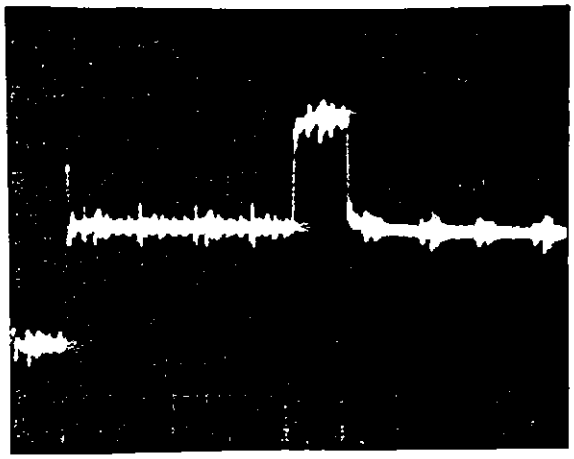
f. Set each channel separately so that the 100 kHz is two divisions peak-to-peak.

g. Set the horizontal control at one uSec per division so that one cycle of the 100 kHz is visible.

h. Invert the right vertical channel (B) and add channel A and channel B to obtain the presentation in Figure 5.7.

i. Insert an LPA into the STANDBY Timer; 0.5 uSec is generally sufficient.

j. Observe the squares on the waveform; they should decrease in width. If not, double the LPA and insert it with the opposite sign into the STANDBY Timer.



SIGNAL AND SOURCE	SETTINGS
	TRIGGER:
Channel A: TP2 (Blue) INTERFACE Module (R) 100-kHz Squarewave	(-) External
Channel B: TP2 (Blue) INTERFACE Module (R) 100-kHz Squarewave (Inverted)	MODE Main
Trigger: TP7 (Red any DRRG Module (E,F,G)	HORIZONTAL: 1 uSec/Div
Channel A & B, ADDED	VERTICAL: .2 V/Div

Figure 5.7. Clean Timer Switch Waveforms (Squarewave)

k. When the waveform reaches its null (a straight line), press RESET TO EXTERNAL on the STANDBY Timer and observe the NO EXTERNAL AGREEMENT indicator. If the NO EXTERNAL AGREEMENT indicator extinguishes, and the waveform remains at its null, switch Timers immediately. If the NO EXTERNAL AGREEMENT indicator does not extinguish, DO NOT switch Timers, proceed to step 'i' of this paragraph, and insert another LPA of opposite polarity and of equal magnitude to the first LPA that was inserted.

NOTE

Ensure the waveform remains at its null before continuing (approximately five seconds). If it continues to move, depress the RESET TO EXTERNAL switch on the STANDBY Timer, and start over with step 'i'.

l. Perform steps a through k above when switching back to the original Timer.

5.8.2. The following procedure may be used for aligning the Cycle Comp Loop circuitry for a Clean Timer Switch using 100-kHz Sinewave Signals:

a. Use a calibrated dual trace oscilloscope with two X10 probes and one X1 probe.

b. Calibrate the two X10 probes.

c. Using the X1 probe, trigger the oscilloscope with the waveform at TP7 (Red) on any DRRG module (E, F, or G card) of the OPERATE Timer.

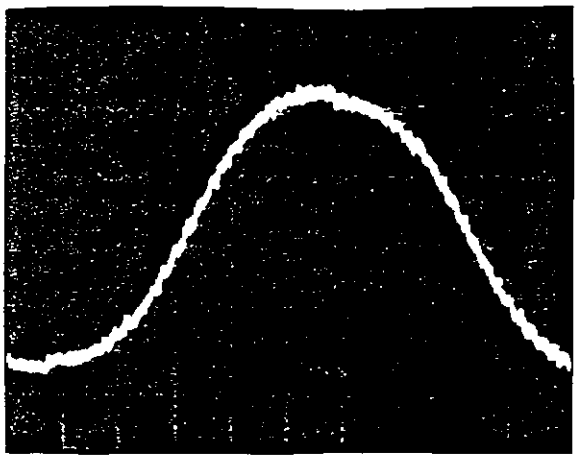
d. Connect a calibrated X10 probe from the left vertical channel (A) on the oscilloscope to TP1 (Red) (100-kHz sinewave) on the INTERFACE module (R card) of the OPERATE Timer.

e. Connet a calibrated X10 probe from the right vertical channel (B) on the oscilloscope to TP1 (Red) (100-kHz sinewave) on the INTERFACE module (R card) of the STANDBY Timer.

f. Set each channel separately so that the 100 kHz is six divisions peak-to-peak.

g. Set the horizontal control at one uSec per division so that one cycle of the 100 kHz is visible.

h. Invert the right vertical channel (B) and add channel A and channel B to obtain the presentation in Figure 5.8.



SIGNAL AND SOURCE	SETTINGS
	TRIGGER:
Channel A: TP1 (Red) INTERFACE Module (R) 100-kHz Sinewave	(-) External
Channel B: TP1 (Red) INTERFACE Module (R) 100-kHz Sinewave (Inverted)	MODE Main
Trigger: TP7 (Red any DRRG Module (E,F,G)	HORIZONTAL: 1 uSec/Div
Channel A & B, ADDED	VERTICAL: .2 V/Div

Figure 5.8. Clean Timer Switch Waveforms (Sinewave)

i. Insert an LPA into the STANDBY Timer; 0.5 uSec is generally sufficient.

j. Observe the resulting waveforms, it should decrease in amplitude . If not, double the LPA and insert it with the opposite sign into the STANDBY Timer.

k. When the waveform reaches its null (a straight line), press RESET TO EXTERNAL on the STANDBY Timer and observe the NO EXTERNAL AGREEMENT indicator. If the NO EXTERNAL AGREEMENT indicator extinguishes, and the waveform remains at its null, switch Timers immediately. If the NO EXTERNAL AGREEMENT indicator does not extinguish, DO NOT switch Timers, proceed to step 'i' of this paragraph, and insert another LPA of opposite polarity and of equal magnitude to the first LPA that was inserted.

NOTE

Ensure the waveform remains at its null before continuing (approximately five seconds). If it continues to move, depress the RESET TO EXTERNAL switch on the STANDBY Timer, and start over with step 'i'.

l. Perform steps a through k above when switching back to the original Timer.

5.9. DRRG Alarm Check. This check should ONLY be performed on the STANDBY Timer using the following procedure:

a. Remove the appropriate +28 VDC fuse on the front panel of the C-8621/FPN Timer Set Control for the Timer under test.

b. Depress the appropriate 115 VAC power switch, removing power to the STANDBY Timer.

c. Remove one DRRG module (E,F or G card) from the STANDBY Timer.

d. Depress the appropriate 115 VAC power switch to re-apply power to the STANDBY Timer. Note that the front panel indicator for the missing DRRG module should be illuminated.

e. Depress the appropriate 115 VAC power switch to remove power to the STANDBY Timer, and replace the DRRG module that was removed.

f. Repeat steps c through e for the remaining DRRG modules. Ensure all alarm indicators operate properly.

g. Remove any two DRRG modules (E, F, or G cards).

h. Depress the appropriate 115 VAC power switch to re-apply power to STANDBY Timer and note the front panel indications. All three DRRG indicators should be illuminated. The CHECK TIMING indicator should also be illuminated, since there is no majority agreement of DRRG modules. (This is also the reason why all three DRRG indicators are illuminated). Also, the NO TRANSMITTER DRIVE light should illuminate.

i. Depress the appropriate 115 VAC power switch to remove power to the STANDBY Timer, and replace the DRRG modules that were removed.

j. Re-apply 115 VAC and + 28 VDC power to the STANDBY Timer.

k. Depress the CHECK TIMING and RESET TO EXTERNAL indicator/switches on the STANDBY Timer to return the equipment to normal operation.

l. Perform the DRRG Alarm Check on the other Timer, when it is placed in STANDBY mode for maintenance, using the above procedure.

5.10. DC Power Supply Checks. Power supplies 1A1A4, 1A1A5, 1A1A6 and 1A1A7 should be checked while installed in the Loran Timer. When troubleshooting suspected power supply problems, ensure the Loran Timer is in the STANDBY mode, pull the Timer out to the chassis slide stop mechanism, and remove the top cover. All Timer power

supplies should be checked for proper output voltage and ripple. The ripple should not exceed 1.0 mV p-p, and the oscilloscope probes should be placed on the same terminals used to measure voltages (do not measure voltage and ripple at the same time, as some types of Digital Voltmeters can introduce noise). Whenever a power supply cannot be adjusted to within the required limits, the supply is considered defective.

NOTE

Perform all power supply checks and adjustments only when the Timer is in STANDBY mode or an OUT-OF-TOLERANCE condition may occur.

5.10.1. 1A1A4 +5 VDC Power Supply Adjustment.

a. Set the voltmeter range to 10 VDC. Connect the negative lead of the voltmeter to 1A1A3TB1-3, and the positive lead to 1A1A3TB1-1. Observe the voltage indicated. If necessary, adjust the voltage control (VA) on the rear apron of the Timer chassis until the meter indicates 5.0 VDC ± 0.1 VDC.

NOTE

Power Supply 1A1A4 current limit is factory set and should not be adjusted.

5.10.2. 1A1A5 +28 VDC Power Supply Adjustment.

a. Set the voltmeter range to 50 VDC. Connect the negative lead of the voltmeter to 1A1A7TB1-8, and the positive lead to 1A1A7TB1-9. Observe the voltage indicated. If necessary, adjust the Voltage Adjust Control on the top front left corner of the power supply 1A1A5 to obtain 28.0 VDC.

5.10.3. 1A1A6 ±15 VDC Power Supply Adjustment. Use the following procedure to adjust the power supply output:

CAUTION

This power supply has an overvoltage protection circuit (LC-OV-11) that is set for 35.5 VDC, or approximately 118.3% of power supply output. It must be set according to the procedure outlined in paragraph 2.5.6.3 when the supply is replaced. Remove the ERR SNS and INTERFACE modules before setting the overvoltage protection circuit, or they may be damaged.

a. Set the voltmeter range to 50 VDC. Connect the negative lead to 1A1A3TB1-5, and the positive lead to 1A1A3TB1-9.

b. Adjust the VDC ADJ Control so the output of the 1A1A6 power supply is +30.0 VDC ±0.1 VDC.

c. Check the voltage between ground and 1A1TB1-5 (should be -15 V ±1 V) and between ground and 1A1TB1-9 (should be +15 V ±1 V).

5.10.4. 1A1A7 +5 VDC Power Supply Adjustment.

NOTE

The 1A1A5 Power Supply must be adjusted before the 1A1A7 Power Supply is adjusted.

a. Set the voltmeter range to 10 VDC. Connect the negative lead of the voltmeter to 1A1A7TB1-8 and the positive lead to 1A1A7TB1-2.

b. If necessary, adjust the 1A1A7 power supply Output Voltage control to obtain +5 VDC ±0.1 VDC.

5.10.5. Disconnect the voltmeter leads, replace the top cover, and release the lock mechanism to slide the Loran Timer into the cabinet.

5.11. MPT Movement (ETA Dial) Check (AN/FPN-54A only). This check should be performed on the STANDBY Timer only to insure MPTs move the desired amount and direction.

a. On the STANDBY Timer, using a calibrated oscilloscope and a X10 scope probe, monitor the Timer output multipulse triggers at TP5 (Orange) on the INTERFACE module (R card).

b. Trigger the oscilloscope from TP7 (Red) on any DRRG module (E, F, or G card).

c. Adjust the oscilloscope time base so that when the Timer ETA dial is changed, a 0.1 uSec change can be observed.

d. Change the Timer ETA dial thumbwheel setting and ensure that the MPTs are moving the desired amount and direction. If MPTs do not move, make sure the Timer is in LOCAL mode.

e. Return the STANDBY Timer to the orginal ETA dial thumbwheel setting.

5.11.1. Perform the MPT Movement (ETA Dial) Check, as outlined above, when the other Timer is placed in STANDBY mode for maintenance.

5.12. Troubleshooting. Table 5.1 can be used as an aid in troubleshooting (NOTE: perform all checks on the STANDBY Timer only). The Table has been formatted in numerical order with indications as follows:

1. Some Front Panel Lamps
2. TIMER STATUS Indicators
3. TIMING REFERENCE Indicators
4. WAVEFORM CONTROL Indicators
5. All Front Panel Lamps
6. LOCAL LPA
7. REMOTE LPA
8. LOCAL BLINK
9. REMOTE BLINK
10. CHECK TIMING Indicator only
11. NO EXTERNAL AGREEMENT Indicator only

5.12. Troubleshooting. (Continued)

12. Any 1 DRRG STATUS Indicator
13. All 3 DRRG STATUS Indicators
14. NO TRANSMITTER DRIVE Indicator only
15. ETA ADJUST

5.12.1. Power Supply Troubleshooting Guide. Troubleshooting of power supply problems for each of the four power supplies within the Timer begins with either an audio alarm or front panel indication. All of the power supplies have over-voltage protection circuits which crowbar the DC output to ground. In the event of a transient at the output, the overvoltage protector may be tripped. Once tripped, the overvoltage protection circuits remain shorted as long as current flows. Power must be removed to reset them. Therefore, power for a suspected unit should be secured for one minute, and then re-applied to establish failure. A Timer whose power supplies have intermittent failures should be switched to STANDBY, and have all power supplies inputs/outputs carefully checked. If the condition re-occurs when the Timer is returned to OPERATE status, switch back to STANDBY, de-energize the Timer and replace the suspect power supply.

5.12.2. Power Supply Indications. Some indications of defective power supplies are:

a. 1A1A4 +5 VDC Power Supply. If the NO TRANSMITTER DRIVE indicator is dimly lit and there is an audio alarm with loss of transmitter drive, depress the LAMP TEST switch. If the switch has no effect on the NO TRANSMITTER DRIVE and BLINK indicators, the output of this power supply is incorrect.

b. 1A1A5 +28 VDC Power Supply. If all front panel lamps are extinguished and the LAMP TEST switch has no effect, the output of this supply is incorrect.

c. 1A1A6 ±15 VDC Power Supply. If the NO TRANSMITTER DRIVE indicator is lit and the audio alarm sounds, depress the LAMP TEST switch. If the LAMP TEST and the Buffered Local Signal (Figure 5.37) are normal, but the Hard Limited Local Signal (Figure 5.38) and the 100-kHz Output (Figure 5.48) are incorrect, the output of this power supply is incorrect.

d. 1A1A7 +5 VDC Power Supply. If the audio alarm sounds and NO TRANSMITTER DRIVE and OPERATE or STANDBY indicators are lit, depress the LAMP TEST Switch. If the Timing Reference Indicators fail to light, the 5 VDC output is incorrect.

TABLE 5.1. Troubleshooting Guide

INDICATIONS	POSSIBLE CAUSES	CHECK	ACTION
1. Some Front Panel Lamps			
a. Some front panel lamps do not operate for lamp test. (Except BLINK SELECTION W, X, Y, Z and OPERATE/STANDBY).	a. Defective lamps.	a. All lamps that do not operate properly.	a. Replace defective lamps with type 387 lamp only.
2. TIMER STATUS Indicators			
a. OPERATE/STANDBY indicators.	a. T-BAR switch in C-8621 Timer Set Control, cabling between Timer and Timer Set Control.	a. TIMER #1: Continuity from A8S1-C4C to Timer S card pin 71. TIMER #2: Continuity from A8S1-C10C to Timer S card pin 69.	a. Repair/replace switch S1 section or interconnect cabling as required.
b. LOCAL/REMOTE indicators.	b. Local: B (CDA) card. Remote: C (CDA) card.	b. NONE.	b. Replace either B or C card, as appropriate.
c. NO EXTERNAL AGREEMENT indicator.	c. J (CONTROL) card.	c. NONE.	c. Replace J card.
3. TIMING REFERENCE Indicators			
a. CLEAR, LOAD or EXECUTE.	a. Local: B (CDA) card. Remote: C (CDA) card.	a. NONE.	a. Replace either B or C card, as appropriate.
b. DRRG, CHECK TIMING, RESET TO EXTERNAL.	b. J (CONTROL) card.	b. NONE.	b. Replace J card, or appropriate DRRG.
c. DRRG, CHECK TIMING, RESET TO EXTERNAL.	c. H. (PROGRAM) card.	c. Check jumper programming.	c. Replace H card, or correct programming.

Table 5.1. Troubleshooting Guide
(Continued)

INDICATIONS	POSSIBLE CAUSES	CHECK	ACTION
4. WAVEFORM CONTROL Indicators			
a. Blink indicator.	a. P (BLINK) card.	a. NONE.	a. Replace P card.
5. All Front Panel Lamps			
a. All front panel lamps do not operate.	a. A5 Power Supply.	a. Output of A5 power supply for +30 VDC. (Pos meter lead to A7TB1-9, Neg meter lead to A7TB1-8).	a. If 30 VDC is not present proceed with check 5.b. If 30 VDC is present, proceed to check 5.c.
b. All front panel lamps do not operate.	b. 115 VAC input.	b. Check input of A5 power supply for 115 VAC.	b. If 115 VAC is not present, repair 115 VAC input as required. If 115 VAC is present, replace A5 power supply.
c. All front panel lamps do not operate.	c. Zener Diode A7CR3.	c. Check output of A7CR3 for 24 VDC.	c. If 24 VDC is not present, replace 1A1A7 power supply. If 24 VDC is present, proceed to to check 5.d.
d. All front panel lamps do not operate.	d. Interconnect wiring.	d. Check continuity from A7CR3 to card file backplane.	d. Repair/replace wiring as required.
6. LOCAL LPA			
a. Timer will not accept LOCAL LPA.	a. Local CDA card (B).	a. NONE.	a. Replace B card. Perform local LPA test again. If Timer does not accept local LPA, proceed to check 6.b.
b. Timer will not accept LOCAL LPA.	b. A3S102-S104.	b. Operation of CLEAR, LOAD and EXECUTE switches A3S102-104.	b. Repair/replace as necessary. Perform local LPA test again. If Timer does not accept LPA, proceed to check 6.c.

Table 5.1. Troubleshooting Guide
(Continued)

INDICATIONS	POSSIBLE CAUSES	CHECK	ACTION
6. LOCAL LPA (Cont.)			
c. Timer will not accept LOCAL LPA.	c. Interconnect wiring.	c. Continuity from front panel to B (CDA) card.	c. Repair/replace wiring as required.
d. Timer accepts incorrect LOCAL LPA.	d. LOCAL CDA card (B).	d. NONE.	d. Replace B card.
e. Timer accepts incorrect LOCAL LPA.	e. Thumbwheel Switches.	e. Attempt different LPA to locate defective switch.	e. Replace defective switch.
f. Timer accepts incorrect LOCAL LPA.	f. Interconnect wiring.	f. Check continuity from switch to front panel PCB (A) card.	f. Repair/replace wiring as required.
7. REMOTE LPA			
a. Timer will not accept REMOTE LPA.	a. Remote CDA card (C).	a. NONE.	a. Replace C card. Perform remote LPA test again. If Timer does not accept LPA, proceed to check 7.b.
b. Timer will not accept REMOTE LPA.	b. RCI or TTY.	b. RCI or TTY.	b. Repair/replace as necessary. Perform remote LPA test again If Timer does not accept LPA proceed to check 7.c.
c. Timer will not accept REMOTE LPA.	c. Interconnect wiring.	c. Interconnect cable between RCI and Timer.	c. Repair/replace as required.
d. Timer accepts incorrect REMOTE LPA.	d. REMOTE CDA card (C).	d. NONE.	d. Replace C card.

Table 5.1. Troubleshooting Guide
(Continued)

INDICATIONS	POSSIBLE CAUSES	CHECK	ACTION
8. LOCAL BLINK			
a. Timer will not BLINK in LOCAL Control.	a. Blink (P) card.	a. NONE.	a. Replace P card. Perform local blink test again. If Timer does not blink, proceed to check 8.b.
b. Timer will not BLINK in LOCAL Control.	b. A3S114-117.	b. Operation of blink select switches A3S114-117.	b. Repair/replace as required. Perform local blink test again. If Timer does not blink, proceed to check 8.c.
c. Timer will not BLINK in LOCAL Control.	c. Interconnect wiring.	c. Interconnect cable between front panel and (P) blink card.	c. Repair/replace as required.
9. REMOTE BLINK			
a. Timer will not BLINK in REMOTE Control.	a. Blink (P) card.	a. NONE.	a. Replace P card. Perform remote blink test again. If Timer does not blink, proceed to check 9.b.
b. Timer will not BLINK in REMOTE Control.	b. RCI or TTY.	b. RCI or TTY.	b. Repair/replace as required. Perform remote blink test again. If Timer does not blink, proceed to check 9.c.
c. Timer will not BLINK in REMOTE Control.	c. Interconnect wiring.	c. Interconnect wiring between RCI/TTY and Timer.	c. Repair/replace as required.
10. CHECK TIMING	Indicator Only		
a. Only CHECK TIMING Indicator lit.	a. Momentary timing malfunction has occurred.	a. Reset Check timing indicator by pressing the associated switch.	a. If check timing indicator remains lit, proceed to action 10.b.
b. Only CHECK TIMING Indicator lit.	b. J (CONTROL) card.	b. NONE.	b. Replace J (CONTROL) card.

Table 5.1. Troubleshooting Guide
(Continued)

INDICATIONS	POSSIBLE CAUSES	CHECK	ACTION
11. NO EXTERNAL AGREEMENT Indicator Only			
a. Only NO EXTERNAL AGREEMENT Indicator lit.	a. STBY Timer not in agreement with OP Timer.	a. Reset by pressing RESET TO EXTERNAL on the STBY Timer ONLY. Attempt to reset two or three times before proceeding.	a. If NO EXTERNAL AGREEMENT lamp remains lit, proceed to action 11.b.
b. Only NO EXTERNAL AGREEMENT Indicator lit.	b. J (CONTROL) card.	b. NONE.	b. Replace J (CONTROL) card. If problem persists, proceed to action 11.c.
c. Only NO EXTERNAL AGREEMENT Indicator lit.	c. D (Ø SHIFT) card.	c. NONE.	c. Replace D Ø SHIFT card.
12. Any 1 DRRG STATUS Indicator			
a. DRRG Status 1, 2, or 3 lit.	a. E,F or G (DRRG) card.	a. NONE.	a. Replace DRRG indicated as failed.
b. DRRG Status 1, 2, or 3 lit.	b. J (CONTROL) card.	b. NONE.	b. Replace J card.
c. DRRG Status 1, 2, or 3 lit.	c. Indicator.	c. Check indicator for possible short.	c. Repair/replace as required.
13. ALL 3 DRRG STATUS Indicators			
a. All DRRG Status Indicators lit.	a. Loss of 5 MHz.	a. Check 5 MHz input to D (Ø SHIFT) card TP5, GREEN (Fig. 5.10).	a. If 5 MHz not present, repair/replace Frequency Standard equipment as required. If 5 MHz is present, proceed to check 13.b.
b. All DRRG Status Indicators lit.	b. D (Ø SHIFT).	b. 5 MHz output of D (Ø SHIFT) card TP3, ORANGE (Fig. 5.8).	b. If 5 MHz is not present, replace D (Ø SHIFT) card. If 5 MHz is present, proceed to action 13.c.

Table 5.1. Troubleshooting Guide
(Continued)

INDICATIONS	POSSIBLE CAUSES	CHECK	ACTION
13. ALL 3 DRRG STATUS Indicators (Cont.)			
c. All DRRG Status Indicators lit.	c. J (CONTROL).	c. NONE.	c. Replace J card. If DRRG indicators remain lit, proceed to check 13.d.
d. All DRRG Status Indicators lit.	d. 2/3 DRRGs failed.	d. DRRG LORTO from each DRRG TP6 ORANGE (Fig. 5.16).	d. Replace DRRG's that have failed.
14. NO TRANSMITTER DRIVE Indicator			
a. Only NO TRANSMITTER DRIVE Indicator lit.	a. A6 power supply.	a. Output of A6 P/S for 30 VDC. (pos meter lead to A3TB1-9, neg meter lead to A3TB1-5).	a. If 30 VDC not present, replace A6 P/S. If 30 VDC is present, proceed to check 14.b.
b. Only NO TRANSMITTER DRIVE Indicator lit.	b. A4 power supply.	b. Output of A4 P/S for +5 VDC. (pos meter lead to A3TB1-1, neg meter lead to A3TB1-3).	b. If 5 VDC not present replace A4 P/S. If 5 VDC is present, proceed to check 14.c.
c. Only NO TRANSMITTER DRIVE Indicator lit.	c. R card.	c. R card outputs; 100 kHz, TP1 RED (Fig. 5.48) +MPT, TP5 ORANGE (Fig. 5.52) -MPT, TP6 YELLOW (Fig. 5.54) P.C. SET, TP4 BROWN (Fig. 5.51).	c. Proceed to indicated check procedure if any of the following R card outputs are missing; 100 kHz - check 14.d. +/- MPT - check 14.g. P.C. SET/RESET - check 14.i.
d. Only NO TRANSMITTER DRIVE Indicator lit.	d. T card.	d. 100-kHz input to R card.	d. If 100 kHz present at TP2 BLUE, replace R card. If 100 kHz is not present, proceed to check 14.e.
e. Only NO TRANSMITTER DRIVE Indicator lit.	e. N card.	e. 100-kHz output of N card TP1 BROWN.	e. If 100 kHz present, replace T card. If 100 kHz not present, proceed to check 14.f.

Table 5.1. Troubleshooting Guide
(Continued)

INDICATIONS	POSSIBLE CAUSES	CHECK	ACTION
14. NO TRANSMITTER DRIVE Indicator (Cont.)			
f. Only NO TRANSMITTER DRIVE Indicator lit.	f. D card.	f. 5 MHz input to N card, TP4 YELLOW (Fig. 5.9).	f. If 5 MHz present, replace N card. If 5 MHz not present, possible problems might exist in the backplane wiring of the card file. Request assistance from higher authority.
g. Only NO TRANSMITTER DRIVE Indicator lit.	g. L card.	g. MPT RECLOCK output of L card TP3 ORANGE (Fig 5.34).	g. If MPT RECLOCK present replace R card. If MPT RECLOCK not present proceed to check 14.h.
h. Only NO TRANSMITTER DRIVE Indicator lit.	h. K card.	h. MPT 9 output of K card, TP8 GRAY (Fig. 5.30).	h. If MPT 9 present, replace L card. If MPT 9 not present, replace K card.
i. Only NO TRANSMITTER DRIVE Indicator lit.	i. R, K cards.	i. PHASE CODE output of K card TP9 WHITE (Fig. 5.31).	i. If PHASE CODE present replace R card. If PHASE CODE not present replace K card.
15. ETA ADJUST			
a. Timer inserts incorrect LOCAL ETA ADJUST.	a. L (ETA) card.	a. NONE.	a. Replace L (ETA) card. If problem persists, proceed to action 15.b.
b. Timer inserts incorrect LOCAL ETA ADJUST.	b. Thumbwheel Switches.	b. NONE.	b. Replace suspected switch. If problem persists, proceed to action 15.c.
c. Timer inserts incorrect LOCAL ETA ADJUST.	c. Interconnect wiring.	c. Check continuity from switch to front panel PCB (A) card.	c. Repair/replace wiring as required.

Table 5.1. Troubleshooting Guide
(Continued)

INDICATIONS	POSSIBLE CAUSES	CHECK	ACTION
15. ETA ADJUST (Cont.)			
d. Timer inserts incorrect REMOTE ETA ADJUST.	d. L (ETA) card.	d. NONE.	d. Replace L (ETA) card. If problem persists, proceed to action 15.e.
e. Timer inserts incorrect REMOTE ETA ADJUST.	e. RCI.	e. Switch to LOCAL control and check.	e. Troubleshoot RCI. If problem persists, proceed to action 15.f.
f. Timer inserts incorrect REMOTE ETA ADJUST.	f. Interconnect wiring.	f. Check interconnect wiring between RCI and Timer.	f. Repair/replace as required.

5.12.3. Test Point Waveform Guide. Table 5.2 is a listing of test point waveforms illustrated in this section, and may be used as an aid in troubleshooting.

Table 5.2. Test Point Waveform Guide

CARD	NAME	WAVEFORM	TEST POINT	FIG#
B/C	CDA	CDA Shift Pulse	TP1 Yellow	5.9
		Ground	TP2 Black	
D	Ø-SHIFT	Shifted 5-MHz Square Wave	TP3 Orange	5.10
		5-MHz Square Wave Input	TP4 Yellow	5.11
		5-MHz Sine Wave Input	TP5 Green	5.12
		Ground	TP6 Black	
E	DRRG	100-kHz Square Wave	TP1 Gray	5.13
		DRRG1-DRRG3 Loss	TP3 Green	5.14
		DRRG1-DRRG3	TP4 Blue	5.15
		Phase Code Interval	TP5 Yellow	5.16
		DRRG LORTO	TP6 Orange	5.17
		Scope Triggers	TP7 Red	5.18
		DRRG Clock Waveform	TP8 Brown	5.19
		Ground	TP9 Black	
F	DRRG	100-kHz Square Wave	TP1 Gray	5.13
		DRRG1-DRRG2 Loss	TP3 Green	5.14
		DRRG1-DRRG2	TP4 Blue	5.15
		Phase Code Interval	TP5 Yellow	5.16
		DRRG LORTO	TP6 Orange	5.17
		Scope Triggers	TP7 Red	5.18
		DRRG Clock Waveform	TP8 Brown	5.19
		Ground	TP9 Black	
G	DRRG	100-kHz Square Wave	TP1 Gray	5.13
		DRRG2-DRRG3 Loss	TP3 Green	5.14
		DRRG2-DRRG3	TP4 Blue	5.15
		Phase Code Interval	TP5 Yellow	5.16
		DRRG LORTO	TP6 Orange	5.17
		Scope Triggers	TP7 Red	5.18
		DRRG Clock Waveform	TP8 Brown	5.19
		Ground	TP9 Black	
J	CONTROL	Internal Clock	TP1 Red	5.20
		External Interval Majority LORTO	TP2 Yellow	5.21
		Majority LORTO	TP3 Blue	5.22
		No Majority Reset	TP4 Green	5.23
		Majority Interval LORTO	TP5 White	5.24
		Ground	TP6 Black	

Table 5.2. Test Point Waveform Guide
(Continued)

CARD	NAME	WAVEFORM	TEST POINT	FIG#
K	PC/MPT	5 MHz - L	TP1 Brown	5.25
		End of Count - L	TP2 Red	5.26
		Phase Code - H	TP3 Orange	5.27
		Maj Int. Ø - H	TP4 Yellow	5.28
		Maj MPT Ø - H	TP5 Green	5.29
		Local Interval - L	TP6 Blue	5.30
		PMPT8 - L	TP7 Violet	5.31
		PMPT9 - L	TP8 Gray	5.32
		Maj PCI - H	TP9 White	5.33
		Ground	TP10 Black	
L	ETA	100 nSec Strobe	TP1 Brown	5.34
		5-MHz Input	TP2 Red	5.35
		MPT Reclock	TP3 Orange	5.36
		10-MHz Clock	TP4 Yellow	5.37
		Preset Pulse	TP5 Green	5.38
		Ground	TP6 Black	
M	ERROR SENSE	Limited Operate RF	TP2 Orange	5.39
		Hard Limited Operate RF	TP3 Red	5.40
		Reference Select Gate	TP4 Blue	5.41
		Reference Select Gate (Expanded View)	TP4 Blue	5.42
		Reference Strobe	TP5 Yellow	5.43
		Ground	TP6 Black	
N	Ø-SHIFT	Gated 1-MHz Output	TP2 Red	5.44
		Ø Shifted 5-MHz Output	TP3 Orange	5.45
		Ground	TP6 Black	
P	BLINK	2-Hz Clock	TP1 Yellow	5.46
		Secondary Blink Code	TP2 Green	5.47
		Blink Code Sync	TP3 Red	5.48
		Master Blink Code	TP4 Blue	5.49
		Ground	TP5 Black	
R	INTERFACE	100-kHz Output	TP1 Red	5.50
		100-kHz Input	TP2 Blue	5.51
		Phase Code Reset	TP3 Green	5.52
		Phase Code Set	TP4 Brown	5.53
		(+) MPT Output	TP5 Orange	5.54
		MPT Output (Expanded)	TP5 Orange	5.55
		(-) MPT Output	TP6 Yellow	5.56
		Ground	TP7 Black	

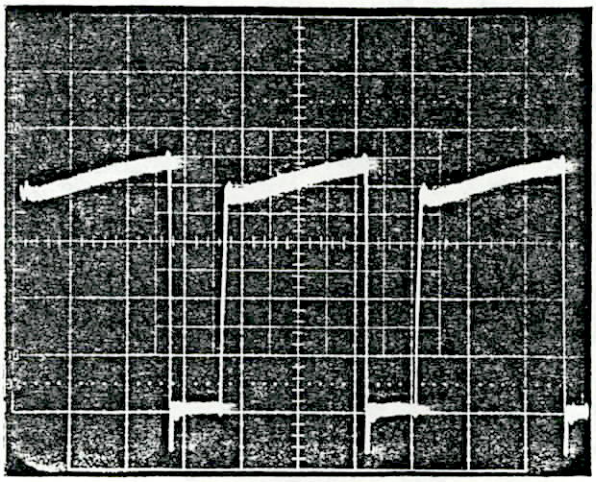
Table 5.2. Test Point Waveform Guide
(Continued)

CARD	NAME	WAVEFORM	TEST POINT	FIG#
T	DRINT/CP	Ground	TP1 Black	5.57
		100 kHz	TP2 Red	5.58
		Multipulse Triggers	TP3 Blue	5.59
		Reclock Pulse Width	TP4 Gray	5.60
		Multipulse Triggers	TP5 Orange	5.61
		Multipulse Triggers (Expanded)	TP5 Orange	5.62
		Blanking Waveform	TP6 Yellow	5.63
		Early Multipulse Triggers	TP7 Green	
		Early Multipulse Triggers (Expanded)	TP7 Green	5.64

5.12.4. Test Points. Table 5.3 lists the figure numbers associated with the various cards within the Loran-C Timer. All test point photographs were taken with a Hewlett-Packard (HP-7834) Storage Oscilloscope using X10 probes with 3-foot cables.

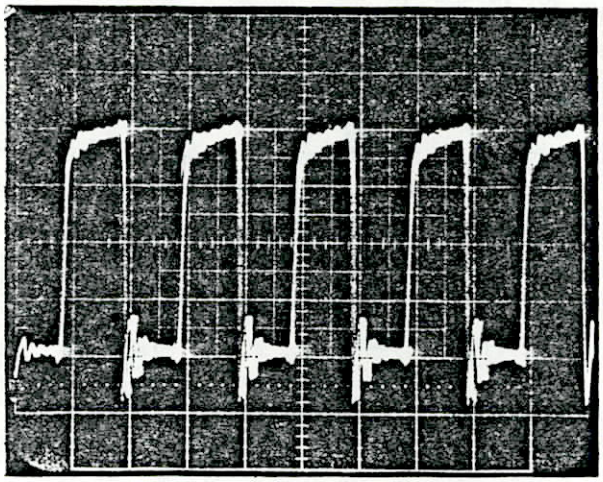
Table 5.3. Test Points

CARD	MODULE DESCRIPTION	FIGURE #'s
B/C	Coding Delay Adjust Module, W0486-5A/CDA	5.9
D	Phase Shift Module, W0486-4/Ø-SHIFT	5.10 - 5.12
E/F/G	Digital Repetition Rate Generator Module, W0486-3A/DRRG	5.13 - 5.19
J	Control Module, W0486-12A/CONTROL	5.20 - 5.24
K	Phase Code Multipulse Trigger Module, W0486-30/PC/MPT	5.25 - 5.33
L	Envelope Timing Adjustment Module, W0486-11/ETA	5.34 - 5.38
M	Error Sense Module, W0486-10E/ERR SNS	5.39 - 5.43
N	Phase Shift Module, W0486-4Ø-SHIFT	5.44 - 5.45
P	Blink Module, W0486-6A/BLINK	5.46 - 5.49
R	Interface Module, W0486-8A/INTERFACE	5.50 - 5.56
T	Dual-Rate Interface/Communications Phase Shift Module, W0486-28B/DRINT/CP	5.57 - 5.64



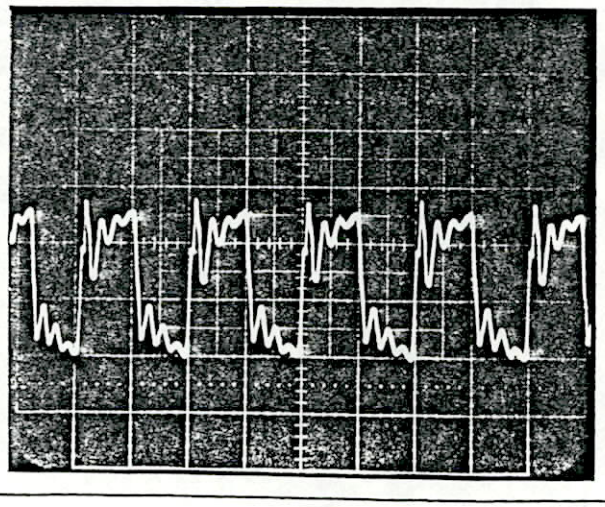
SIGNAL AND SOURCE	SETTINGS
CARD (B) WO486-5A/CDA TP-1 (Yellow)	TRIGGER Internal (+) Auto
Ground reference is 3 Divisions below center	MODE Main Sweep
NOTE: Pulses only present when EXECUTE lamp is LIT.	HORIZONTAL: 200 nSec/Div
	VERTICAL: 0.1 V/Div

Figure 5.9. CDA Shift Pulse



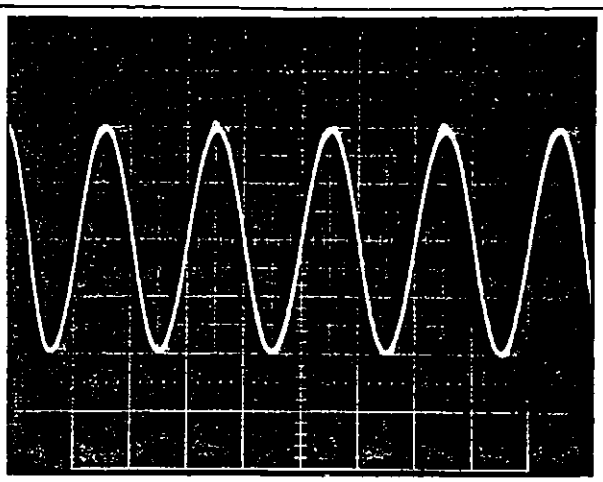
SIGNAL AND SOURCE	SETTINGS
CARD (D) WO486-4/Ø-SHIFT TP-3 (Orange)	TRIGGER Internal (-) Auto
Ground reference is 2 Divisions below center	MODE Main Sweep
	HORIZONTAL: 100 nSec/Div
	VERTICAL: 0.1 V/Div

Figure 5.10. Shifted 5-MHz Square Wave



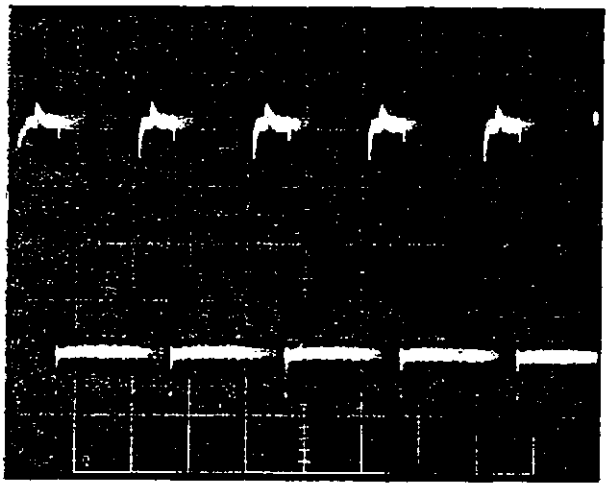
SIGNAL AND SOURCE	SETTINGS
CARD (D) WO486-4/Ø-SHIFT TP-4 (Yellow)	TRIGGER Internal (-) Normal
Ground reference is 2 Divisions below center	MODE Main Sweep
	HORIZONTAL: 100 nSec/Div
	VERTICAL: 0.2 V/Div

Figure 5.11. 5-MHz Square Wave Input



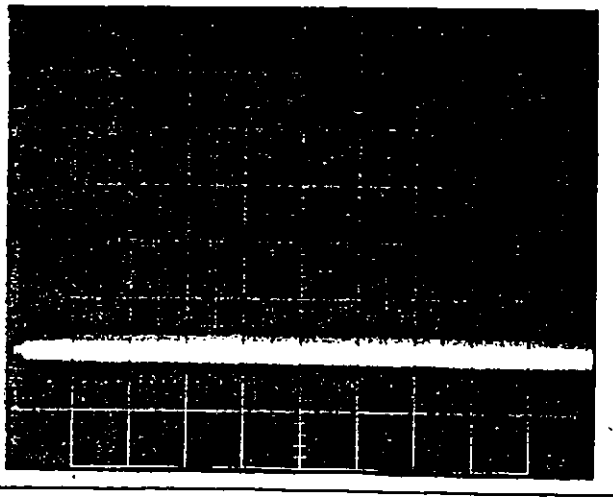
SIGNAL AND SOURCE	SETTINGS
CARD (D) WO486-4/Ø-SHIFT TP-5 (Green) Ground reference is at center of screen.	TRIGGER Internal (+) Normal MODE Main Sweep HORIZONTAL: 100 nSec/Div VERTICAL: 0.2 V/Div

Figure 5.12. 5-MHz Sine Wave Input



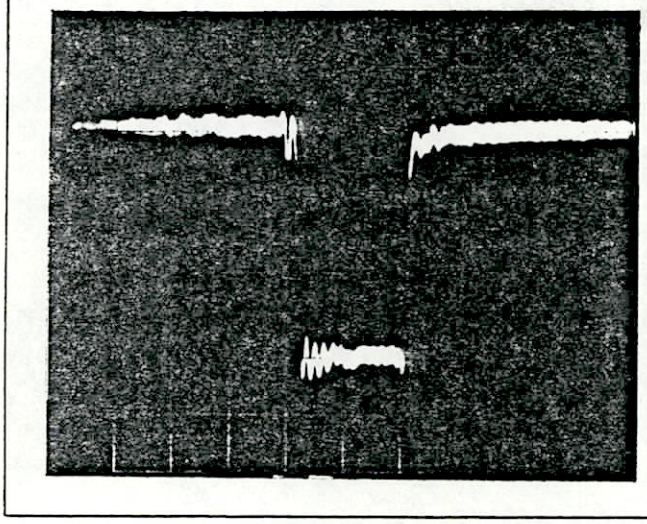
SIGNAL AND SOURCE	SETTINGS
CARDS E,F,G WO486-3A/DRRG TP-1 (Gray) Ground reference is 2 Divisions below center	TRIGGER Internal (+) Normal MODE Main Sweep HORIZONTAL: 5 uSec/Div VERTICAL: 0.1 V/Div

Figure 5.13. 100-kHz Square Wave



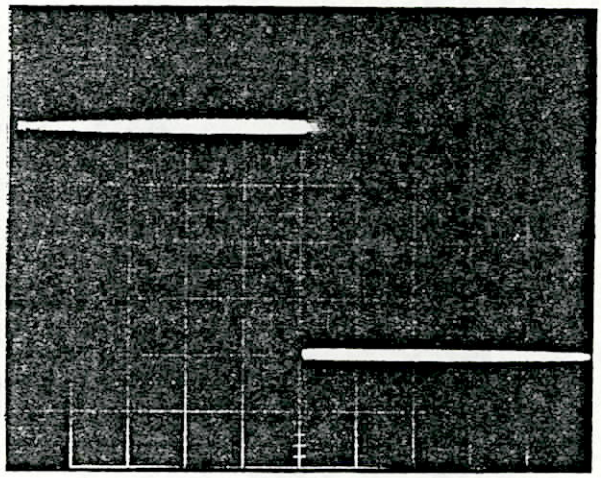
SIGNAL AND SOURCE	SETTINGS
CARDS E,F,G WO486-3A/DRRG TP-3 (Green) Ground reference is 2 Divisions below center	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Main Sweep HORIZONTAL: 5 uSec/Div VERTICAL: 0.1 V/Div

Figure 5.14. DRRGx-DRRGy Loss



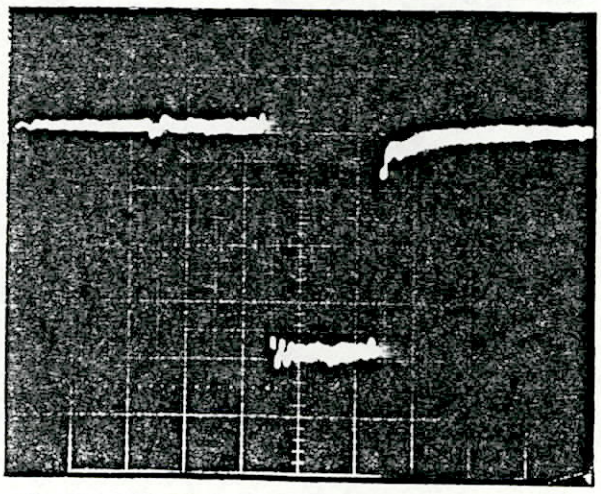
SIGNAL AND SOURCE	SETTINGS
CARDS E,F,G WO486-3A/DRRG TP-4 (Blue) Ground reference is 2 Divisions below center	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Main Sweep .1 mSec/Div Sweep Delay .1 uSec/Div HORIZONTAL: .1 uSec/Div VERTICAL: 0.1 V/Div

Figure 5.15. DRRGx-DRRGy



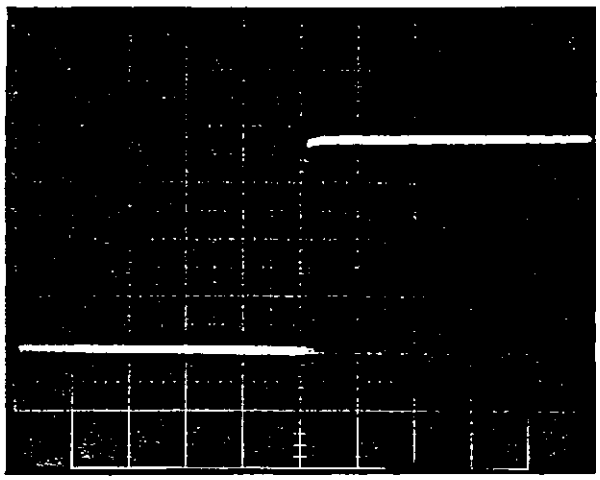
SIGNAL AND SOURCE	SETTINGS
CARDS E,F,G WO486-3A/DRRG TP-5 (Yellow) Ground reference is 2 Divisions below center	TRIGGER Normal Internal (+) MODE Main Sweep HORIZONTAL: 20 mSec/Div VERTICAL: 0.1 V/Div

Figure 5.16. Phase Code Interval



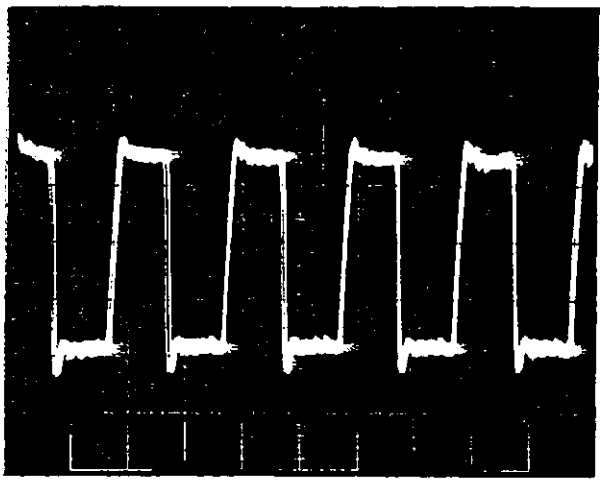
SIGNAL AND SOURCE	SETTINGS
CARDS E,F,G WO486-3A/DRRG TP-6 (Orange) Ground reference is 2 Divisions below center	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Main Sweep .1 mSec/Div Sweep Delay .1 uSec/Div HORIZONTAL: 0.1 uSec/Div Delayed VERTICAL: 0.1 V/Div

Figure 5.17. DRRG LORTO



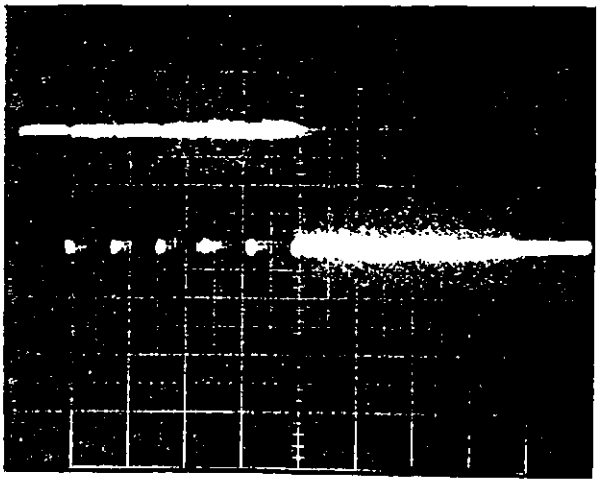
SIGNAL AND SOURCE	SETTINGS
CARDS E,F,G WO486-3A/DRRG TP-7 (Red) Ground reference is 2 Divisions below center Falling edge occurs 100 uSec before LORTO	TRIGGER Normal Internal (-) MODE Main Sweep HORIZONTAL: 20 uSec/Div VERTICAL: 0.1 V/Div

Figure 5.18. Scope Triggers



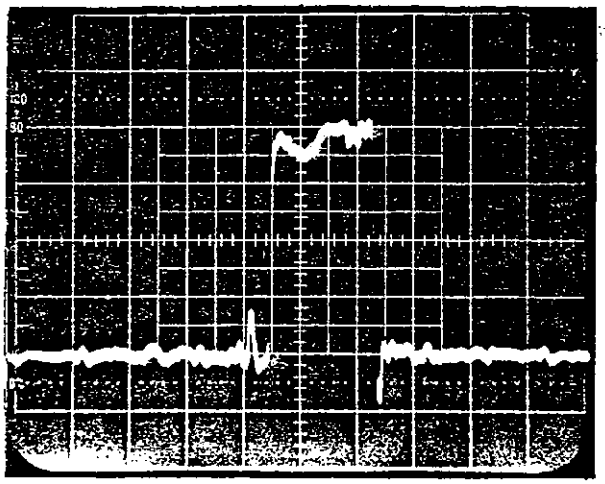
SIGNAL AND SOURCE	SETTINGS
CARDS E,F,G WO486-3A/DRRG TP-8 (Brown) Ground reference is 2 Divisions below center.	TRIGGER Internal (+) Normal MODE Main Sweep HORIZONTAL: 100 nSec/Div VERTICAL: 0.1 V/Div

Figure 5.19. DRRG Clock Waveform



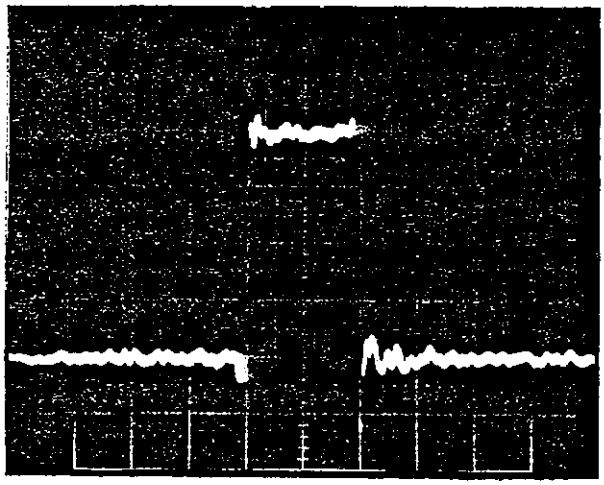
SIGNAL AND SOURCE	SETTINGS
CARD (J) WO486-12A/CONTROL TP-1 (Red) Ground reference is Center line NOTE: Pulse present only immediately following execution of RESET TO EXTERNAL	TRIGGER Internal (+) Normal MODE Main Sweep HORIZONTAL: 2 uSec/Div VERTICAL: 0.2 V/Div

Figure 5.20. Internal Clock



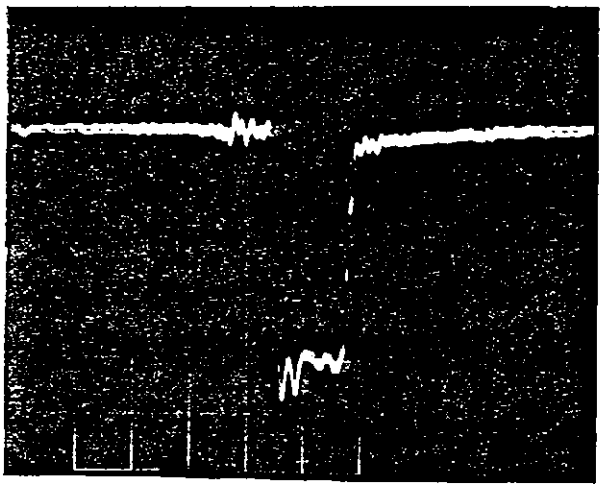
SIGNAL AND SOURCE	SETTINGS
CARD (J) WO486-12A/CONTROL TP-2 (Yellow) Ground reference is 2 Divisions below center	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Main Sweep 50 uSec/Div Sweep Delay .1 uSec/Div HORIZONTAL: .1 uSec/Div Delayed VERTICAL: 0.1 V/Div

Figure 5.21. External Interval Majority LORTO



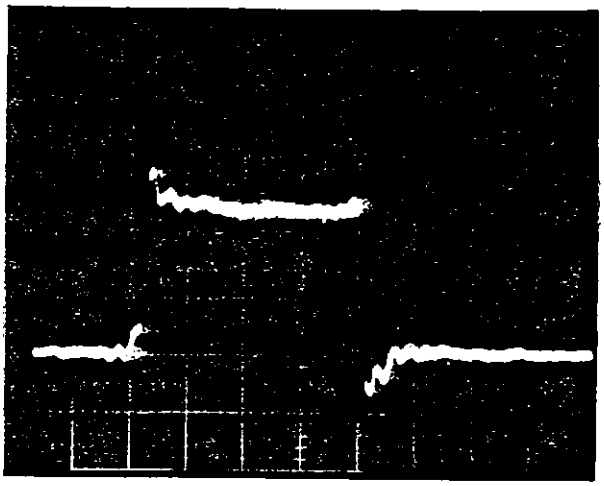
SIGNAL AND SOURCE	SETTINGS
CARD (J) WO486-12A/CONTROL TP-3 (Blue) Ground reference is 2 Divisions below center	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Main Sweep 50 uSec/Div Sweep Delay .1 uSec/Div HORIZONTAL: .1 uSec/Div Delayed VERTICAL: 0.1 V/Div

Figure 5.22. Majority LORTO



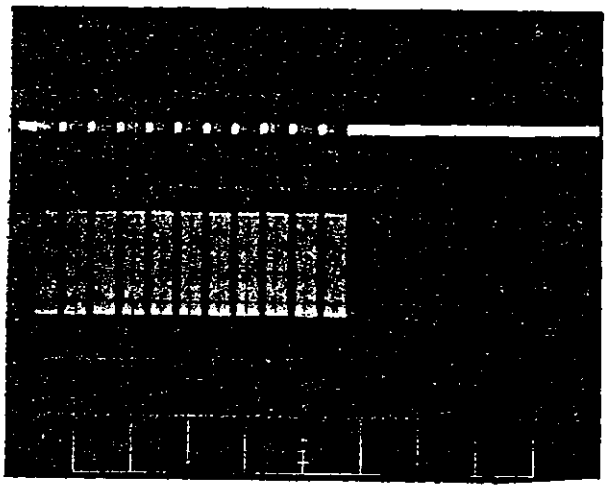
SIGNAL AND SOURCE	SETTINGS
CARD (J) WO486-12A/CONTROL TP-4 (Green) Ground reference is 2 divisions above center NOTE: Two DRRG cards must be removed to see this pulse	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Main Sweep 50 uSec/Div Sweep Delay .1 uSec/Div HORIZONTAL: .1 uSec/Div Delayed VERTICAL: 0.1 V/Div

Figure 5.23. No Majority Reset



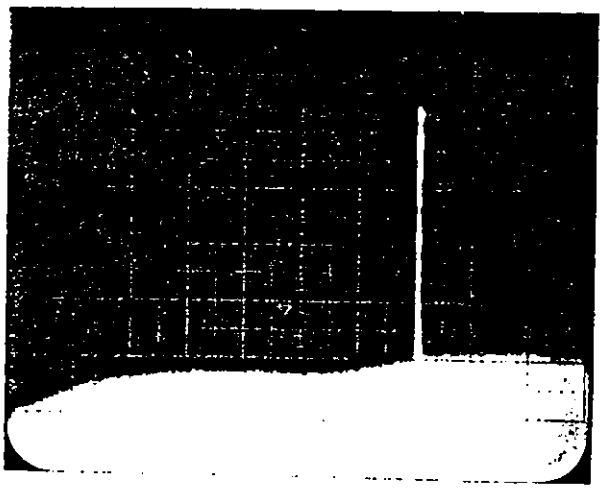
SIGNAL AND SOURCE	SETTINGS
CARD (J) WO486-12A/CONTROL TP-5 (White) Ground reference is 2 Divisions below center NOTE: Pulse is only present on every other sweep.	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Main Sweep .1 mSec/Div Sweep Delay 50 nSec/Div HORIZONTAL: Sweep Delay 50 nSec/Div VERTICAL: 0.2 V/Div

Figure 5.24. Majority Interval LORTO



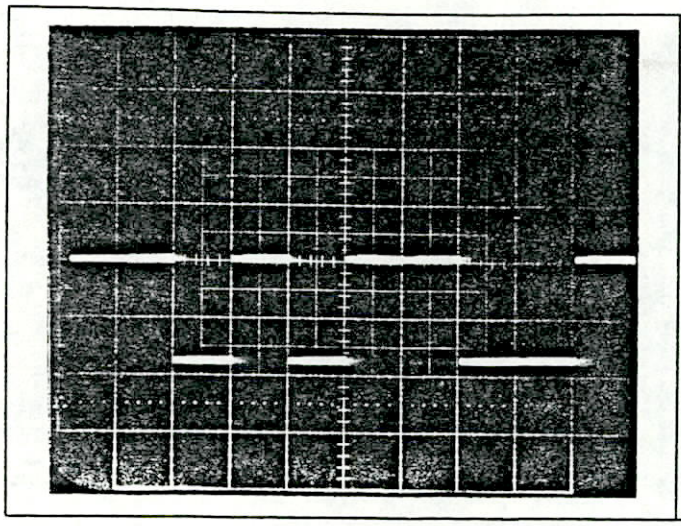
SIGNAL AND SOURCE	SETTINGS
CARD (K) WO486-30/PC/MPT TP-1 (Brown) Ground reference is 2 Divisions below center	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Main Sweep HORIZONTAL: 2 mSec/Div VERTICAL: 0.1 V/Div

Figure 5.25. 5 MHz-L



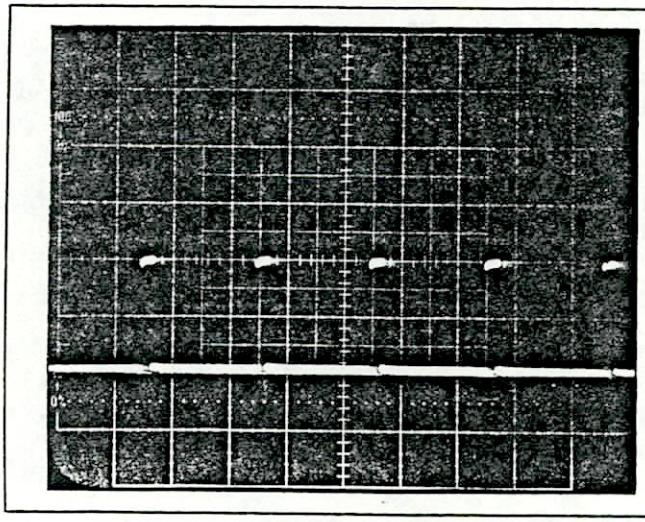
SIGNAL AND SOURCE	SETTINGS
CARD (K) WO486-30/PC/MPT TP-2 (Red) Ground reference is 4 Divisions below center	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Main Sweep HORIZONTAL: .2 mSec/Div VERTICAL: 50 mV/Div

Figure 5.26. End of Count-L



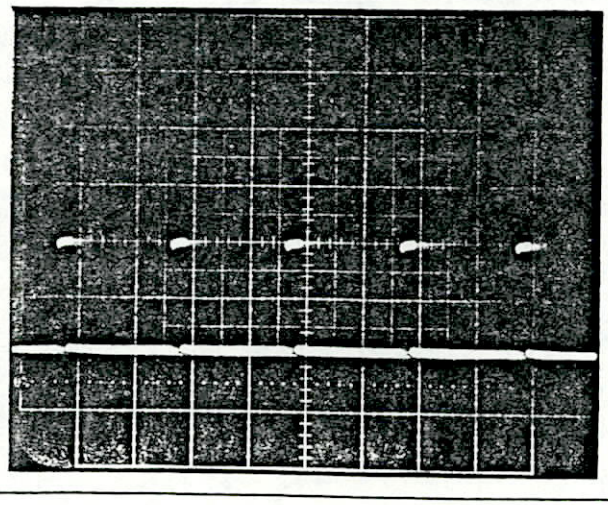
SIGNAL AND SOURCE	SETTINGS
CARD (K) WO486-30/PC/MPT TP-3 (Orange) Secondary Ground reference is 2 Divisions below center (Program dependent)	TRIGGER DRRG Cards E,F, or G TP-5 (YELLOW) External (-) MODE Main Sweep HORIZONTAL: 1 mSec/Div VERTICAL: 0.2 V/Div

Figure 5.27. Phase Code-H



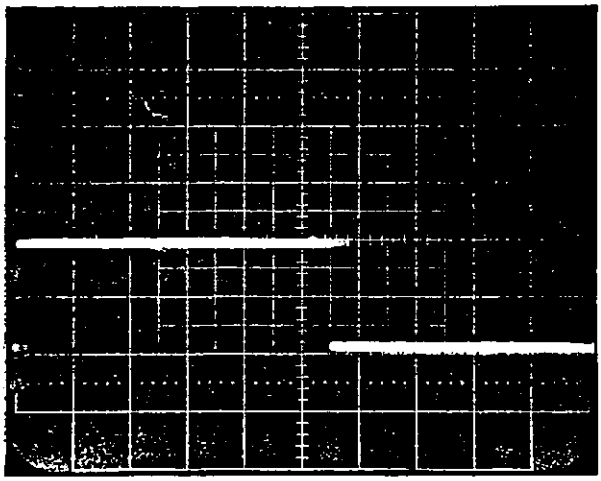
SIGNAL AND SOURCE	SETTINGS
CARD (K) WO486-30/PC/MPT TP-4 (Yellow) Tube XMTR Ground reference is 2 Divisions below center	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Main Sweep HORIZONTAL: 0.5 mSec/Div VERTICAL: 0.2 V/Div

Figure 5.28. Maj Int Ø - H



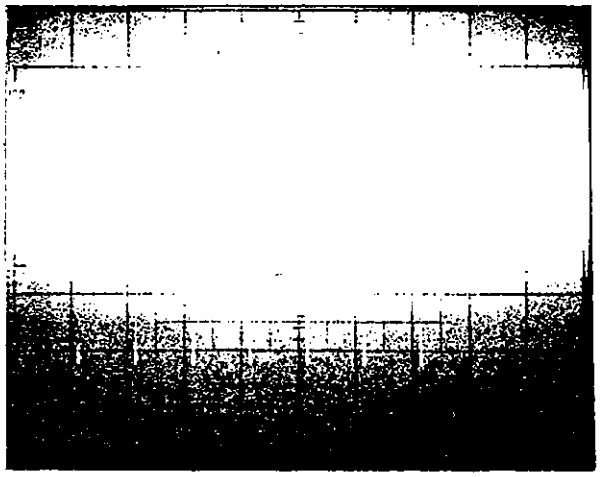
SIGNAL AND SOURCE	SETTINGS
CARD (K) WO486-30/PC/MPT TP-5 (Green) Tube XMTR Ground reference is 2 Divisions below center	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Main Sweep HORIZONTAL: 0.5 mSec/Div VERTICAL: 0.2 V/Div

Figure 5.29. Maj MPT Ø - H



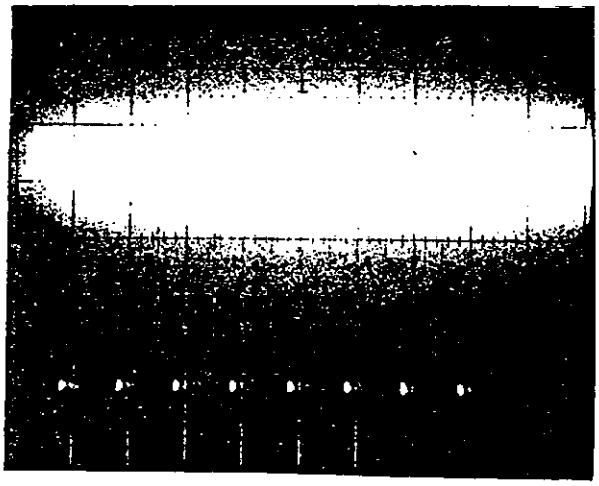
SIGNAL AND SOURCE	SETTINGS
CARD (K) WO486-30/PC/MPT TP-6 (Blue) Ground reference is 2 Divisions below center (Program dependent)	TRIGGER DRRG CARDS E,F, or G TP-7 (RED) External (-) MODE Main Sweep HORIZONTAL: 2 mSec/Div VERTICAL: 0.2 V/Div

Figure 5.30. Local Interval-L



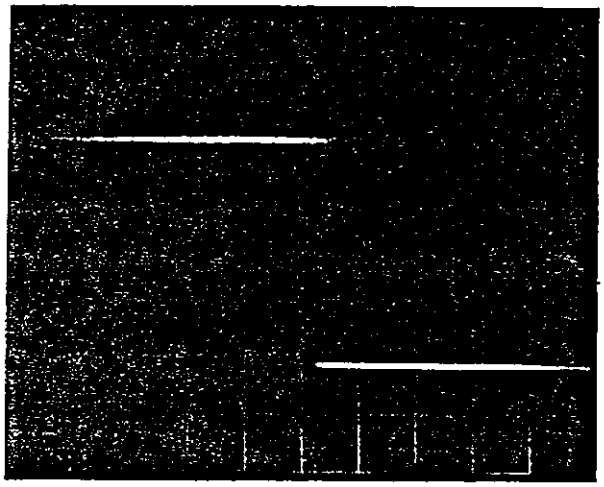
SIGNAL AND SOURCE	SETTINGS
CARD (K) WO486-30/PC/MPT TP-7 (Violet) Ground reference is 2 Divisions below center	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Main Sweep HORIZONTAL: 1 mSec/Div VERTICAL: 0.1 V/Div

Figure 5.31. PMPT8-L



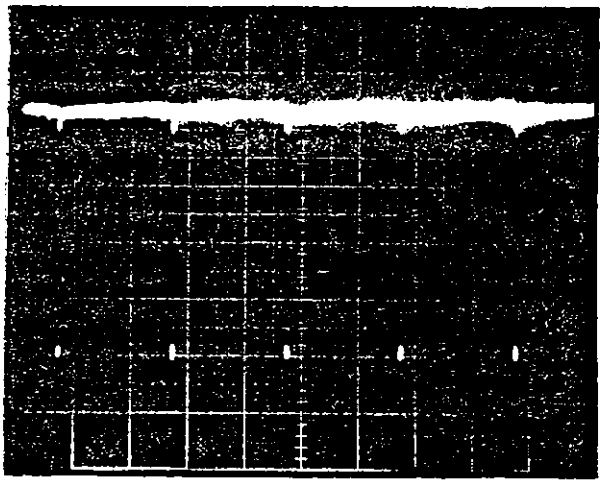
SIGNAL AND SOURCE	SETTINGS
CARD (K) WO486-30/PC/MPT TP-8 (Gray) Ground reference is 2 Divisions below center	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Main Sweep HORIZONTAL: 1 mSec/Div VERTICAL: 0.1 V/Div

Figure 5.32. PMPT9-L



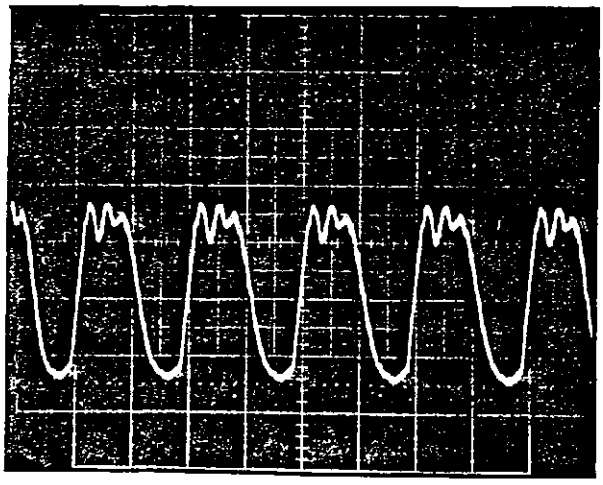
SIGNAL AND SOURCE	SETTINGS
CARD (K) WO486-30/PC/MPT TP-9 (White) Ground reference is 2 Divisions below center (Program dependent)	TRIGGER DRRG Cards E,F, or G TP-5 (YELLOW) External (-) MODE Main Sweep HORIZONTAL: 20 mSec/Div VERTICAL: 0.1 V/Div

Figure 5.33. Maj PCI - H



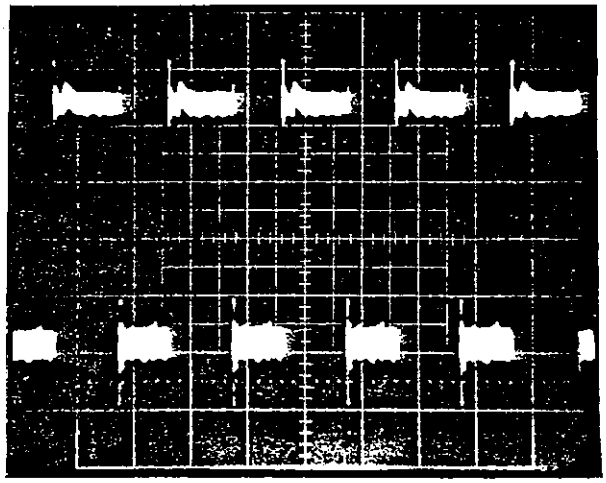
SIGNAL AND SOURCE	SETTINGS
CARD (L) WO486-11/ETA TP-1 (Brown) Ground reference is 2 Divisions below center	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Main Sweep HORIZONTAL: 5 uSec/Div VERTICAL: 0.1 V/Div

Figure 5.34. 100 nSec Strobe



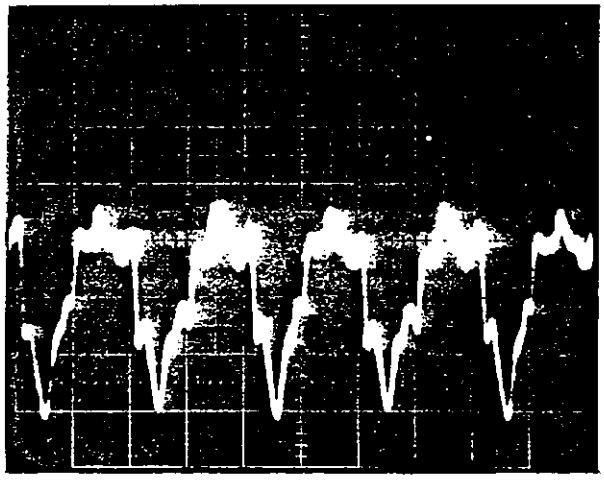
SIGNAL AND SOURCE	SETTINGS
CARD (L) WO486-11/ETA TP-2 (Red) Ground reference is 2 Divisions below center	TRIGGER Internal (+) MODE Main Sweep HORIZONTAL: 0.1 uSec/Div VERTICAL: 0.1 V/Div

Figure 5.35. 5 MHz Input



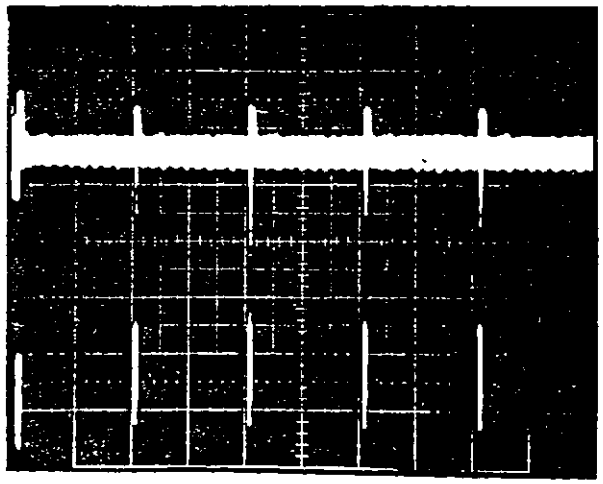
SIGNAL AND SOURCE	SETTINGS
CARD (L) WO486-11/ETA TP-3 (Orange)	TRIGGER Internal (-)
Ground reference is 2 Divisions below center	MODE Main Sweep
	HORIZONTAL: 5 uSec/Div
	VERTICAL: 0.1 V/Div

Figure 5.36. MPT Reclock



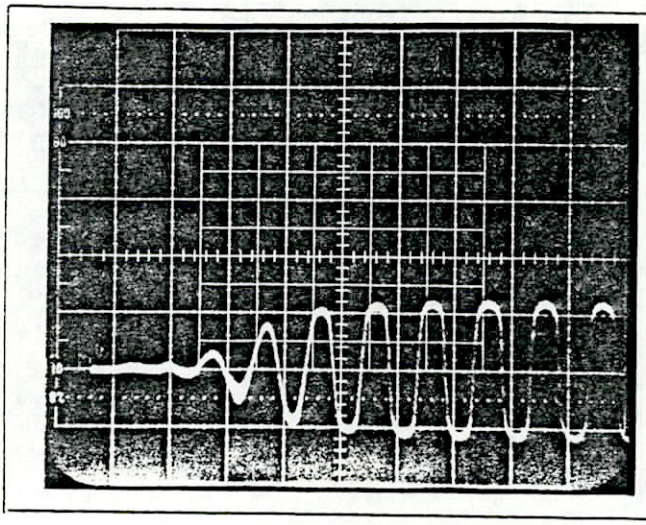
SIGNAL AND SOURCE	SETTINGS
CARD (L) WO486-11/ETA TP-4 (Yellow)	TRIGGER Internal (-)
Ground reference is 2 Divisions below center	MODE Main Sweep
	HORIZONTAL: 50 nSec/Div
	VERTICAL: 0.2 V/Div

Figure 5.37. 10 MHz Clock



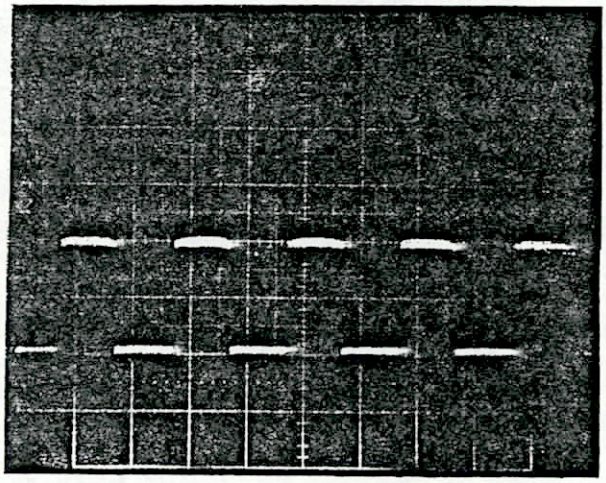
SIGNAL AND SOURCE	SETTINGS
CARD (L) WO486-11/ETA TP-5 (Green)	TRIGGER Internal (-)
Ground reference is 2 Divisions below center	MODE Main Sweep
	HORIZONTAL: 5 uSec/Div
	VERTICAL: 0.1 V/Div

Figure 5.38. Preset Pulse



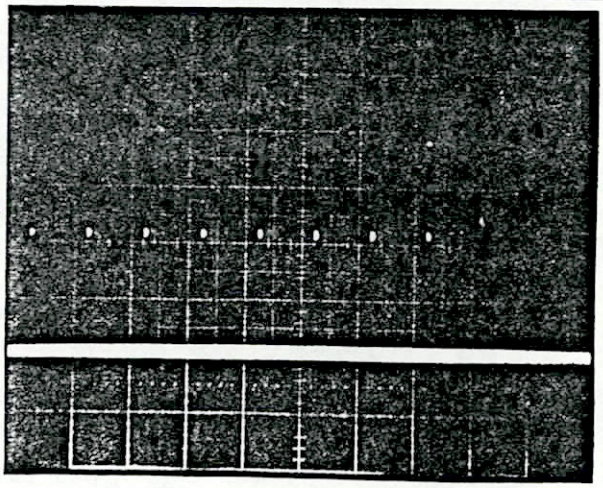
SIGNAL AND SOURCE	SETTINGS
CARD (M) WO486-10E/ERR SNS TP-2 (Orange) Ground reference is 2 Divisions below center	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Delayed Sweep HORIZONTAL: 10 uSec/Div VERTICAL: 0.2 V/Div

Figure 5.39. Limited Operate RF



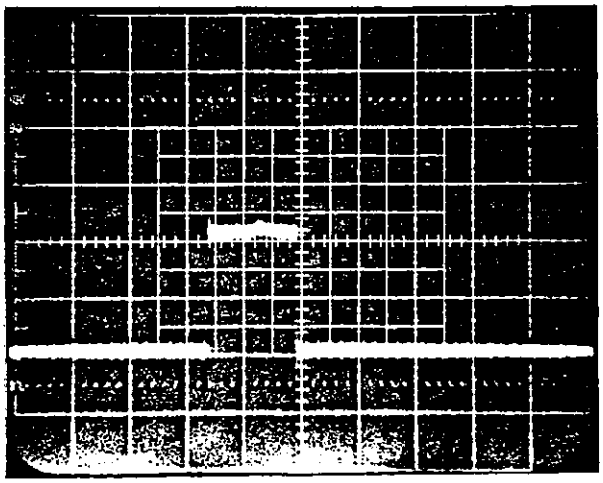
SIGNAL AND SOURCE	SETTINGS
CARD (M) WO486-10E/ERR SNS TP-3 (Red) Ground reference is 2 Divisions below center	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Delayed Sweep HORIZONTAL: 5 uSec/Div VERTICAL: 0.2 V/Div

Figure 5.40. Hard Limited Operate RF



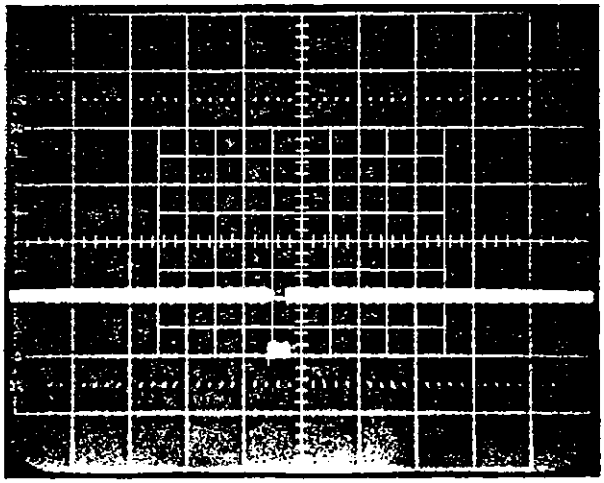
SIGNAL AND SOURCE	SETTINGS
CARD (M) WO486-10E/ERR SNS TP-4 (Blue) Ground reference is 2 Divisions below center	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Main Sweep HORIZONTAL: 1 mSec/Div VERTICAL: 0.2 V/Div

Figure 5.41. Reference Select Gate



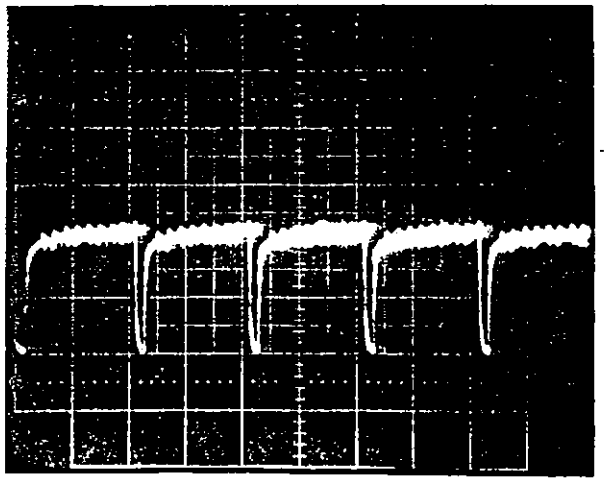
SIGNAL AND SOURCE	SETTINGS
CARD (M) WO486-10E/ERR SNS TP-4 (Blue)	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-)
Ground reference is 2 Divisions below center	MODE Main Sweep 1 mSec/Div Sweep Delay 5 uSec/Div
NOTE: Expanded view of previous Figure	HORIZONTAL: 5 uSec/Div Delayed
	VERTICAL: 0.2 V/Div

Figure 5.42. Reference Select Gate (Expanded View)



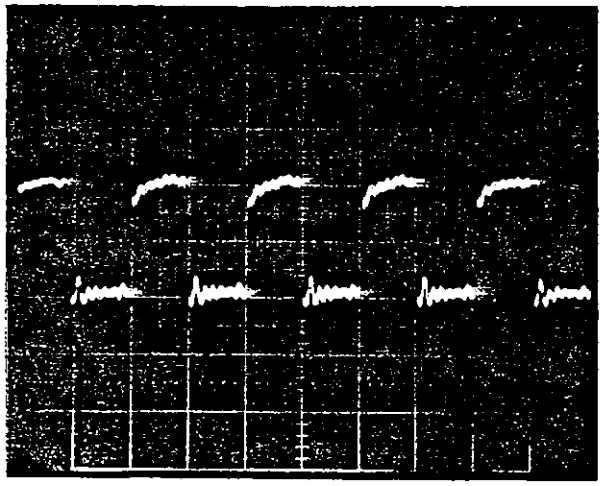
SIGNAL AND SOURCE	SETTINGS
CARD (M) WO486-10E/ERR SNS TP-5 (Yellow)	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-)
Ground reference is 2 Divisions below center	MODE Main Sweep .5 mSec/Div Sweep Delay 10 uSec/Div
	HORIZONTAL: 10 uSec/Div Delayed
	VERTICAL: 0.2 V/Div

Figure 5.43. Reference Strobe



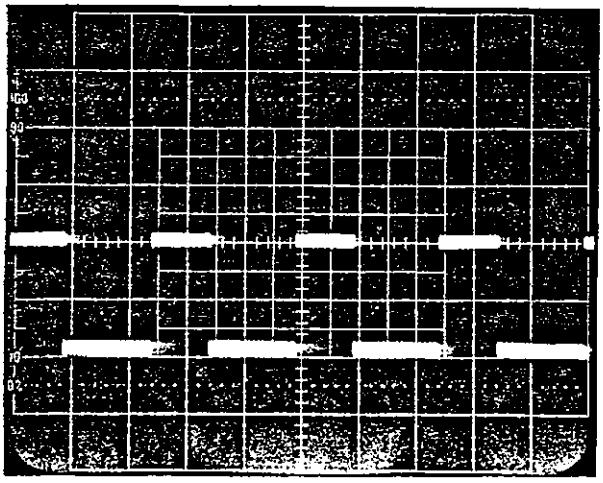
SIGNAL AND SOURCE	SETTINGS
CARD (N) WO486-4/Ø-SHIFT TP-2 (Red)	TRIGGER Internal (-)
Ground reference is 2 Divisions below cneter	MODE Main Sweep
	HORIZONTAL: 0.5 uSec/Div
	VERTICAL: 0.2 V/Div

Figure 5.44. Gated 1 MHz Output



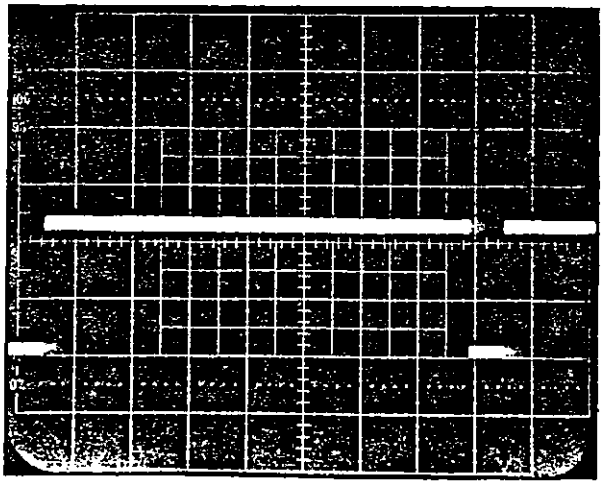
SIGNAL AND SOURCE	SETTINGS
CARD (N) WO486-4/Ø-SHIFT TP-3 (Orange)	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-)
Ground reference is 1 Division below center	MODE Main Sweep
	HORIZONTAL: 100 nSec/Div
	VERTICAL: 0.2 V/Div

Figure 5.45. Ø Shifted 5 MHz Output



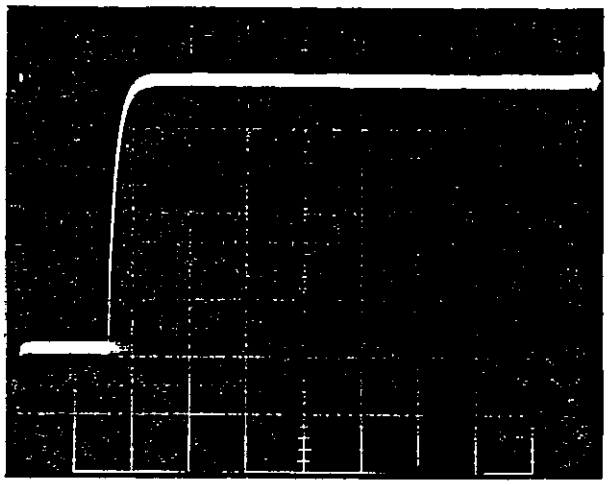
SIGNAL AND SOURCE	SETTINGS
CARD (P) WO486-6A/BLINK TP-1 (Yellow)	TRIGGER Internal (+)
Ground reference is 2 Divisions below center	MODE Main Sweep
	HORIZONTAL: 0.2 Sec/Div
	VERTICAL: 0.2 V/Div

Figure 5.46. 2 Hz Clock



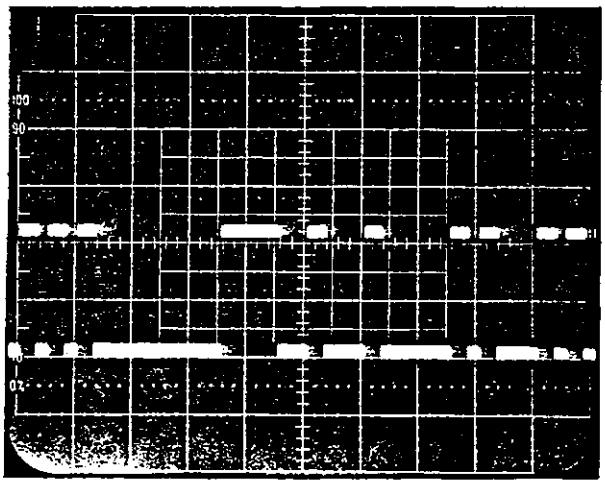
SIGNAL AND SOURCE	SETTINGS
CARD (P) WO486-6A/BLINK TP-2 (Green)	TRIGGER Internal (-)
Ground reference is 2 Divisions below center NOTE: BLINK switches must be depressed.	MODE Main Sweep
	HORIZONTAL: 0.5 Sec/Div
	VERTICAL: 0.2 V/Div

Figure 5.47. Secondary Blink Code



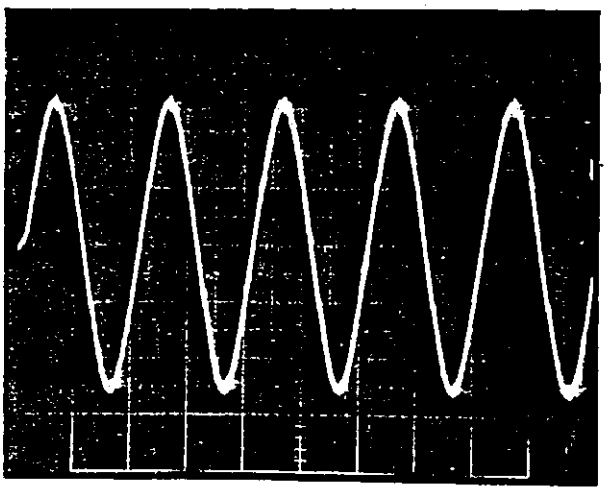
SIGNAL AND SOURCE	SETTINGS
CARD (P) WO486-6A/BLINK TP-3 (Red) Ground reference is 2 Divisions below center	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Main Sweep HORIZONTAL: 5.0 mSec/Div VERTICAL: 0.1 V/Div

Figure 5.48. Blink Code Sync



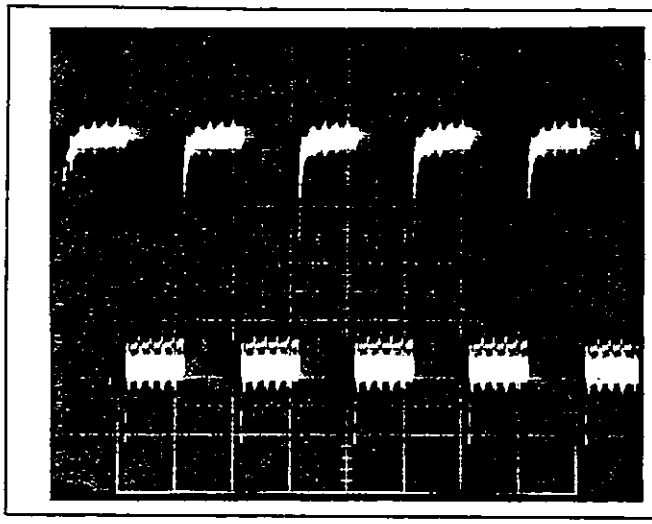
SIGNAL AND SOURCE	SETTINGS
CARD (P) WO486-6A/BLINK TP-4 (Blue) Ground reference is 2 Divisions below center NOTE: BLINK switches must be depressed.	TRIGGER Internal (+) MODE Main Sweep HORIZONTAL: 1 Sec/Div VERTICAL: 0.2 V/Div

Figure 5.49. Master Blink Code



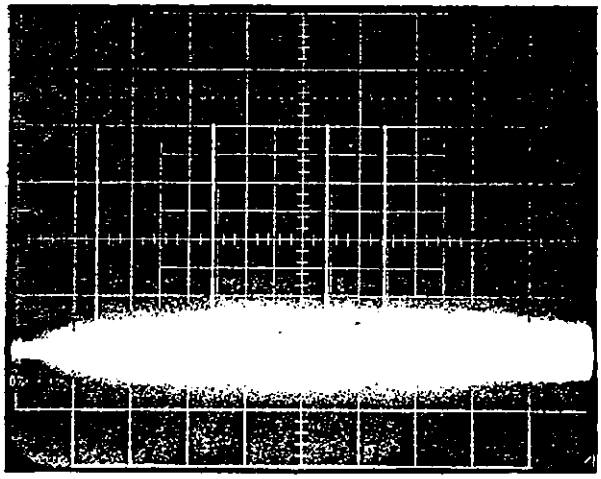
SIGNAL AND SOURCE	SETTINGS
CARD (R) WO486-8A/INTERFACE TP-1 (Red) Ground reference is center line.	TRIGGER Internal (+) MODE Main Sweep HORIZONTAL: 5 uSec/Div VERTICAL: 0.2 V/Div

Figure 5.50. 100-kHz Output



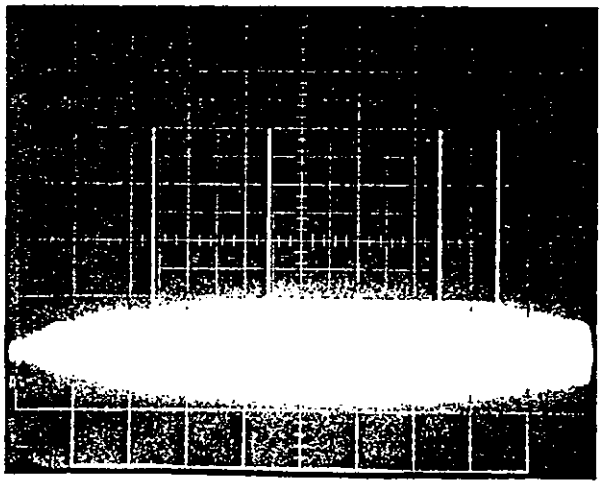
SIGNAL AND SOURCE	SETTINGS
CARD (R) WO486-8A/INTERFACE TP-2 (Blue) Ground reference is 2 Divisions below center	TRIGGER Internal (+) MODE Main Sweep HORIZONTAL: 5 uSec/Div VERTICAL: 0.1 V/Div

Figure 5.51. 100-kHz Input



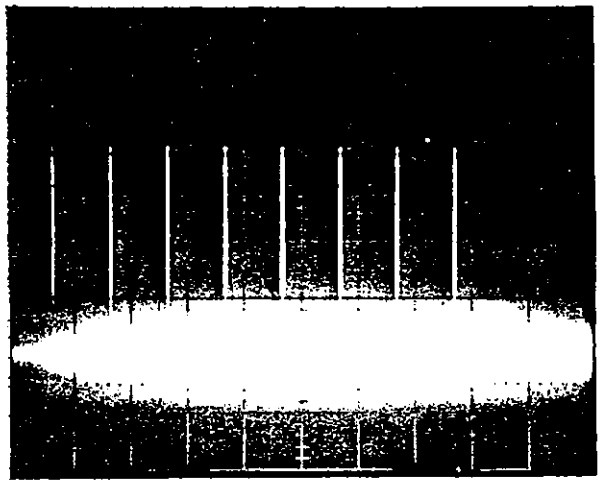
SIGNAL AND SOURCE	SETTINGS
CARD (R) WO486-8A/INTERFACE TP-3 (Green) Ground reference is 2 Divisions below center	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Main Sweep HORIZONTAL: 1 mSec/Div VERTICAL: 0.5 V/Div

Figure 5.52. Phase Code Reset



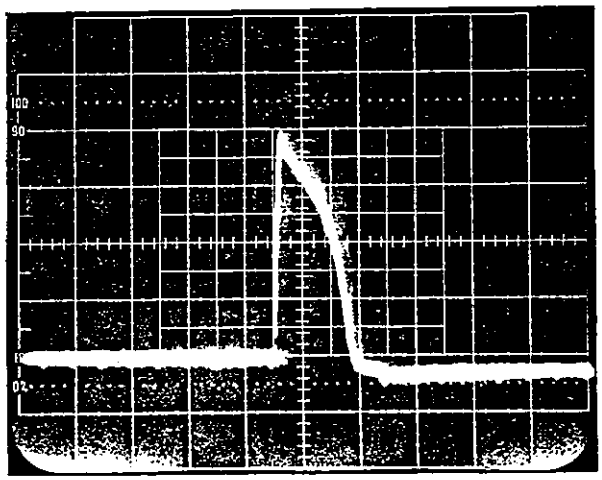
SIGNAL AND SOURCE	SETTINGS
CARD (R) WO486-8A/INTERFACE TP-4 (Brown) Ground reference is 2 Divisions below center	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Main Sweep HORIZONTAL: 1 mSec/Div VERTICAL: 0.5 V/Div

Figure 5.53. Phase Code Set



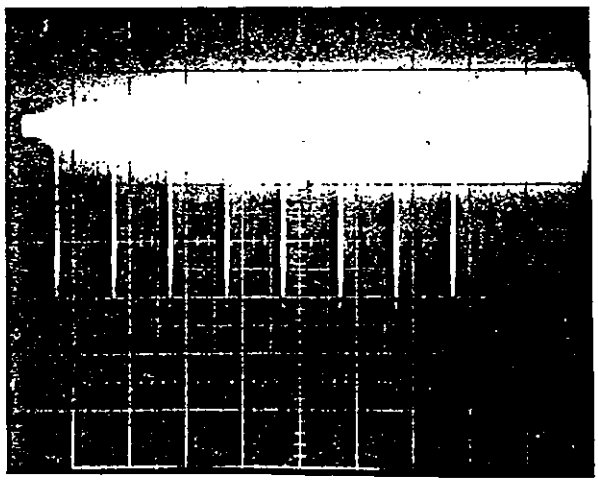
SIGNAL AND SOURCE	SETTINGS
CARD (R) WO486-8A/INTERFACE TP-5 (Orange) Ground reference is 2 Divisions below center	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Main Sweep HORIZONTAL: 1 mSec/Div VERTICAL: 0.5 V/Div

Figure 5.54. (+) MPT Output



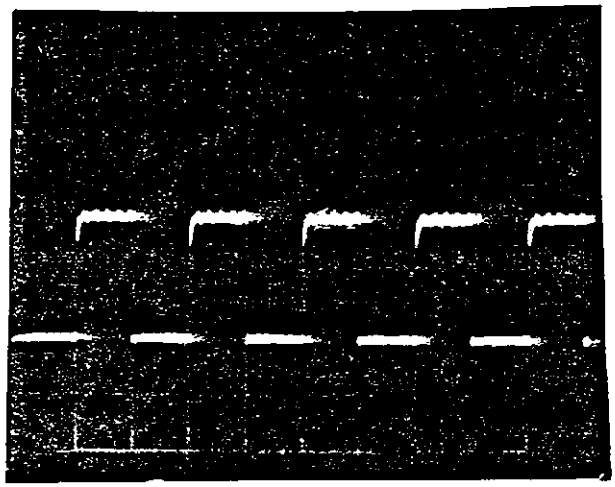
SIGNAL AND SOURCE	SETTINGS
CARD (R) WO486-8A/INTERFACE TP-5 (Orange) Operate Timer Ground reference is 2 Divisions below center	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Main Sweep 1.0 mSec/Div Sweep Delay 2 uSec/Div HORIZONTAL: 2 uSec/Div Delayed VERTICAL: 0.5 V/Div

Figure 5.55. MPT Output (Expanded)



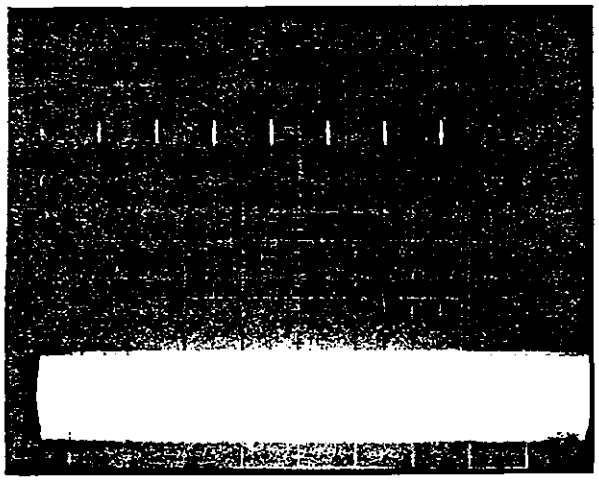
SIGNAL AND SOURCE	SETTINGS
CARD (R) WO486-8A/INTERFACE TP-6 (Yellow) Ground reference is 2 Divisions above center	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Main Sweep HORIZONTAL: 1 mSec/Div VERTICAL: 0.2 V/Div

Figure 5.56. (-) MPT Output



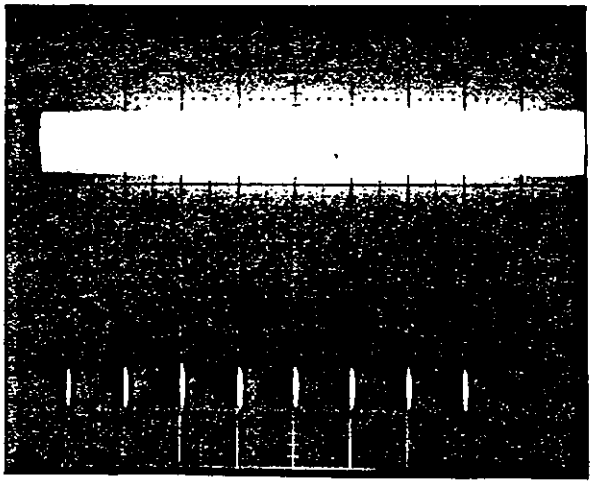
SIGNAL AND SOURCE	SETTINGS
CARD (T) WO486-28B/DRINT/CP TP-2 (Red) Ground reference is 2 Divisions below center	TRIGGER Internal (-) MODE Main Sweep HORIZONTAL: 5 uSec/Div VERTICAL: 0.2 V/Div

Figure 5.57. 100 kHz



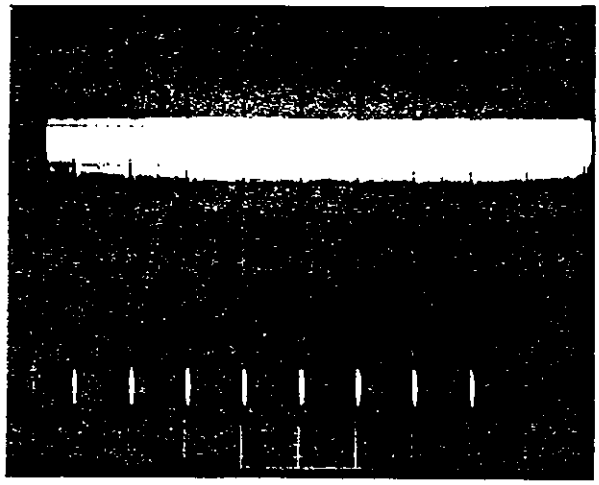
SIGNAL AND SOURCE	SETTINGS
CARD (T) WO486-28B/DRINT/CP TP-3 (Blue) Ground reference is 2 Divisions below center	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Main Sweep HORIZONTAL: 1 mSec/Div VERTICAL: 0.1 mV/Div

Figure 5.58. Multipulse Triggers



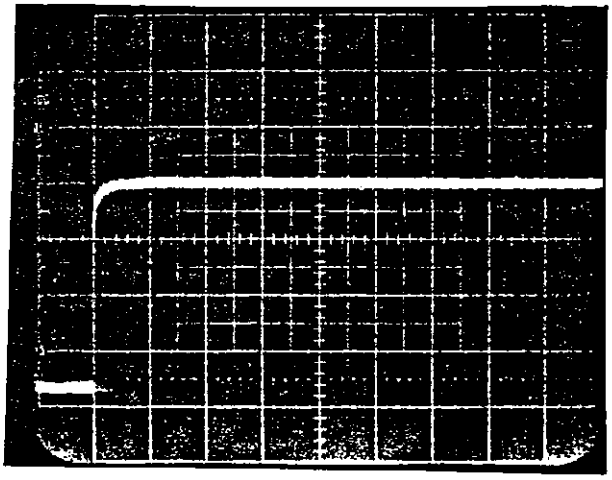
SIGNAL AND SOURCE	SETTINGS
CARD (T) WO486-28B/DRINT/CP TP-4 (Gray) Ground reference is 2 Divisions below center	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Main Sweep HORIZONTAL: 1 mSec/Div VERTICAL: 0.1 V/Div

Figure 5.59. Reclock Pulse Width



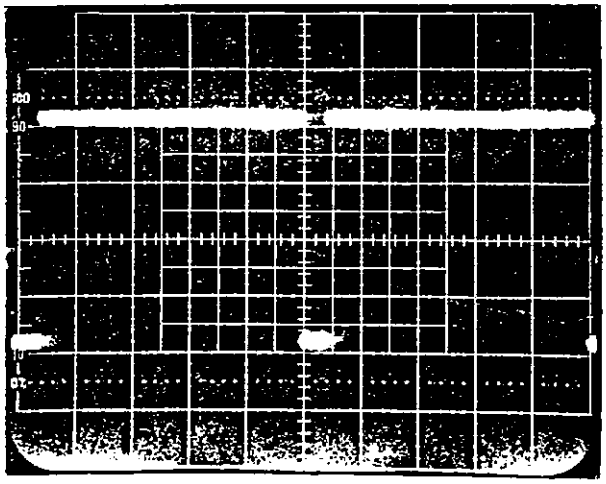
SIGNAL AND SOURCE	SETTINGS
CARD (T) WO486-28B/DRINT/CP TP-5 (Orange) Ground reference is 1 Division above center	TRIGGER Internal (-) MODE Main Sweep HORIZONTAL: 1 mSec/Div VERTICAL: 0.1 V/Div

Figure 5.60. Multipulse Triggers



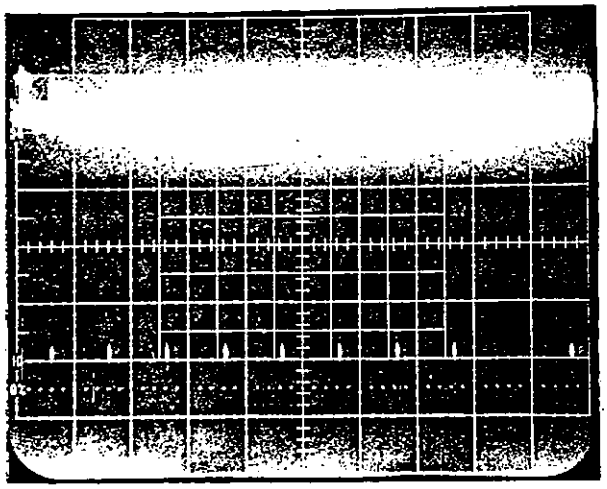
SIGNAL AND SOURCE	SETTINGS
CARD (T) WO486-28B/DRINT/CP TP-5 (Orange) Ground reference is 1 Division above center	TRIGGER Internal (-) MODE Main Sweep HORIZONTAL: 20 uSec/Div VERTICAL: 0.1 V/Div

Figure 5.61. Multipulse Trigger (Expanded)



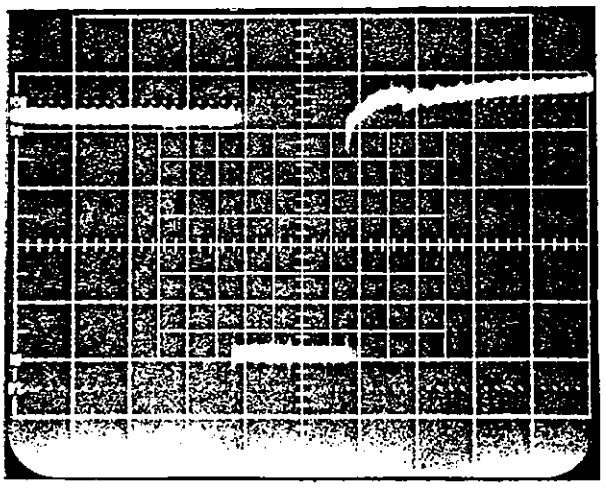
SIGNAL AND SOURCE	SETTINGS
CARD (T) WO486-28B/DRINT/CP TP-6 (Yellow) Ground reference is 2 Divisions below center NOTE: Signal shown for Dual-rated station. At Single-rate station, this signal is a constant (5 Volt) level.	TRIGGER Internal (-) MODE Main Sweep HORIZONTAL: 20 mSec/Div VERTICAL: 0.1 V/Div

Figure 5.62. Blanking Waveform



SIGNAL AND SOURCE	SETTINGS
CARD (T) WO486-28B/DRINT/CP TP-7 (Green) Ground reference is 2 Divisions below center	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Main Sweep HORIZONTAL: 1 mSec/Div VERTICAL: 0.1 V/Div

Figure 5.63. Early Multipulse Triggers



SIGNAL AND SOURCE	SETTINGS
CARD (T) WO486-28B/DRINT/CP TP-7 (Green) Ground reference is 2 Divisions below center	TRIGGER DRRG Cards E,F, or G TP-7 (RED) External (-) MODE Main Sweep 1 mSec/Div Sweep Delay 5 uSec/Div HORIZONTAL: 5 uSec/Div Delayed VERTICAL: 0.1 V/Div

Figure 5.64. Early Multipulse Trigger (Expanded)

5.12.5. Timer Wire Lists. Table 5.4 contains a listing of the interconnect wires in the TD-989A/FPN-54A Loran-C Timer. Table 5.5 contains a listing of the interconnect wires in the TD-1365/FPN-65 Loran-C Timer. Each may be used as an aid in signal tracing and general troubleshooting.

Table 5.4. TD-989A/FPN-54A Timer Wire List

PIN	FROM	TO	CABLES	WIRE NAME
A:1		B:51		CDA 10 8
A:2	S:71			STANDBY LAMP
A:3		B:53		CDA 10 4
A:4				+24V
A:5		B:55		CDA 10 2
A:6	S:69			OPERATE LAMP
A:7		B:43		CDA 100 8
A:8		B:28		LOC/REM SHIFT
A:9		B:45		CDA 100 4
A:10		B:30		LOC/REM SHIFT
A:11		B:47		CDA 100 2
A:12				+5V (Vcc)
A:13		B:49		CDA 100 1
A:14				GND
A:15		B:35		CDA 1K 8
A:16	C:14			LOC/REM LAMP
A:17		B:37		CDA 1K 4
A:18	B:14			LOC/REM LAMP
A:19		B:39		CDA 1K 2
A:20	J:39			NO EXT AGMT DVR
A:21		B:41		CDA 1K 1
A:22		B:77		CDA 0.02 4
A:23		B:27		CDA 10K 8
A:24		B:79		CDA 0.02 2
A:25		B:29		CDA 10K 4
A:26		B:81		CDA 0.02 1
A:27		B:31		CDA 10K 2
A:28		B:67		CDA 0.1 8
A:29		B:33		CDA 10K 1
A:30		B:69		CDA 0.1 4
A:31		B:19		CDA 100K 8
A:32		B:71		CDA 0.1 2
A:33		B:21		CDA 100K 4
A:34		B:73		CDA 0.1 1
A:35		B:23		CDA 100K 2
A:36		B:59		CDA 1.0 8
A:37		B:25		CDA 100K 1
A:38		B:61		CDA 1.0 4
A:39				GND
A:40		B:63		CDA 1.0 2
A:41		B:9		SHIFT RIGHT
A:42		B:65		CDA 1.0 1
A:43		B:7		SHIFT LEFT
A:44		B:57		CDA 10 1
A:45				+5V (Vcc)
A:46				+24V
A:47				GND
A:48				GND

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
A:49		B:36		CLEAR
A:50		P:66		LOCAL BLINK Sw
A:51	C:12			CLEAR LAMP
A:52				+5V (Vcc)
A:53		B:32		LOAD
A:54	P:62			BLINK LAMP
A:55	C:8			LOAD LAMP
A:56		P:72		LOCAL BLINK Sx
A:57		B:11		EXECUTE
A:58		P:76		LOCAL BLINK Sy
A:59				+24V
A:60		P:64		LOCAL BLINK Sz
A:61	C:10			EXECUTE LAMP
A:62	R:48			LOST XMTR DRIVE LAMP
A:63	J:37			RESET TO EXT DVR
A:64				+24V
A:65		J:35		LOC RESET TO EXT
A:66	C:16	J:80		LAMP TEST
A:67	J:76			DRRG #2 JUMP
A:68				+5V (Vcc)
A:69	J:74			DRRG #3 JUMP
A:70				GND
A:71	J:41			CHECK TIMING DVR
A:72				GND
A:73		J:50		CHECK TIMING RESET
A:74		L:80		LOCAL LSD 1 ETA
A:75				+5V (Vcc)
A:76		L:78		LOCAL LSD 2 ETA
A:77				GND
A:78		L:72		LOCAL LSD 4 ETA
A:79	J:78			DRRG #1 JUMP
A:80		L:70		LOCAL LSD 8 ETA
A:81		S:49		+24 VDC
A:82		L:64		LOCAL MSD 1 ETA
A:83				
A:84		L:62		LOCAL MSD 2 ETA
A:85		L:54		LOCAL MSD 8 ETA
A:86		L:56		LOCAL MSD 4 ETA
B:1				GND
B:2		B:22		GND
B:3		B:13		+5V (Vcc)
B:4				+5V (Vcc)
B:5		D:41		SHIFT DIRECTION
B:6				CLEAR
B:7	A:43			SHIFT LEFT
B:8		C:8		LOAD LAMP

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
B:9	A:41			SHIFT RIGHT
B:10		C:10		EXECUTE LAMP
B:11	A:57			EXECUTE
B:12		C:12		CLEAR LAMP
B:13	B:3			LOC/REM SHIFT INHIBIT
B:14		A:18		LOC/REM LAMP
B:15				LOC/REM SHIFT INHIBIT
B:16		C:16		LAMP TEST
B:17				EXECUTE
B:18				LOC/REM SECONDARY
B:19	A:31			CDA 100K 8
B:20	C:56			LOC/REM SHIFT
B:21	A:33			CDA 100K 4
B:22	B:2			LOC/REM SECONDARY
B:23	A:35			CDA 100K 2
B:24		L:50		LOCAL/REMOTE
B:25	A:37			CDA 100K 1
B:26		C:22		LOCAL/REMOTE
B:27	A:23			CDA 10K 8
B:28	A:8			LOC/REM SHIFT
B:29	A:25			CDA 10K 4
B:30	A:10			LOC/REM SHIFT
B:31	A:27			CDA 10K 2
B:32	A:53			LOAD
B:33	A:29			CDA 10K 1
B:34		D:35		SHIFT PULSE
B:35	A:15			CDA 1K 8
B:36	A:49			CLEAR
B:37	A:17			CDA 1K 4
B:38				LOAD
B:39	A:19			CDA 1K 2
B:40				
B:41	A:21			CDA 1K 1
B:42				
B:43	A:7			CDA 100 8
B:44				
B:45	A:9			CDA 100 4
B:46				
B:47	A:11			CDA 100 2
B:48				
B:49	A:13			CDA 100 1
B:50				
B:51	A:1			CDA 10 8
B:52				
B:53	A:3			CDA 10 4
B:54				
B:55	A:5			CDA 10 2
B:56				
B:57	A:44			CDA 10 1

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
B:58				
B:59	A:36			CDA 1.0 8
B:60				
B:61	A:38			CDA 1.0 4
B:62				
B:63	A:40			CDA 1.0 2
B:64				
B:65	A:42			CDA 1.0 1
B:66				
B:67	A:28			CDA 0.1 8
B:68				
B:69	A:30			CDA 0.1 4
B:70				
B:71	A:32			CDA 0.1 2
B:72				
B:73	A:34			CDA 0.1 1
B:74				
B:75	B:83			CDA 0.02 8
B:76				
B:77	A:22			CDA 0.02 4
B:78				
B:79	A:24			CDA 0.02 2
B:80				
B:81	A:26			CDA 0.02 1
B:82				
B:83		B:75		+5V (Vcc)
B:84				+5V (Vcc)
B:85				GND
B:86				GND
C:1		C:19		GND
C:2				GND
C:3		C:20		+5V (Vcc)
C:4		C:28		+5V (Vcc)
C:5		D:39		SHIFT DIRECTION
C:6			J3-z	CLEAR
C:7			J3-g	SHIFT LEFT
C:8	B:8	A:55		LOAD LAMP
C:9			J3-a	SHIFT RIGHT
C:10	B:10	A:61		EXECUTE LAMP
C:11			J3-DD	EXECUTE
C:12	B:12	A:51		CLEAR LAMP
C:13				LOC/REM SHIFT INHIBIT
C:14		A:16		LOC/REM LAMP
C:15				LOC/REM SHIFT INHIBIT
C:16	B:16	A:66		LAMP TEST
C:17			J3-p	EXECUTE
C:18	C:22			LOC/REM SECONDARY

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
C:19	C:1	C:25	J3-b	CDA 100K 8
C:20	C:3	C:21		LOC/REM SHIFT
C:21	C:20	C:23		CDA 100K 4
C:22	B:26	C:18		LOC/REM SECONDARY
C:23	C:21	C:29		CDA 100K 2
C:24				LOCAL/REMOTE
C:25	C:19	C:27	J3-V	CDA 100K 1
C:26			J3-AA	LOCAL/REMOTE
C:27	C:25	C:33	J3-U	CDA 10K 8
C:28	C:4	C:30		LOC/REM SHIFT
C:29	C:23	C:31		CDA 10K 4
C:30	C:28			LOC/REM SHIFT
C:31	C:29	C:37		CDA 10K 2
C:32			J3-H	LOAD
C:33	C:27	C:35	J3-f	CDA 10K 1
C:34		D:33		SHIFT PULSE
C:35	C:33	C:41	J3-e	CDA 1K 8
C:36			J3-G	CLEAR
C:37	C:31	C:39		CDA 1K 4
C:38				LOAD LOGIC
C:39	C:37	C:45		CDA 1K 2
C:40	J:5		J3-J	RESET TO EXTERNAL
C:41	C:35	C:43	J3-CC	CDA 1K 1
C:42	J:11		J3-T	NO EXT AGMT LAMP
C:43	C:41	C:49	J3-BB	CDA 100 8
C:44	J:9		J3-v	CHECK TIMING LAMP
C:45	C:39	C:47		CDA 100 4
C:46	J:7		J3-w	ALARM DRIVER
C:47	C:45	C:53		CDA 100 2
C:48		J:32	J3-x	REM RESET TO EXT
C:49	C:43	C:51	J3-d	CDA 100 1
C:50	P:22		J3-y	BLINK
C:51	C:49	C:57	J3-c	CDA 10 8
C:52				
C:53	C:47	C:55		CDA 10 4
C:54				
C:55	C:53	C:56		CDA 10 2
C:56	C:55	B:20		LOC/REM SHIFT
C:57	C:51		J3-u	CDA 10 1
C:58		P:80	J3-K	REMOTE BLINK Sx
C:59			J3-t	CDA 1.0 8
C:60		P:78	J3-L	REMOTE BLINK Sy
C:61			J3-s	CDA 1.0 4
C:62		P:70	J3-M	REMOTE BLINK Sz
C:63			J3-Z	CDA 1.0 2
C:64		P:68	J3-h	REMOTE BLINK Sw
C:65			J3-r	CDA 1.0 1
C:66	J:10		J3-i	LOSS XMTR DRIVE

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
C:67			J3-q	CDA 0.1 8
C:68		L:52	J3-j	REMOTE MSD 8 ETA
C:69			J3-F	CDA 0.1 4
C:70		L:58	J3-N	REMOTE MSD 4 ETA
C:71			J3-E	CDA 0.1 2
C:72		L:60	J3-P	REMOTE MSD 2 ETA
C:73			J3-D	CDA 0.1 1
C:74		L:66	J3-R	REMOTE MSD 1 ETA
C:75	C:83		J3-Y	CDA 0.02 8
C:76		L:68	J3-k	REMOTE LSD 8 ETA
C:77			J3-X	CDA 0.02 4
C:78		L:74	J3-m	REMOTE LSD 4 ETA
C:79			J3-W	CDA 0.02 2
C:80		L:76	J3-n	REMOTE LSD 2 ETA
C:81			J3-C	CDA 0.02 1
C:82		L:82	J3-S	REMOTE LSD 1 ETA
C:83		C:75		+5V (Vcc)
C:84				+5V (Vcc)
C:85			J3-A	GND
C:86			J3-B	GND
D:1		D:9		GND
D:2				GND
D:3				+5V (Vcc)
D:4		D:12		+5V (Vcc)
D:5				GATED 100 KHZ
D:6				100 KHZ, 100us STROBE
D:7				100 KHZ SQUAREWAVE
D:8				100 KHZ, 1us STROBE
D:9	D:1	D:15		100 KHZ GATING
D:10				100 KHZ SQUAREWAVE
D:11				GATED 1 MHZ
D:12	D:4	D:18		DIVIDER RESET
D:13				GATED 5 MHZ
D:14				BUFFERED 5 MHZ
D:15	D:9	D:17		5 MHZ GATING
D:16		D:40		BUFFERED 5 MHZ
D:17	D:15			1 MHZ GATING
D:18	D:12	D:37		COMPARATOR INHIBIT
D:19	D:28			P3 DECIMAL COUNTER BCD PARALLEL
D:20		J:33		EXT PHASE SHIFT AGREE
D:21	D:26			P2 DECIMAL COUNTER BCD PARALLEL
D:22	D:25			B0 DIGITAL COMPARE BCD
D:23	S:5	D:24		P1 COUNT BCD PARALLEL
D:24	D:23			B1 DIGITAL COMPARE BCD
D:25	S:3	D:22		P0 COUNT BCD PARALLEL
D:26	S:7	D:21		B2 DIGITAL COMPARE BCD

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
D:27				PARALLEL ENTRY SHIFT PULSE
D:28	S:9	D:19		B3 DIGITAL COMPARATOR BCD
D:29	J:15			SHIFT PULSE
D:30		S:11		Q0 DECIMAL COUNTER BCD
D:31	J:27			PARALLEL ENTRY COMMAND
D:32		S:13		Q1 DECIMAL COUNTER BCD
D:33	C:34			SHIFT PULSE
D:34		S:15		Q2 DECIMAL COUNTER BCD
D:35	B:34			SHIFT PULSE
D:36		S:17		Q3 DECIMAL COUNTER BCD
D:37	D:18			SHIFT DIRECTION COMMAND
D:38				DECIMAL COUNTER TERM COUNT
D:39	C:5			SHIFT DIRECTION
D:40	D:16	E:74		0-SHIFTED COUNTER SYNCH.
D:41	B:5			SHIFT DIRECTION
D:42				
D:43				
D:44				
D:45				
D:46				
D:47				
D:48				
D:49				
D:50				
D:51				
D:52				
D:53				
D:54				
D:55				
D:56				
D:57				
D:58				
D:59				
D:60				
D:61				
D:62				
D:63				
D:64				
D:65				
D:66				
D:67				
D:68				
D:69				
D:70				
D:71				
D:72				
D:73				
D:74				

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
D:75				
D:76				
D:77	S:65			5 MHZ SINE WAVE
D:78				
D:79				5 MHZ SQUARE WAVE
D:80				PHASE SHIFTED 5 MHZ
D:81		D:82		5 MHZ SQUARE WAVE
D:82	D:81			5 MHZ SQUARE WAVE
D:83				+5V (Vcc)
D:84				+5V (Vcc)
D:85	S:67			GND
D:86				GND
E:1				GND
E:2		E:38		GND
E:3				+5V (Vcc)
E:4				+5V (Vcc)
E:5		H:57		1 D64
E:6				1 LFF2 RESET
E:7		H:59		1 D63
E:8	E:71			1 LFF3 RESET
E:9				1 D62
E:10	E:75			1 LFF3 SET
E:11		H:47		1 D69
E:12		J:21		1 LFF3
E:13		H:49		1 D68
E:14				1 LFF2 SET
E:15		H:51		1 D67
E:16				1 LFF2
E:17		H:53		1 D66
E:18		E:26		1 DRRG 0
E:19		H:55		1 D65
E:20		J:56		1,3 DRRG LOSS
E:21				1 D61
E:22		J:64		1,3 INTERVAL LORTO
E:23				1 D51
E:24		F:80		1 LORTO
E:25				1 D52
E:26	E:18	F:78	J2-a	1 DRRG INTERVAL
E:27				1 D54
E:28		H:63		1 D59
E:29				1 D53
E:30				1 D58
E:31				1 D55
E:32				1 D57
E:33		H:61		1 D50
E:34				1 D56

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
E:35		H:79		1 D43
E:36	E:60			1 RESET
E:37		H:77		1 D44
E:38	E:2			1 RO RATE SET
E:39		H:81		1 D42
E:40	H:41			1 R1 RATE SET
E:41				1 D41
E:42	H:43			1 R2 RATE SET
E:43		H:65		1 D40
E:44		H:67		1 D49
E:45				1 D30
E:46		H:69		1 D48
E:47				1 D32
E:48		H:71		1 D47
E:49				1 D33
E:50		H:73		1 D46
E:51				1 D34
E:52		H:75		1 D45
E:53				1 D31
E:54	H:45			1 R3 RATE SET
E:55				1 D39
E:56	H:39			1 T1 TRIGGER SET
E:57				1 D38
E:58				
E:59				1 D37
E:60	J:79	E:36		1 EXTERNAL RESET
E:61				1 D36
E:62				DIVIDER CONTROL
E:63				1 D35
E:64	E:70			COUNT SET
E:65				1 D21
E:66	E:84			1 D2 PRESET
E:67				1 D22
E:68				1 D24
E:69				1 D23
E:70		E:64		1 D14
E:71		E:8		1 D29
E:72				1 D10
E:73				1 D27
E:74	D:40	F:74		5 MHZ CLOCK
E:75		E:10		1 D26
E:76				1 D60
E:77				1 D25
E:78	G:26	K:13		CHECK INTERVAL
E:79				1 D28
E:80	G:24	J:68		CHECK LORTO
E:81				1 D20
E:82		R:18		COUNT ENABLE

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
E:83				+5V (Vcc)
E:84		E:66		+5V (Vcc)
E:85				GND
E:86				GND
F:1				GND
F:2		F:38		GND
F:3				+5V (Vcc)
F:4				+5V (Vcc)
F:5		H:68		2 D64
F:6				2 LFF2 RESET
F:7		H:70		2 D63
F:8	F:71			2 LFF3 RESET
F:9				2 D62
F:10	F:75			2 LFF3 SET
F:11		H:58		2 D69
F:12		J:19		2 LFF3
F:13		H:60		2 D68
F:14				2 LFF2 SET
F:15		H:62		2 D67
F:16				2 LFF2
F:17		H:64		2 D66
F:18		F:26		2 DRRG 0
F:19		H:66		2 D65
F:20		J:54		1,2 DRRG LOSS
F:21				2 D61
F:22		J:66		1,2 INTERVAL LORTO
F:23				2 D51
F:24		G:80		2 LORTO
F:25				2 D52
F:26	F:18	G:78		2 DRRG INTERVAL
F:27				2 D54
F:28		H:56		2 D59
F:29				2 D53
F:30				2 D58
F:31				2 D55
F:32				2 D57
F:33		H:54		2 D50
F:34				2 D56
F:35		H:19		2 D43
F:36	F:60			2 RESET
F:37		H:21		2 D44
F:38	F:2			2 R0 RATE SET
F:39		H:17		2 D42
F:40	H:37			2 R1 RATE SET
F:41				2 D41
F:42	H:52			2 R2 RATE SET
F:43		H:33		2 D40

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
F:44		H:31		2 D49
F:45				2 D30
F:46		H:29		2 D48
F:47				2 D32
F:48		H:27		2 D47
F:49				2 D33
F:50		H:25		2 D46
F:51				2 D34
F:52		H:23		2 D45
F:53				2 D31
F:54	H:50			2 R3 RATE SET
F:55				2 D39
F:56	H:35			2 T1 TRIGGER SET
F:57				2 D38
F:58				
F:59				2 D37
F:60	J:77	F:36		2 EXTERNAL RESET
F:61				2 D36
F:62				DIVIDER CONTROL
F:63				2 D35
F:64	F:70			COUNT SET
F:65				2 D21
F:66	F:84			2 D2 PRESET
F:67				2 D22
F:68				2 D24
F:69				2 D23
F:70		F:64		2 D14
F:71		F:8		2 D29
F:72				2 D10
F:73				2 D27
F:74	E:74	G:74		5 MHZ CLOCK
F:75		F:10		2 D26
F:76				2 D60
F:77				2 D25
F:78	E:26	K:9		CHECK INTERVAL
F:79				2 D28
F:80	E:24	J:73		CHECK LORTO
F:81				2 D20
F:82		R:20		COUNT ENABLE
F:83				+5V (Vcc)
F:84		F:66		+5V (Vcc)
F:85				GND
F:86				GND
G:1				GND
G:2		G:38		GND
G:3				+5V (Vcc)
G:4				+5V (Vcc)
G:5		H:30		3 D64

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
G:6				3 LFF2 RESET
G:7		H:28		3 D63
G:8	G:71			3 LFF3 RESET
G:9				3 D62
G:10	G:75			3 LFF3 SET
G:11		H:40		3 D69
G:12		J:17		3 LFF3
G:13		H:38		3 D68
G:14				3 LFF2 SET
G:15		H:36		3 D67
G:16				3 LFF2
G:17		H:34		3 D66
G:18		G:26		3 DRRG 0
G:19		H:32		3 D65
G:20		J:58		2,3 DRRG LOSS
G:21				3 D61
G:22		J:62		2,3 INTERVAL LORTO
G:23				3 D51
G:24		E:80		3 LORTO
G:25				3 D52
G:26	G:18	E:78		3 DRRG INTERVAL
G:27				3 D54
G:28		H:24		3 D59
G:29				3 D53
G:30				3 D58
G:31				3 D55
G:32				3 D57
G:33		H:26		3 D50
G:34				3 D56
G:35		H:8		3 D43
G:36	G:60			3 RESET
G:37		H:10		3 D44
G:38	G:2			3 RO RATE SET
G:39		H:6		3 D42
G:40	H:46			3 R1 RATE SET
G:41				3 D41
G:42	H:44			3 R2 RATE SET
G:43		H:22		3 D40
G:44		H:20		3 D49
G:45				3 D30
G:46		H:18		3 D48
G:47				3 D32
G:48		H:16		3 D47
G:49				3 D33
G:50		H:14		3 D46
G:51				3 D34
G:52		H:12		3 D45
G:53				3 D31

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
G:54	H:42			3 R3 RATE SET
G:55				3 D39
G:56	H:48			3 T1 TRIGGER SET
G:57				3 D38
G:58				
G:59				3 D37
G:60	J:75	G:36		3 EXTERNAL RESET
G:61				3 D36
G:62				DIVIDER CONTROL
G:63				3 D35
G:64	G:70			COUNT SET
G:65				3 D21
G:66	G:84			3 D2 PRESET
G:67				3 D22
G:68				3 D24
G:69				3 D23
G:70		G:64		3 D14
G:71		G:8		3 D29
G:72				3 D10
G:73				3 D27
G:74	F:74	J:23		5 MHZ CLOCK
G:75		G:10		3 D26
G:76				3 D60
G:77				3 D25
G:78	F:26	K:11		CHECK INTERVAL
G:79				3 D28
G:80	F:24	J:71		CHECK LORTO
G:81				3 D20
G:82		R:22		COUNT ENABLE
G:83				+5V (Vcc)
G:84		G:66		+5V (Vcc)
G:85				GND
G:86				GND
H:1				GND
H:2				GND
H:3				+5V (Vcc)
H:4				+5V (Vcc)
H:5	P:34			MASTER BLINK CODE
H:6	G:39			3 D42 (200)
H:7	P:36			SECONDARY BLINK CODE
H:8	G:35			3 D43 (300)
H:9		P:22		BLINK
H:10	G:37			3 D44 (400)
H:11	P:46			MASTER
H:12	G:52	K:15		3 D45 (500)
H:13	P:48			SECONDARY
H:14	G:50			3 D46 (600)
H:15		P:56		BLINK SET

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
H:16	G:48			3 D47 (700)
H:17	F:39			2 D42 (200)
H:18	G:46			3 D48 (800)
H:19	F:35			2 D43 (300)
H:20	G:44	K:23		3 D49 (900)
H:21	F:37			2 D44 (400)
H:22	G:43			3 D40 (000)
H:23	F:52	K:16		2 D45 (500)
H:24	G:28			3 D59 (9K)
H:25	F:50			2 D46 (600)
H:26	G:33			3 D50 (0000)
H:27	F:48			2 D47 (700)
H:28	G:7			3 D63 (30K)
H:29	F:46			2 D48 (800)
H:30	G:5			3 D64 (40K)
H:31	F:44	K:27		2 D49 (900)
H:32	G:19			3 D65 (50K)
H:33	F:43			2 D40 (000)
H:34		G:17		3 D66 (60K)
H:35		F:56		2 T1 SCOPE TRIGGER
H:36	G:15			3 D67 (70K)
H:37		F:40		2 R1 RATE SET (GRI-100)
H:38	G:13			3 D68 (80K)
H:39		E:56		1 T1 SCOPE TRIGGER
H:40	G:11			3 D69 (90K)
H:41		E:40		1 R1 RATE SET (GRI-100)
H:42		G:54		3 R3 RATE SET (GRI-10K)
H:43		E:42		1 R2 RATE SET (GRI-1K)
H:44		G:42		3 R2 RATE SET (GRI-1K)
H:45		E:54		1 R3 RATE SET (GRI-10K)
H:46		G:40		3 R1 RATE SET (GRI-100)
H:47	E:11			1 D69 (90K)
H:48		G:56		3 T1 SCOPE TRIGGER
H:49	E:13			1 D68 (80K)
H:50		F:54		2 R3 RATE SET (GRI-10K)
H:51	E:15			1 D67 (70K)
H:52		F:42		2 R2 RATE SET (GRI-1K)
H:53	E:17			1 D66 (60K)
H:54	F:33			2 D50 (0000)
H:55	E:19			1 D65 (50K)
H:56	F:28			2 D59 (9K)
H:57	E:5			1 D64 (40K)
H:58	F:11			2 D69 (90K)
H:59	E:7			1 D63 (30K)
H:60	F:13			2 D68 (80K)
H:61	E:33			1 D50 (0000)
H:62	F:15			2 D67 (70K)
H:63	E:28			1 D59 (9K)

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
H:64	F:17			2 D66 (60K)
H:65	E:43			1 D40 (000)
H:66	F:19			2 D65 (50K)
H:67	E:44	K:19		1 D49 (900)
H:68	F:5			2 D64 (40K)
H:69	E:46			1 D48 (800)
H:70	F:7			2 D63 (30K)
H:71	E:48			1 D47 (700)
H:72	K:80			MASTER RESET
H:73	E:50			1 D46 (600)
H:74	K:78			SECONDARY RESET
H:75	E:52	K:12		1 D45 (500)
H:76		K:31		LOCAL INTERVAL RESET
H:77	E:37			1 D44 (400)
H:78		K:10		P.C. CONTROL
H:79	E:35			1 D43 (300)
H:80				
H:81	E:39			1 D42 (200)
H:82				
H:83				+5V (Vcc)
H:84				+5V (Vcc)
H:85				GND
H:86				GND
J:1				GND
J:2				GND
J:3				+5V (Vcc)
J:4				+5V (Vcc)
J:5		C:40		RESET TO EXTERNAL
J:6				
J:7		C:46		ALARM DRIVER
J:8	J:40			NO EXT. ALARM
J:9		C:44		CHECK TIMING LAMP
J:10	R:52	C:66		LOST XMTR DRIVE
J:11		C:42		NO EXT AGMT LAMP
J:12		S:59		LOSS ALARM DRIVER
J:13				
J:14				
J:15		D:29		SHIFT PULSE
J:16		M:12		MAJORITY
J:17	G:12			SOURCE 3
J:18				CP
J:19	F:12			SOURCE 2
J:20				
J:21	E:12			SOURCE 1
J:22				
J:23	G:74	M:32		5 MHZ CLOCK

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
J:24				
J:25				
J:26				
J:27		D:31		0-SHIFT RESET TO EXTERNAL
J:28	J:30			CLOCK ENABLE
J:29				
J:30		J:28		0-SHIFT CLOCK SET
J:31				
J:32	C:48			REM RESET TO EXT
J:33	D:20			EXT PHASE SHIFT AGREE
J:34				
J:35	A:65			LOC RESET TO EXT
J:36				
J:37		A:63		RESET TO EXT DVR
J:38				
J:39		A:20		NO EXT AGMT DVR
J:40		J:8		NO EXT. ALARM
J:41		A:71		CHECK TIMING DVR
J:42				
J:43		K:41		LOST MAJORITY
J:44	S:55			EXT MAJ INT LORTO
J:45				MAJORITY LORTO
J:46				
J:47				MAJORITY INTERVAL LORTO
J:48				LOST MAJORITY
J:49				
J:50	A:73			CHECK TIMING RESET
J:51				
J:52		S:53		MAJ INT LORTO
J:53				
J:54	F:20			1,2 DRRG LOSS
J:55				
J:56	E:20			1,3 DRRG LOSS
J:57				
J:58	G:20			2,3 DRRG LOSS
J:59				
J:60				
J:61				
J:62	G:22			2,3 INTERVAL LORTO
J:63				
J:64	E:22			1,3 INTERVAL LORTO
J:65				
J:66	F:22			1,2 INTERVAL LORTO
J:67				
J:68	E:80			LORTO DRRG #3
J:69				
J:70		J:72		NO MAJORITY RESET
J:71	G:80			LORTO DRRG #2

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
J:72	J:70			NO MAJORITY RESET
J:73	F:80			LORTO DRRG #1
J:74		A:69		DRRG #3 JUMP
J:75		G:60		DRRG #3 RESET
J:76		A:67		DRRG #2 JUMP
J:77		F:60		DRRG #2 RESET
J:78		A:79		DRRG #1 JUMP
J:79		E:60		DRRG #1 RESET
J:80	A:66	P:60		LAMP TEST
J:81				
J:82				
J:83				+5V (Vcc)
J:84				+5V (Vcc)
J:85				GND
J:86				GND
K:1				GND
K:2				GND
K:3				+5V (Vcc)
K:4				+5V (Vcc)
K:5		T:38		PMPT 9
K:6	G:52	K:15		05-L1
K:7		M:16		PMPT 8
K:8	K:12			05-L2
K:9	F:78			PCI-L1 DRRG #1
K:10	H:78			MAS/SEC SELECT
K:11	G:78			PCI-L2 DRRG #2
K:12	H:75	K:8		05-L2
K:13	E:78			PCI-L3 DRRG #3
K:14	F:52	K:16		05-L3
K:15	H:12	K:6		05-L1
K:16	H:23	K:14		05-L3
K:17	K:19			09-L2
K:18				
K:19	H:67	K:17		09-L2
K:20		T:60		PHASE CODE INTERVAL
K:21	K:23			09-L1
K:22				
K:23	H:20	K:21		09-L1
K:24				
K:25	K:27			09-L3
K:26				
K:27	H:31	K:25		09-L3
K:28				
K:29				
K:30				
K:31	H:76			LOCAL INTERVAL RESET
K:32				
K:33	M:68	T:22		LOCAL INTERVAL

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
K:34				
K:35				
K:36				
K:37				LOCAL INTERVAL
K:38				
K:39				
K:40		M:11		PHASE CODE
K:41	J:43	M:60		LORTO
K:42	M:13	R:49		PHASE CODE
K:43				
K:44				TUBE/SSX SELECT
K:45				
K:46				
K:47				
K:48	T:55			1 MHZ
K:49				100 KHZ DELAYED
K:50				
K:51				
K:52				
K:53				EXT. OSC.
K:54				
K:55				OSC. DISABLE
K:56				
K:57				
K:58				
K:59				
K:60				
K:61				
K:62				
K:63				
K:64				
K:65	K:73			+5V (Vcc)
K:66				
K:67				
K:68				
K:69				
K:70				
K:71				
K:72				
K:73	K:75	K:65		+5V (Vcc)
K:74				
K:75	K:81	K:73		+5V (Vcc)
K:76				100 KHZ
K:77				
K:78		H:74		SECONDARY RESET
K:79				
K:80		H:72		MASTER RESET
K:81	K:83	K:75		+5V (Vcc)

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
K:82				
K:83		K:81		+5V (Vcc)
K:84				+5V (Vcc)
K:85				GND
K:86				GND
L:1		T:86		GND
L:2				GND
L:3		T:84		+5V (Vcc)
L:4		L:18		+5V (Vcc)
L:5				
L:6				DELAYED 100nSEC STROBE
L:7				
L:8				DELAYED 100nSEC STROBE
L:9				
L:10	L:43			FINE STROBE WIDTH
L:11				
L:12	L:19			COARSE STROBE WIDTH
L:13				
L:14				DELAYED VARIABLE WIDTH STROBE
L:15				7 uSEC
L:16		R:55		DELAY VAR WIDTH STROBE
L:17				6 uSEC
L:18	L:4			10 MHZ
L:19		L:12		5 uSEC
L:20		N:40		5 MHZ
L:21				8 uSEC
L:22				
L:23				9 uSEC
L:24				
L:25				0 uSEC
L:26				
L:27				1 uSEC
L:28				
L:29				2 uSEC
L:30				
L:31				3 uSEC
L:32				
L:33				4 uSEC
L:34				
L:35				500 nSEC
L:36				
L:37				400 nSEC
L:38				
L:39				300 nSEC
L:40				
L:41				600 nSEC
L:42				
L:43		L:10		700 nSEC

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
L:44				PHASE 1-10 MHZ
L:45				800 nSEC
L:46				PHASE 2-10 MHZ
L:47				900 nSEC
L:48				100nSEC LATE STROBE
L:49				000 nSEC
L:50	B:24	P:54		LOCAL/REMOTE
L:51				100 nSEC
L:52	C:68			REMOTE MSD 8 ETA
L:53				200 nSEC
L:54	A:85			LOCAL MSD 8 ETA
L:55				
L:56	A:86			LOCAL MSD 4 ETA
L:57				
L:58	C:70			REMOTE MSD 4 ETA
L:59				
L:60	C:72			REMOTE MSD 2 ETA
L:61				
L:62	A:84			LOCAL MSD 2 ETA
L:63				
L:64	A:82			LOCAL MSD 1 ETA
L:65				
L:66	C:74			REMOTE MSD 1 ETA
L:67				
L:68	C:76			REMOTE LSD 8 ETA
L:69	R:47	L:71		100 KHZ REF #3
L:70	A:80			LOCAL LSD 8 ETA
L:71	L:69	L:73		100 KHZ REF #1
L:72	A:78			LOCAL LSD 4 ETA
L:73	L:71			100 KHZ REF #2
L:74	C:78			REMOTE LSD 4 ETA
L:75				
L:76	C:80			REMOTE LSD 2 ETA
L:77				
L:78	A:76			LOCAL LSD 2 ETA
L:79				
L:80	A:74			LOCAL LSD 1 ETA
L:81				
L:82	C:82			REMOTE LSD 1 ETA
L:83				+5V (Vcc)
L:84				+5V (Vcc)
L:85				GND
L:86				GND
M:1	S:42			GND
M:2				GND
M:3				+5V (Vcc 2)
M:4				+5V (Vcc 2)
M:5	M:19			-15 VDC

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
M:6				
M:7				LOCAL SIGNAL
M:8				5MHZ CLOCK RETURN
M:9	S:43			LOCAL ZERO CROSSING
M:10				C-SSS RESET
M:11	K:40			PHASE CODE
M:12	J:16	P:8		D20, D23 STROBE
M:13		K:42		PHASE CODE
M:14	T:26			STROBE INHIBIT
M:15				DERIVED ENVELOPE
M:16	K:7	P:52		MPT
M:17	R:62			+15 VDC
M:18				
M:19	R:60	M:5		-15 VDC
M:20				
M:21				
M:22				
M:23				
M:24				
M:25				
M:26				
M:27				
M:28				
M:29				
M:30				
M:31				
M:32	J:23	N:82		5 MHZ CLOCK
M:33				
M:34				
M:35				
M:36				
M:37				
M:38				
M:39				
M:40				
M:41				
M:42				
M:43				
M:44				
M:45				
M:46				
M:47				
M:48				
M:49				
M:50				
M:51				
M:52				
M:53				

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
M:54				
M:55				
M:56				
M:57				
M:58				
M:59				
M:60	K:41	P:44		LORTO RESET
M:61				
M:62		N:39		SLEW DIRECTION
M:63				
M:64				SLEW DIRECTION
M:65				
M:66		N:35		SLEW COMMAND
M:67				
M:68	R:65	K:33		SLEW PULSE
M:69				
M:70				
M:71				
M:72				
M:73		M:79		GND
M:74		M:77		GND
M:75		M:81		GND
M:76				
M:77	M:74			GND
M:78				
M:79	M:73			GND
M:80				
M:81	M:75			GND
M:82	M:86			GND
M:83				+5V (Vcc)
M:84				+5V (Vcc)
M:85				GND
M:86		M:82		GND
N:1		N:9		GND
N:2				GND
N:3		N:12		+5V (Vcc)
N:4				+5V (Vcc)
N:5				GATED 100 KHZ
N:6				100 KHZ, 100us STROBE
N:7		T:59		100 KHZ SQUAREWAVE
N:8				100 KHZ, 1us STROBE
N:9	N:1	N:15		100 KHZ GATING
N:10				100 KHZ SQUAREWAVE
N:11		R:25		GATED 1 MHZ
N:12	N:3	N:18		DIVIDER RESET
N:13				GATED 5 MHZ
N:14				BUFFERED 5 MHZ
N:15	N:9			5 MHZ GATING

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
N:16	N:40	T:49		BUFFERED 5 MHZ
N:17	N:18	N:19		1 MHZ GATING
N:18	N:12	N:17		COMPARATOR INHIBIT
N:19	N:17	N:21		P3 DECIMAL COUNTER BCD PARALLEL
N:20				COMPARATOR
N:21	N:19	N:23		P2 DECIMAL COUNTER BCD PARALLEL
N:22				B0 DIGITAL COMPARATOR BCD
N:23	N:21	N:25		P1 DECIMAL COUNTER BCD PARALLEL
N:24				B1 DIGITAL COMPARATOR BCD
N:25	N:23	N:29		P0 DECIMAL COUNTER BCD PARALLEL
N:26				B2 DIGITAL COMPARATOR BCD
N:27				PARALLEL ENTRY SHIFT PULSE
N:28				B3 DIGITAL COMPARATOR BCD
N:29	N:25	N:31		SHIFT PULSE
N:30				Q0 DECIMAL COUNTER BCD
N:31	N:29	N:33		PARALLEL ENTRY COMMAND
N:32				Q1 DECIMAL COUNTER BCD
N:33	N:31	N:37		SHIFT PULSE
N:34				Q2 DECIMAL COUNTER BCD
N:35	M:66			SHIFT PULSE
N:36				Q3 DECIMAL COUNTER BCD
N:37	N:33	N:41		SHIFT DIRECTION COMMAND
N:38				DECIMAL COUNTER TERM COUNT
N:39	M:62			SHIFT DIRECTION COMMAND
N:40	L:20	N:16		0-SHIFTED COUNTER SYNCH.
N:41	N:37			SHIFT DIRECTION COMMAND
N:42				
N:43				
N:44				
N:45				
N:46				
N:47				
N:48				
N:49				
N:50				
N:51				
N:52				
N:53				
N:54				
N:55				
N:56				
N:57				
N:58				
N:59				
N:60				
N:61				
N:62				
N:63				
N:64				

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
N:65				
N:66				
N:67				
N:68				
N:69				
N:70				
N:71				
N:72				
N:73				
N:74				
N:75				
N:76				
N:77	N:85			5 MHZ SINE WAVE
N:78				
N:79				5 MHZ SQUARE WAVE
N:80				PHASE SHIFTED 5 MHZ
N:81				5 MHZ SQUARE WAVE
N:82	M:32			5 MHZ SQUARE WAVE
N:83				+5V (Vcc)
N:84				+5V (Vcc)
N:85		N:77		GND
N:86				GND
P:1				GND
P:2				GND
P:3				+5V (Vcc)
P:4				+5V (Vcc)
P:5				
P:6				
P:7				
P:8	M:12			MAJORITY 100 KHZ
P:9				
P:10				
P:11				TRANSMITT INHIBIT
P:12		P:58		2 HZ
P:13				
P:14				
P:15				
P:16				
P:17				
P:18				10 HZ
P:19				
P:20				
P:21				
P:22	H:9	C:50		BLINK
P:23				
P:24		P:74		BLINK JUMPER
P:25				
P:26		T:40		TRANSMITT INHIBIT

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
P:27				
P:28				
P:29				
P:30				
P:31				
P:32				
P:33				
P:34		H:5		MASTER BLINK CODE
P:35				
P:36		H:7		SECONDARY BLINK CODE
P:37				
P:38				
P:39				
P:40				
P:41				
P:42				
P:43				
P:44	M:60			LORTO
P:45				
P:46		H:11		MASTER
P:47				
P:48		H:13		SECONDARY
P:49				
P:50				
P:51				
P:52	M:16			MPT
P:53				
P:54	L:50			REM/LOC SELECT
P:55				
P:56	H:15			BLINK SET
P:57				
P:58	P:12			2 HZ
P:59				
P:60	J:80	R:50		LAMP TEST
P:61				
P:62		A:54		BLINK LAMP
P:63				
P:64	A:60			LOCAL BLINK Sz
P:65				
P:66	A:50			LOCAL BLINK Sw
P:67				
P:68	C:64			REMOTE BLINK Sw
P:69				
P:70	C:62			REMOTE BLINK Sz
P:71				
P:72	A:56			LOCAL BLINK Sx
P:73				
P:74	P:24			BLINK JUMPER
P:75				

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
P:76	A:58			LOCAL BLINK Sy
P:77				
P:78	C:60			REMOTE BLINK Sy
P:79				
P:80	C:58			REMOTE BLINK Sx
P:81				
P:82				
P:83				+5V (Vcc)
P:84				+5V (Vcc)
P:85				GND
P:86				GND
R:1				GND
R:2				GND
R:3				+5V (Vcc)
R:4				+5V (Vcc)
R:5	S:77			RECORDER 2 +V,-I
R:6				
R:7		S:79		RECORDER 2 +I
R:8				
R:9				REC CHANNEL 1 REF.1
R:10				
R:11				REC CHANNEL 1 REF.2
R:12				
R:13				REC CHANNEL 1 REF.3
R:14				
R:15				
R:16				
R:17				
R:18	E:82	T:39		RECORDER 2 REF #1
R:19				
R:20	F:82	T:41		RECORDER 2 REF #2
R:21				
R:22	G:82	T:43		RECORDER 2 REF #3
R:23				
R:24				
R:25	N:11			RECORDER 2 VARIABLE
R:26				
R:27				REC CHANNEL 1 VARIABLE
R:28				
R:29				
R:30				
R:31				
R:32				UNUSED GATE 2 OUT
R:33				
R:34				UNUSED GATE 2 IN
R:35				REC CHANNEL 1 +V,-I
R:36	T:62	S:73		1 MHZ
R:37		S:75		1 MHZ NEU

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
R:38				UNUSED GATE 1 OUT
R:39				UNUSED GATE 3 IN
R:40				UNUSED GATE 1 IN
R:41				UNUSED GATE 3 IN
R:42				UNUSED GATE 1 IN
R:43				UNUSED GATE 3 OUT
R:44				UNUSED GATE 2 IN
R:45	R:53			DISABLE P C ALARM
R:46		S:19		100 KHZ
R:47	T:47	L:69		100 KHZ SQUAREWAVE
R:48		A:62		LOST XMTR DRIVE LAMP
R:49	K:42			PHASE CODE
R:50	P:60			LAMP TEST
R:51	R:86			100 KHZ GATING INTERVAL
R:52		J:10		LOST XMTR DRIVE
R:53	R:83	R:45		PHASE CODE MODE
R:54				
R:55	L:16			MPT RECLOCK
R:56				
R:57				
R:58		S:61	J2-DD	BLANKING
R:59	T:35			MPT
R:60	S:83	M:19		-15 VDC
R:61				RECLOCKED MPT
R:62	S:81	M:17		+15 VDC
R:63		R:83		MPT INHIBIT
R:64	T:18			EARLY TRIGGER
R:65		M:68		INTERVAL
R:66		S:27		-MPT
R:67				
R:68		S:25		+MPT
R:69				
R:70	S:49	T:8		+24 VDC
R:71				
R:72				+EARLY TRIGGER
R:73				
R:74				-EARLY TRIGGER
R:75				
R:76		S:33		+P.C. RESET TRIG
R:77				
R:78		S:35		-P.C. RESET TRIG
R:79				
R:80		S:29		+P.C. SET TRIG
R:81				
R:82		S:31		-P.C. SET TRIG
R:83	R:63	R:53		+5V (Vcc)
R:84				+5V (Vcc)
R:85				GND
R:86		R:51		GND

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
S:1			J1-E	GND/RECORDER
S:2				GND
S:3		D:25	J1-D	P0 COUNT BCD PARALLEL
S:4				GND
S:5		D:23	J1-B	P1 COUNT BCD PARALLEL
S:6				GND
S:7		D:26	J1-F	B2 DIGITAL COMPARE BCD
S:8				GND
S:9		D:28	J1-H	B3 DIGITAL COMPARE BCD
S:10				GND
S:11	D:30		J1-T	Q0 DECIMAL COUNTER BCD
S:12				GND
S:13	D:32		J1-V	Q1 DECIMAL COUNTER BCD
S:14				GND
S:15	D:34		J1-W	Q2 DECIMAL COUNTER BCD
S:16				GND
S:17	D:36		J1-Y	Q3 DECIMAL COUNTER BCD
S:18				GND
S:19	R:46		J1-J	100 KHZ
S:20				GND
S:21		S:22	J1-L	GND/100 KHZ
S:22	S:21			GND
S:23			J1-N	GND/100 KHZ
S:24				GND
S:25	R:68		J1-S	+XMTR TRIG
S:26				GND
S:27	R:66		J1-P	-XMTR TRIG
S:28				GND
S:29	R:80		J1-X	+P.C. SET
S:30				GND
S:31	R:82		J1-Z	-P.C. SET
S:32				GND
S:33	R:76		J1-e	+P.C. RESET
S:34				GND
S:35	R:78		J1-c	-P.C. RESET
S:36				GND
S:37	T:5		J1-m	+EARLY TRIG
S:38				GND
S:39	T:7		J1-p	-EARLY TRIG
S:40				GND
S:41			J1-s	GND8/EARLY TRIG
S:42		M:1		GND
S:43		M:9	J1-d	RF IN
S:44				GND
S:45	T:50		J1-n	PCI OUT
S:46				GND
S:47			J1-x	GND/5 MHZ SHLD
S:48				GND
S:49	A:81	R:70	J1-K	+24 VDC

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
S:50				GND
S:51			J1-y	GND/RF INPUT
S:52				GND
S:53	J:52		J1-f	MAJ LORTO OUT
S:54				GND
S:55		J:44	J1-j	MAJ LORTO IN
S:56				GND
S:57			J1-U	GND/XMTR TRIG
S:58				GND
S:59	J:12		J1-k	LOSS ALARM DRIVE
S:60				GND
S:61	R:58		J1-r	INTERVAL WAVEFORM
S:62				GND
S:63			J1-b	GND/PC SET
S:64				GND
S:65		D:77	J1-a	5 MHZ INPUT
S:66				GND
S:67		D:85	J1-EE	GND/OPR 1 MHZ
S:68				GND
S:69	A:6	J2-EE	J1-w	OPERATE LAMP
S:70				GND
S:71		A:2	J1-u	STANDBY LAMP
S:72				GND
S:73	R:36		J1-DD	1 MHZ OUT
S:74				GND
S:75	R:37		J1-BB	1 MHZ NEU
S:76				GND
S:77		R:5	J1-A	RECORDER 2 +V,-I
S:78				GND
S:79	R:7		J1-C	RECORDER 2 +I
S:80				GND
S:81		R:62		+15 VDC
S:82				GND
S:83		R:60		-15 VDC
S:84			J1-h	GND
S:85				GND/PC RESET
S:86				GND
T:1	T:21	T:2	J2-B	GND
T:2	T:1			GND
T:3	T:4		J2-i	+5V (Vcc)
T:4	T:52	T:3		+5V (Vcc)
T:5	T:54	S:37		+ET/MPT
T:6				
T:7	T:56	S:39		-ET/MPT
T:8	R:70			+24 VDC
T:9				GND
T:10			J6	BLANKING IN
T:11	T:29			EMPT

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
T:12				
T:13				
T:14				ET-INT-L
T:15				
T:16				AUX-INT-L
T:17				
T:18		R:64		ET ALARM
T:19				
T:20			J2-z	GUARD-H
T:21	T:45	T:1		GND
T:22	K:33			LOCAL INTERVAL
T:23				
T:24				BLANK-L
T:25		T:46		GUARD HI
T:26		M:14		INHIBIT ERR SNS
T:27				
T:28	T:40			BLINK
T:29		T:11		EMPT
T:30				
T:31				MX-INT-L
T:32				
T:33				C-APT-L
T:34				
T:35		R:59		MPT
T:36				
T:37				TEST RESET
T:38	K:5			MPT9
T:39	R:18			1 MHZ
T:40	P:26	T:28		BLINK
T:41	R:20			1 MHZ
T:42				100 KHZ
T:43	R:22			1 MHZ
T:44		T:47		100 KHZ
T:45	T:48	T:21		GND
T:46	T:25	T:67		RESET
T:47	T:44	R:47		100 KHZ
T:48	T:85	T:45		RESET
T:49	N:16	T:58		5 MHZ
T:50		S:45	J2-CC	PCI
T:51				
T:52	T:83	T:4		+5V (Vcc)
T:53				
T:54		T:5		5 MHZ
T:55		K:48		1 MHZ
T:56		T:7		5 MHZ
T:57				
T:58	T:49			5 MHZ
T:59	N:7			100 KHZ SQUAREWAVE
T:60	K:20			PCI

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
T:61			J2-p	S24
T:62		R:36		1 MHZ
T:63			J2-q	S22
T:64				
T:65			J2-x	SHIFT
T:66				
T:67	T:46			STROBE
T:68				
T:69			J2-r	S28
T:70				
T:71			J2-s	RETARD
T:72				
T:73			J2-t	S11
T:74				
T:75			J2-u	S12
T:76				
T:77			J2-v	S18
T:78				
T:79			J2-w	S14
T:80				
T:81				TEST RESET
T:82				
T:83	T:84	T:52		+5V (Vcc)
T:84	L:3	T:83		+5V (Vcc)
T:85	T:86	T:48		GND
T:86	L:1	T:85	J2-A	GND
J1-A		S:77		RECORDER 2 +V,-I
J1-B		S:5		P1 COUNT BCD PARALLEL
J1-C	S:79			RECORDER 2 +I
J1-D		S:3		P0 COUNT BCD PARALLEL
J1-E	S:1			GND/RECORDER
J1-F		S:7		IN A2
J1-G				
J1-H		S:9		IN A3
J1-J	S:19			100 KHZ
J1-K	S:49			+24 VDC
J1-L		S:21		GND/100 KHZ
J1-M				
J1-N		S:23		GND/100 KHZ
J1-P	S:27			-XMTR TRIG
J1-R				
J1-S	S:25			+XMTR TRIG
J1-T	S:11			OUT A0
J1-U		S:57		GND/XMTR TRIG
J1-V	S:13			OUT A1
J1-W	S:15			OUT A2
J1-X	S:29			+P.C. SET
J1-Y	S:17			OUT A3

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
J1-Z	S:31			-P.C. SET
J1-a		S:65		5 MHZ
J1-b		S:63		GND/PC SET
J1-c	S:35			-P.C. RESET
J1-d		S:43		RF IN
J1-e	S:33			+P.C. RESET
J1-f	S:53			MAJ LORTO OUT
J1-g				
J1-h	S:85			GND/PC RESET
J1-i				
J1-j		S:55		MAJ LORTO IN
J1-k	S:59			LOSS ALARM DRIVE
J1-m	S:37			+EARLY TRIG
J1-n	S:45			PCI OUT
J1-p	S:39			-EARLY TRIG
J1-q				
J1-r	S:61			INTERVAL WAVEFORM
J1-s		S:41		GND/EARLY TRIG
J1-t				
J1-u		S:71		STANDBY LAMP
J1-v				
J1-w		S:69		OPERATE LAMP
J1-x		S:47		GND/5 MHZ SHLD
J1-y		S:51		GND/RF INPUT
J1-z				
J1-AA				
J1-BB	S:75			1 MHZ NEU
J1-CC				
J1-DD	S:73			1 MHZ OUT
J1-EE	S:67			GND/OPR 1 MHZ
J1-FF				
J1-GG				
J1-HH				
J2-A	T:86			GND
J2-B	T:1			GND
J2-C				
J2-D				
J2-E				
J2-F				
J2-G				
J2-H				
J2-J				
J2-K				
J2-L				
J2-M				
J2-N				
J2-P				
J2-R				

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
J2-S				
J2-T				
J2-U				
J2-V				
J2-W				
J2-X				
J2-Y				
J2-Z				
J2-a	E:26			1 DRRG INTERVAL
J2-b				
J2-c				
J2-d				
J2-e				
J2-f				
J2-g				
J2-h				
J2-i	T:3			+5V (Vcc)
J2-j				
J2-k				
J2-m				
J2-n				
J2-p		T:61		S2 4
J2-q		T:63		S2 2
J2-r		T:69		S2 8
J2-s		T:71		RETARD
J2-t		T:73		S1 1
J2-u		T:75		S1 2
J2-v		T:77		S1 8
J2-w		T:79		S1 4
J2-x		T:65		SHIFT
J2-y				
J2-z	T:20			GUARD
J2-AA				
J2-BB				
J2-CC	T:50			PCI
J2-DD	R:58			BLANKING
J2-EE		S:69		OPERATE LAMP
J2-FF				
J2-GG				
J2-HH				
J3-A	C:85			GND
J3-B	C:86			GND
J3-C		C:81		CDA 0.02 1
J3-D		C:73		CDA 0.1 1
J3-E		C:71		CDA 0.1 2
J3-F		C:69		CDA 0.1 4
J3-G	C:36			CLEAR
J3-H	C:32			LOAD

Table 5.4. TD-989A/FPN-54A Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
J3-J	C:40			RESET TO EXTERNAL
J3-K		C:58		REMOTE BLINK Sx
J3-L		C:60		REMOTE BLINK Sy
J3-M		C:62		REMOTE BLINK Sz
J3-N		C:70		REMOTE MSD 4 ETA
J3-P		C:72		REMOTE MSD 2 ETA
J3-R		C:74		REMOTE MSD 1 ETA
J3-S		C:82		REMOTE LSD 1 ETA
J3-T	C:42			NO EXT AGMT LAMP
J3-U		C:27		CDA 10K 8
J3-V		C:25		CDA 100K 1
J3-W		C:79		CDA 0.02 2
J3-X		C:77		CDA 0.02 4
J3-Y		C:75		CDA 0.02 8
J3-Z		C:63		CDA 1.0 2
J3-a		C:9		SHIFT RIGHT
J3-b		C:19		CDA 100K 8
J3-c		C:51		CDA 10 8
J3-d		C:49		CDA 100 1
J3-e		C:35		CDA 1K 8
J3-f		C:33		CDA 10K 1
J3-g		C:7		SHIFT LEFT
J3-h		C:64		REMOTE BLINK Sw
J3-i		C:66		LOSS XMTR DRIVE
J3-j		C:68		REMOTE MSD 8 ETA
J3-k		C:76		REMOTE LSD 8 ETA
J3-m		C:78		REMOTE LSD 4 ETA
J3-n		C:80		REMOTE LSD 2 ETA
J3-p	C:17			EXECUTE
J3-q		C:67		CDA 0.1 8
J3-r		C:65		CDA 1.0 1
J3-s		C:61		CDA 1.0 4
J3-t		C:59		CDA 1.0 8
J3-u		C:57		CDA 10 1
J3-v	C:44			CHECK TIMING LAMP
J3-w	C:46			ALARM DRIVER
J3-x		C:48		REM RESET TO EXT
J3-y		C:50		BLINK
J3-z	C:6			CLEAR
J3-AA	C:26			LOCAL/REMOTE
J3-BB		C:43		CDA 100 8
J3-CC		C:41		CDA 1K 1
J3-DD		C:11		EXECUTE
J3-EE				
J3-FF				
J3-GG				
J3-HH				
J6		T:10		BLANKING IN

Table 5.5. TD-1365/FPN-65 Timer Wire List

PIN	FROM	TO	CABLES	WIRE NAME
A:1	B:51			CDA 10 8
A:2	S:71			STANDBY LAMP
A:3		B:53		CDA 10 4
A:4				+24V
A:5		B:55		CDA 10 2
A:6	S:69			OPERATE LAMP
A:7		B:43		CDA 100 8
A:8		B:28		LOC/REM SHIFT
A:9		B:45		CDA 100 4
A:10		B:30		LOC/REM SHIFT
A:11		B:47		CDA 100 2
A:12				+5V (Vcc)
A:13		B:49		CDA 100 1
A:14				GND
A:15		B:35		CDA 1K 8
A:16	C:14			LOC/REM LAMP
A:17		B:37		CDA 1K 4
A:18	B:14			LOC/REM LAMP
A:19		B:39		CDA 1K 2
A:20	J:39			NO EXT AGMT DVR
A:21		B:41		CDA 1K 1
A:22		B:77		CDA 0.02 4
A:23		B:27		CDA 10K 8
A:24		B:79		CDA 0.02 2
A:25		B:29		CDA 10K 4
A:26		B:81		CDA 0.02 1
A:27		B:31		CDA 10K 2
A:28		B:67		CDA 0.1 8
A:29		B:33		CDA 10K 1
A:30		B:69		CDA 0.1 4
A:31		B:19		CDA 100K 8
A:32		B:71		CDA 0.1 2
A:33		B:21		CDA 100K 4
A:34		B:73		CDA 0.1 1
A:35		B:23		CDA 100K 2
A:36		B:59		CDA 1.0 8
A:37		B:25		CDA 100K 1
A:38		B:61		CDA 1.0 4
A:39				GND
A:40		B:63		CDA 1.0 2
A:41		B:9		SHIFT RIGHT
A:42		B:65		CDA 1.0 1
A:43		B:7		SHIFT LEFT
A:44		B:57		CDA 10 1
A:45				+5V (Vcc)
A:46				+24V
A:47				GND
A:48				GND
A:49		B:36		CLEAR

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
A:50		P:66		LOCAL BLINK Sw
A:51	C:12			CLEAR LAMP
A:52				+5V (Vcc)
A:53		B:32		LOAD
A:54	P:62			BLINK LAMP
A:55	C:8			LOAD LAMP
A:56		P:72		LOCAL BLINK Sx
A:57		B:11		EXECUTE
A:58		P:76		LOCAL BLINK Sy
A:59				+24V
A:60		P:64		LOCAL BLINK Sz
A:61	C:10			EXECUTE LAMP
A:62	R:48			LOST XMTR DRIVE LAMP
A:63	J:37			RESET TO EXT DVR
A:64				+24V
A:65		J:35		LOC RESET TO EXT
A:66	C:16	J:80		LAMP TEST
A:67	J:76			DRRG #2 JUMP
A:68				+5V (Vcc)
A:69	J:74			DRRG #3 JUMP
A:70				GND
A:71	J:41			CHECK TIMING DVR
A:72				GND
A:73		J:50		CHECK TIMING RESET
A:74		L:80		LOCAL LSD 1 ETA
A:75				+5V (Vcc)
A:76		L:78		LOCAL LSD 2 ETA
A:77				GND
A:78		L:72		LOCAL LSD 4 ETA
A:79	J:78			DRRG #1 JUMP
A:80		L:70		LOCAL LSD 8 ETA
A:81		S:49		+24 VDC
A:82		L:64		LOCAL MSD 1 ETA
A:83				
A:84		L:62		LOCAL MSD 2 ETA
A:85		L:54		LOCAL MSD 8 ETA
A:86		L:56		LOCAL MSD 4 ETA
B:1				GND
B:2		B:22		GND
B:3		B:13		+5V (Vcc)
B:4				+5V (Vcc)
B:5		D:41		SHIFT DIRECTION
B:6				CLEAR
B:7	A:43			SHIFT LEFT
B:8		C:8		LOAD LAMP
B:9	A:41			SHIFT RIGHT
B:10		C:10		EXECUTE LAMP

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
B:11	A:57			EXECUTE
B:12		C:12		CLEAR LAMP
B:13	B:3			LOC/REM SHIFT INHIBIT
B:14		A:18		LOC/REM LAMP
B:15				LOC/REM SHIFT INHIBIT
B:16		C:16		LAMP TEST
B:17		C:17		EXECUTE
B:18				LOC/REM SECONDARY
B:19	A:31			CDA 100K 8
B:20	C:56			LOC/REM SHIFT
B:21	A:33			CDA 100K 4
B:22	B:2			LOC/REM SECONDARY
B:23	A:35			CDA 100K 2
B:24		L:50		LOCAL/REMOTE
B:25	A:37			DA 100K 1
B:26		C:22		LOCAL/REMOTE
B:27	A:23			CDA 10K 8
B:28	A:8			LOC/REM SHIFT
B:29	A:25			CDA 10K 4
B:30	A:10			LOC/REM SHIFT
B:31	A:27			CDA 10K 2
B:32	A:53			LOAD
B:33	A:29			CDA 10K 1
B:34		D:35		SHIFT PULSE
B:35	A:15			CDA 1K 8
B:36	A:49			CLEAR
B:37	A:17			CDA 1K 4
B:38				LOAD
B:39	A:19			CDA 1K 2
B:40				
B:41	A:21			CDA 1K 1
B:42				
B:43	A:7			CDA 100 8
B:44				
B:45	A:9			CDA 100 4
B:46				
B:47	A:11			CDA 100 2
B:48				
B:49	A:13			CDA 100 1
B:50				
B:51	A:1			CDA 10 8
B:52				
B:53	A:3			CDA 10 4
B:54				
B:55	A:5			CDA 10 2
B:56				
B:57	A:44			CDA 10 1
B:58				
B:59	A:36			CDA 1.0 8

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
B:60				
B:61	A:38			CDA 1.0 4
B:62				
B:63	A:40			CDA 1.0 2
B:64				
B:65	A:42			CDA 1.0 1
B:66				
B:67	A:28			CDA 0.1 8
B:68				
B:69	A:30			CDA 0.1 4
B:70				
B:71	A:32			CDA 0.1 2
B:72				
B:73	A:34			CDA 0.1 1
B:74				
B:75	B:83			CDA 0.02 8
B:76				
B:77	A:22			CDA 0.02 4
B:78				
B:79	A:24			CDA 0.02 2
B:80				
B:81	A:26			CDA 0.02 1
B:82				
B:83		B:75		+5V (Vcc)
B:84				+5V (Vcc)
B:85				GND
B:86				GND
C:1		C:19		GND
C:2				GND
C:3		C:20		+5V (Vcc)
C:4		C:28		+5V (Vcc)
C:5		D:39		SHIFT DIRECTION
C:6			J3-z	CLEAR
C:7			J3-g	SHIFT LEFT
C:8	B:8	A:55		LOAD LAMP
C:9			J3-a	SHIFT RIGHT
C:10	B:10	A:61		EXECUTE LAMP
C:11			J3-DD	EXECUTE
C:12	B:12	A:51		CLEAR LAMP
C:13				LOC/REM SHIFT INHIBIT
C:14		A:16		LOC/REM LAMP
C:15				LOC/REM SHIFT INHIBIT
C:16	B:16	A:66		LAMP TEST
C:17	B:17	R:63	J3-p	EXECUTE
C:18	C:22			LOC/REM SECONDARY
C:19	C:1	C:25	J3-b	CDA 100K 8
C:20	C:3	C:21		LOC/REM SHIFT

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
C:21	C:20	C:23		CDA 100K 4
C:22	B:26	C:18		LOC/REM SECONDARY
C:23	C:21	C:29		CDA 100K 2
C:24				LOCAL/REMOTE
C:25	C:19	C:27	J3-V	CDA 100K 1
C:26			J3-AA	LOCAL/REMOTE
C:27	C:25	C:33	J3-U	CDA 10K 8
C:28	C:4	C:30		LOC/REM SHIFT
C:29	C:23	C:31		CDA 10K 4
C:30	C:28			LOC/REM SHIFT
C:31	C:29	C:37		CDA 10K 2
C:32			J3-H	LOAD
C:33	C:27	C:35	J3-f	CDA 10K 1
C:34		D:33		SHIFT PULSE
C:35	C:33	C:41	J3-e	CDA 1K 8
C:36			J3-G	CLEAR
C:37	C:31	C:39		CDA 1K 4
C:38				LOAD LOGIC
C:39	C:37	C:45		CDA 1K 2
C:40	J:5		J3-J	RESET TO EXTERNAL
C:41	C:35	C:43	J3-CC	CDA 1K 1
C:42	J:11		J3-T	NO EXT AGMT LAMP
C:43	C:41	C:49	J3-BB	CDA 100 8
C:44	J:9		J3-v	CHECK TIMING LAMP
C:45	C:39	C:47		CDA 100 4
C:46	J:7		J3-w	ALARM DRIVER
C:47	C:45	C:53		CDA 100 2
C:48		J:32	J3-x	REM RESET TO EXT
C:49	C:43	C:51	J3-d	CDA 100 1
C:50	P:22		J3-y	BLINK
C:51	C:49	C:57	J3-c	CDA 10 8
C:52				
C:53	C:47	C:55		CDA 10 4
C:54				
C:55	C:53	C:56		CDA 10 2
C:56	C:55	B:20		LOC/REM SHIFT
C:57	C:51		J3-u	CDA 10 1
C:58		P:80	J3-K	REMOTE BLINK Sx
C:59			J3-t	CDA 1.0 8
C:60		P:78	J3-L	REMOTE BLINK Sy
C:61			J3-s	CDA 1.0 4
C:62		P:70	J3-M	REMOTE BLINK Sz
C:63			J3-Z	CDA 1.0 2
C:64		P:68	J3-h	REMOTE BLINK Sw
C:65			J3-r	CDA 1.0 1
C:66	J:10		J3-i	LOSS XMTR DRIVE
C:67			J3-q	CDA 0.1 8
C:68		L:52	J3-j	REMOTE MSD 8 ETA
C:69			J3-F	CDA 0.1 4

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
C:70		L:58	J3-N	REMOTE MSD 4 ETA
C:71			J3-E	CDA 0.1 2
C:72		L:60	J3-P	REMOTE MSD 2 ETA
C:73			J3-D	CDA 0.1 1
C:74		L:66	J3-R	REMOTE MSD 1 ETA
C:75	C:83		J3-Y	CDA 0.02 8
C:76		L:68	J3-$\underline{k}$	REMOTE LSD 8 ETA
C:77			J3-$\overline{X}$	CDA 0.02 4
C:78		L:74	J3-$\underline{m}$	REMOTE LSD 4 ETA
C:79			J3-$\overline{W}$	CDA 0.02 2
C:80		L:76	J3-$\underline{n}$	REMOTE LSD 2 ETA
C:81			J3-$\overline{C}$	CDA 0.02 1
C:82		L:82	J3-S	REMOTE LSD 1 ETA
C:83		C:75		+5V (Vcc)
C:84				+5V (Vcc)
C:85			J3-A	GND
C:86			J3-B	GND
D:1		D:9	GND	
D:2				GND
D:3				+5V (Vcc)
D:4		D:12		+5V (Vcc)
D:5				GATED 100 KHZ
D:6				100 KHZ, 100us STROBE
D:7				100 KHZ SQUAREWAVE
D:8				100 KHZ, 1us STROBE
D:9	D:1	D:15		100 KHZ GATING
D:10				100 KHZ SQUAREWAVE
D:11				GATED 1 MHZ
D:12	D:4	D:18		DIVIDER RESET
D:13				GATED 5 MHZ
D:14				BUFFERED 5 MHZ
D:15	D:9	D:17		5 MHZ GATING
D:16		D:40		BUFFERED 5 MHZ
D:17	D:15			1 MHZ GATING
D:18	D:12	D:37		COMPARATOR INHIBIT
D:19	D:28			P3 DECIMAL COUNTER BCD PARALLEL
D:20		J:33		EXT PHASE SHIFT AGREE
D:21	D:26			P2 DECIMAL COUNTER BCD PARALLEL
D:22	D:25			B0 DIGITAL COMPARE BCD
D:23	S:5	D:24		P1 COUNT BCD PARALLEL
D:24	D:23			B1 DIGITAL COMPARE BCD
D:25	S:3	D:22		P0 COUNT BCD PARALLEL
D:26	S:7	D:21		B2 DIGITAL COMPARE BCD
D:27				PARALLEL ENTRY SHIFT PULSE
D:28	S:9	D:19		B3 DIGITAL COMPARATOR BCD
D:29	J:15			SHIFT PULSE
D:30		S:11		Q0 DECIMAL COUNTER BCD
D:31	J:27			PARALLEL ENTRY COMMAND

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
D:32		S:13		Q1 DECIMAL COUNTER BCD
D:33	C:34			SHIFT PULSE
D:34		S:15		Q2 DECIMAL COUNTER BCD
D:35	B:34			SHIFT PULSE
D:36		S:17		Q3 DECIMAL COUNTER BCD
D:37	D:18			SHIFT DIRECTION COMMAND
D:38				DECIMAL COUNTER TERM COUNT
D:39	C:5			SHIFT DIRECTION
D:40	D:16	E:74		0-SHIFTED COUNTER SYNCH.
D:41	B:5			SHIFT DIRECTION
D:42				
D:43				
D:44				
D:45				
D:46				
D:47				
D:48				
D:49				
D:50				
D:51				
D:52				
D:53				
D:54				
D:55				
D:56				
D:57				
D:58				
D:59				
D:60				
D:61				
D:62				
D:63				
D:64				
D:65				
D:66				
D:67				
D:68				
D:69				
D:70				
D:71				
D:72				
D:73				
D:74				
D:75				
D:76				
D:77	S:65			5 MHZ SINE WAVE
D:78				
D:79				5 MHZ SQUARE WAVE
D:80				PHASE SHIFTED 5 MHZ

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
D:81		D:82		5 MHZ SQUARE WAVE
D:82	D:81			5 MHZ SQUARE WAVE
D:83				+5V (Vcc)
D:84				+5V (Vcc)
D:85	S:67			GND
D:86				GND
E:1				GND
E:2		E:38		GND
E:3				+5V (Vcc)
E:4				+5V (Vcc)
E:5		H:57		1 D64
E:6				1 LFF2 RESET
E:7		H:59		1 D63
E:8	E:71			1 LFF3 RESET
E:9				1 D62
E:10	E:75			1 LFF3 SET
E:11		H:47		1 D69
E:12		J:21		1 LFF3
E:13		H:49		1 D68
E:14				1 LFF2 SET
E:15		H:51		1 D67
E:16				1 LFF2
E:17		H:53		1 D66
E:18		E:26		1 DRRG 0
E:19		H:55		1 D65
E:20		J:56		1,3 DRRG LOSS
E:21				1 D61
E:22		J:64		1,3 INTERVAL LORTO
E:23				1 D51
E:24		F:80		1 LORTO
E:25				1 D52
E:26	E:18	F:78	J2-a	1 DRRG INTERVAL
E:27				1 D54
E:28		H:63		1 D59
E:29				1 D53
E:30				1 D58
E:31				1 D55
E:32				1 D57
E:33		H:61		1 D50
E:34				1 D56
E:35		H:79		1 D43
E:36	E:60			1 RESET
E:37		H:77		1 D44
E:38	E:2			1 R0 RATE SET
E:39		H:81		1 D42
E:40	H:41			1 R1 RATE SET
E:41				1 D41
E:42	H:43			1 R2 RATE SET

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
E:43		H:65		1 D40
E:44		H:67		1 D49
E:45				1 D30
E:46		H:69		1 D48
E:47				1 D32
E:48		H:71		1 D47
E:49				1 D33
E:50		H:73		1 D46
E:51				1 D34
E:52		H:75		1 D45
E:53				1 D31
E:54	H:45			1 R3 RATE SET
E:55				1 D39
E:56	H:39			1 T1 TRIGGER SET
E:57				1 D38
E:58				
E:59				1 D37
E:60	J:79	E:36		1 EXTERNAL RESET
E:61				1 D36
E:62				DIVIDER CONTROL
E:63				1 D35
E:64	E:70			COUNT SET
E:65				1 D21
E:66	E:84			1 D2 PRESET
E:67				1 D22
E:68				1 D24
E:69				1 D23
E:70		E:64		1 D14
E:71		E:8		1 D29
E:72				1 D10
E:73				1 D27
E:74	D:40	F:74		5 MHZ CLOCK
E:75		E:10		1 D26
E:76				1 D60
E:77				1 D25
E:78	G:26	K:13		CHECK INTERVAL
E:79				1 D28
E:80	G:24	J:68		CHECK LORTO
E:81				1 D20
E:82		R:18		COUNT ENABLE
E:83				+5V (Vcc)
E:84		E:66		+5V (Vcc)
E:85				GND
E:86				GND
F:1				GND
F:2		F:38		GND
F:3				+5V (Vcc)

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
F:4				+5V (Vcc)
F:5		H:68		2 D64
F:6				2 LFF2 RESET
F:7		H:70		2 D63
F:8	F:71			2 LFF3 RESET
F:9				2 D62
F:10	F:75			2 LFF3 SET
F:11		H:58		2 D69
F:12		J:19		2 LFF3
F:13		H:60		2 D68
F:14				2 LFF2 SET
F:15		H:62		2 D67
F:16				2 LFF2
F:17		H:64		2 D66
F:18		F:26		2 DRRG 0
F:19		H:66		2 D65
F:20		J:54		1,2 DRRG LOSS
F:21				2 D61
F:22		J:66		1,2 INTERVAL LORTO
F:23				2 D51
F:24		G:80		2 LORTO
F:25				2 D52
F:26	F:18	G:78		2 DRRG INTERVAL
F:27				2 D54
F:28		H:56		2 D59
F:29				2 D53
F:30				2 D58
F:31				2 D55
F:32				2 D57
F:33		H:54		2 D50
F:34				2 D56
F:35		H:19		2 D43
F:36	F:60			2 RESET
F:37		H:21		2 D44
F:38	F:2			2 R0 RATE SET
F:39		H:17		2 D42
F:40	H:37			2 R1 RATE SET
F:41				2 D41
F:42	H:52			2 R2 RATE SET
F:43		H:33		2 D40
F:44		H:31		2 D49
F:45				2 D30
F:46		H:29		2 D48
F:47				2 D32
F:48		H:27		2 D47
F:49				2 D33
F:50		H:25		2 D46
F:51				2 D34
F:52		H:23		2 D45

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
F:53				2 D31
F:54	H:50			2 R3 RATE SET
F:55				2 D39
F:56	H:35			2 T1 TRIGGER SET
F:57				2 D38
F:58				
F:59				2 D37
F:60	J:77	F:36		2 EXTERNAL RESET
F:61				2 D36
F:62				DIVIDER CONTROL
F:63				2 D35
F:64	F:70			COUNT SET
F:65				2 D21
F:66	F:84			2 D2 PRESET
F:67				2 D22
F:68				2 D24
F:69				2 D23
F:70		F:64		2 D14
F:71		F:8		2 D29
F:72				2 D10
F:73				2 D27
F:74	E:74	G:74		5 MHZ CLOCK
F:75		F:10		2 D26
F:76				2 D60
F:77				2 D25
F:78	E:26	K:9		CHECK INTERVAL
F:79				2 D28
F:80	E:24	J:73		CHECK LORTO
F:81				2 D20
F:82		R:20		COUNT ENABLE
F:83				+5V (Vcc)
F:84		F:66		+5V (Vcc)
F:85				GND
F:86				GND
G:1				GND
G:2		G:38		GND
G:3				+5V (Vcc)
G:4				+5V (Vcc)
G:5		H:30		3 D64
G:6				3 LFF2 RESET
G:7		H:28		3 D63
G:8	G:71			3 LFF3 RESET
G:9				3 D62
G:10	G:75			3 LFF3 SET
G:11		H:40		3 D69
G:12		J:17		3 LFF3
G:13		H:38		3 D68
G:14				3 LFF2 SET

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
G:15		H:36		3 D67
G:16				3 LFF2
G:17		H:34		3 D66
G:18		G:26		3 DRRG 0
G:19		H:32		3 D65
G:20		J:58		2,3 DRRG LOSS
G:21				3 D61
G:22		J:62		2,3 INTERVAL LORTO
G:23				3 D51
G:24		E:80		3 LORTO
G:25				3 D52
G:26	G:18	E:78		3 DRRG INTERVAL
G:27				3 D54
G:28		H:24		3 D59
G:29				3 D53
G:30				3 D58
G:31				3 D55
G:32				3 D57
G:33		H:26		3 D50
G:34				3 D56
G:35		H:8		3 D43
G:36	G:60			3 RESET
G:37		H:10		3 D44
G:38	G:2			3 R0 RATE SET
G:39		H:6		3 D42
G:40	H:46			3 R1 RATE SET
G:41				3 D41
G:42	H:44			3 R2 RATE SET
G:43		H:22		3 D40
G:44		H:20		3 D49
G:45				3 D30
G:46		H:18		3 D48
G:47				3 D32
G:48		H:16		3 D47
G:49				3 D33
G:50		H:14		3 D46
G:51				3 D34
G:52		H:12		3 D45
G:53				3 D31
G:54	H:42			3 R3 RATE SET
G:55				3 D39
G:56	H:48			3 T1 TRIGGER SET
G:57				3 D38
G:58				
G:59				3 D37
G:60	J:75	G:36		3 EXTERNAL RESET
G:61				3 D36
G:62				DIVIDER CONTROL
G:63				3 D35

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
G:64	G:70			COUNT SET
G:65				3 D21
G:66	G:84			3 D2 PRESET
G:67				3 D22
G:68				3 D24
G:69				3 D23
G:70		G:64		3 D14
G:71		G:8		3 D29
G:72				3 D10
G:73				3 D27
G:74	F:74	J:23		5 MHZ CLOCK
G:75		G:10		3 D26
G:76				3 D60
G:77				3 D25
G:78	F:26	K:11		CHECK INTERVAL
G:79				3 D28
G:80	F:24	J:71		CHECK LORTO
G:81				3 D20
G:82		R:22		COUNT ENABLE
G:83				+5V (Vcc)
G:84		G:66		+5V (Vcc)
G:85				GND
G:86				GND
H:1				GND
H:2				GND
H:3				+5V (Vcc)
H:4				+5V (Vcc)
H:5	P:34			MASTER BLINK CODE
H:6	G:39			3 D42 (200)
H:7	P:36			SECONDARY BLINK CODE
H:8	G:35			3 D43 (300)
H:9		P:22		BLINK
H:10	G:37			3 D44 (400)
H:11	P:46			MASTER
H:12	G:52	K:15		3 D45 (500)
H:13	P:48			SECONDARY
H:14	G:50			3 D46 (600)
H:15		P:56		BLINK SET
H:16	G:48			3 D47 (700)
H:17	F:39			2 D42 (200)
H:18	G:46			3 D48 (800)
H:19	F:35			2 D43 (300)
H:20	G44	K:23		3 D49 (900)
H:21	F:37			2 D44 (400)
H:22	G:43			3 D40 (000)
H:23	F:52	K:16		2 D45 (500)
H:24	G:28			3 D59 (9K)

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
H:25	F:50			2 D46 (600)
H:26	G:33			3 D50 (0000)
H:27	F:48			2 D47 (700)
H:28	G:7			3 D63 (30K)
H:29	F:46			2 D48 (800)
H:30	G:5			3 D64 (40K)
H:31	F:44	K:27		2 D49 (900)
H:32	G:19			3 D65 (50K)
H:33	F:43			2 D40 (000)
H:34		G:17		3 D66 (60K)
H:35		F:56		2 T1 SCOPE TRIGGER
H:36	G:15			3 D67 (70K)
H:37		F:40		2 R1 RATE SET (GRI-100)
H:38	G:13			3 D68 (80K)
H:39		E:56		1 T1 SCOPE TRIGGER
H:40	G:11			3 D69 (90K)
H:41		E:40		1 R1 RATE SET (GRI-100)
H:42		G:54		3 R3 RATE SET (GRI-10K)
H:43		E:42		1 R2 RATE SET (GRI-1K)
H:44		G:42		3 R2 RATE SET (GRI-1K)
H:45		E:54		1 R3 RATE SET (GRI-10K)
H:46		G:40		3 R1 RATE SET (GRI-100)
H:47	E:11			1 D69 (90K)
H:48		G:56		3 T1 SCOPE TRIGGER
H:49	E:13			1 D68 (80K)
H:50		F:54		2 R3 RATE SET (GRI-10K)
H:51	E:15			1 D67 (70K)
H:52		F:42		2 R2 RATE SET (GRI-1K)
H:53	E:17			1 D66 (60K)
H:54	F:33			2 D50 (0000)
H:55	E:19			1 D65 (50K)
H:56	F:28			2 D59 (9K)
H:57	E:5			1 D64 (40K)
H:58	F:11			2 D69 (90K)
H:59	E:7			1 D63 (30K)
H:60	F:13			2 D68 (80K)
H:61	E:33			1 D50 (0000)
H:62	F:15			2 D67 (70K)
H:63	E:28			1 D59 (9K)
H:64	F:17			2 D66 (60K)
H:65	E:43			1 D40 (000)
H:66	F:19			2 D65 (50K)
H:67	E:44	K:19		1 D49 (900)
H:68	F:5			2 D64 (40K)
H:69	E:46			1 D48 (800)
H:70	F:7			2 D63 (30K)
H:71	E:48			1 D47 (700)
H:72	K:80			MASTER RESET
H:73	E:50			1 D46 (600)

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
H:74	K:78			SECONDARY RESET
H:75	E:52	K:12		1 D45 (500)
H:76		K:31		LOCAL INTERVAL RESET
H:77	E:37			1 D44 (400)
H:78		K:10		P.C. CONTROL
H:79	E:35			1 D43 (300)
H:80				
H:81	E:39			1 D42 (200)
H:82				
H:83				+5V (Vcc)
H:84				+5V (Vcc)
H:85				GND
H:86				GND
J:1				GND
J:2				GND
J:3				+5V (Vcc)
J:4				+5V (Vcc)
J:5		C:40		RESET TO EXTERNAL
J:6				
J:7		C:46		ALARM DRIVER
J:8	J:40			NO EXT. ALARM
J:9		C:44		CHECK TIMING LAMP
J:10	R:52	C:66		LOST XMTR DRIVE
J:11		C:42		NO EXT AGMT LAMP
J:12		S:59		LOSS ALARM DRIVER
J:13				
J:14				
J:15		D:29		SHIFT PULSE
J:16		M:12		MAJORITY
J:17	G:12			SOURCE 3
J:18				CP
J:19	F:12			SOURCE 2
J:20				
J:21	E:12			SOURCE 1
J:22				
J:23	G:74	M:32		5 MHZ CLOCK
J:24				
J:25				
J:26				
J:27		D:31		0-SHIFT RESET TO EXTERNAL
J:28	J:30			CLOCK ENABLE
J:29				
J:30		J:28		0-SHIFT CLOCK SET
J:31				
J:32	C:48			REM RESET TO EXT
J:33	D:20			EXT PHASE SHIFT AGREE
J:34				

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
J:35	A:65			LOC RESET TO EXT
J:36				
J:37		A:63		RESET TO EXT DVR
J:38				
J:39		A:20		NO EXT AGMT DVR
J:40		J:8		NO EXT. ALARM
J:41		A:71		CHECK TIMING DVR
J:42				
J:43		K:41		LOST MAJORITY
J:44	S:55			EXT MAJ INT LORTO
J:45				MAJORITY LORTO
J:46				
J:47				MAJORITY INTERVAL LORTO
J:48				LOST MAJORITY
J:49				
J:50	A:73			CHECK TIMING RESET
J:51				
J:52		S:53		MAJ INT LORTO
J:53				
J:54	F:20			1,2 DRRG LOSS
J:55				
J:56	E:20			1,3 DRRG LOSS
J:57				
J:58	G:20			2,3 DRRG LOSS
J:59				
J:60				
J:61				
J:62	G:22			2,3 INTERVAL LORTO
J:63				
J:64	E:22			1,3 INTERVAL LORTO
J:65				
J:66	F:22			1,2 INTERVAL LORTO
J:67				
J:68	E:80			LORTO DRRG #3
J:69				
J:70		J:72		NO MAJORITY RESET
J:71	G:80			LORTO DRRG #2
J:72	J:70			NO MAJORITY RESET
J:73	F:80			LORTO DRRG #1
J:74		A:69		DRRG #3 JUMP
J:75		G:60		DRRG #3 RESET
J:76		A:67		DRRG #2 JUMP
J:77		F:60		DRRG #2 RESET
J:78		A:79		DRRG #1 JUMP
J:79		E:60		DRRG #1 RESET
J:80	A:66	P:60		LAMP TEST
J:81				
J:82				
J:83				+5V (Vcc)

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
J:84				+5V (Vcc)
J:85				GND
J:86				GND
K:1				GND
K:2				GND
K:3				+5V (Vcc)
K:4				+5V (Vcc)
K:5		T:38		PMPT 9
K:6	G:52	K:15		05-L1
K:7		M:16		PMPT 8
K:8	K:12			05-L2
K:9	F:78			PCI-L1 DRRG #1
K:10	H:78			MAS/SEC SELECT
K:11	G:78			PCI-L2 DRRG #2
K:12	H:75	K:8		05-L2
K:13	E:78			PCI-L3 DRRG #3
K:14	F:52	K:16		05-L3
K:15	H:12	K:6		05-L1
K:16	H:23	K:14		05-L3
K:17	K:19			09-L2
K:18				
K:19	H:67	K:17		09-L2
K:20		T:60		PHASE CODE INTERVAL
K:21	K:23			09-L1
K:22				
K:23	H:20	K:21		09-L1
K:24				
K:25	K:27			09-L3
K:26				
K:27	H:31	K:25		09-L3
K:28				
K:29				
K:30				
K:31	H:76			LOCAL INTERVAL RESET
K:32				
K:33	M:68	T:22		LOCAL INTERVAL
K:34				
K:35				
K:36				
K:37				LOCAL INTERVAL
K:38				
K:39				
K:40		M:11		PHASE CODE
K:41	J:43	M:60		LORTO
K:42	M:13	R:49		PHASE CODE
K:43				
K:44				TUBE/SSX SELECT
K:45				

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
K:46				
K:47				
K:48	T:55			1 MHZ
K:49				100 KHZ DELAYED
K:50				
K:51				
K:52				
K:53				EXT. OSC.
K:54				
K:55				OSC. DISABLE
K:56				
K:57				
K:58				
K:59				
K:60				
K:61				
K:62				
K:63				
K:64				
K:65	K:73			+5V (Vcc)
K:66				
K:67				
K:68				
K:69				
K:70				
K:71				
K:72				
K:73	K:75	K:65		+5V (Vcc)
K:74				
K:75	K:81	K:73		+5V (Vcc)
K:76				100 KHZ
K:77				
K:78		H:74		SECONDARY RESET
K:79				
K:80		H:72		MASTER RESET
K:81	K:83	K:75		+5V (Vcc)
K:82				
K:83		K:81		+5V (Vcc)
K:84				+5V (Vcc)
K:85				GND
K:86				GND
L:1		T:86		GND
L:2				GND
L:3		T:84		+5V (Vcc)
L:4		L:18		+5V (Vcc)
L:5				
L:6				DELAYED 100nSEC STROBE

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
L:7				
L:8				DELAYED 100nSEC STROBE
L:9				
L:10	L:43			FINE STROBE WIDTH
L:11				
L:12	L:19			COARSE STROBE WIDTH
L:13				
L:14				DELAYED VARIABLE WIDTH STROBE
L:15				7 uSEC
L:16		R:55		DELAY VAR WIDTH STROBE
L:17				6 uSEC
L:18	L:4			10 MHZ
L:19		L:12		5 uSEC
L:20		N:40		5 MHZ
L:21				8 uSEC
L:22				
L:23				9 uSEC
L:24				
L:25				0 uSEC
L:26				
L:27				1 uSEC
L:28				
L:29				2 uSEC
L:30				
L:31				3 uSEC
L:32				
L:33				4 uSEC
L:34				
L:35				500 nSEC
L:36				
L:37				400 nSEC
L:38				
L:39				300 nSEC
L:40				
L:41				600 nSEC
L:42				
L:43		L:10		700 nSEC
L:44				PHASE 1-10 MHZ
L:45				800 nSEC
L:46				PHASE 2-10 MHZ
L:47				900 nSEC
L:48				100nSEC LATE STROBE
L:49				000 nSEC
L:50	B:24	P:54		LOCAL/REMOTE
L:51				100 nSEC
L:52	C:68			REMOTE MSD 8 ETA
L:53				200 nSEC
L:54	A:85			LOCAL MSD 8 ETA

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
L:55				
L:56	A:86			LOCAL MSD 4 ETA
L:57				
L:58	C:70			REMOTE MSD 4 ETA
L:59				
L:60	C:72			REMOTE MSD 2 ETA
L:61				
L:62	A:84			LOCAL MSD 2 ETA
L:63				
L:64	A:82			LOCAL MSD 1 ETA
L:65				
L:66	C:74			REMOTE MSD 1 ETA
L:67				
L:68	C:76			REMOTE LSD 8 ETA
L:69	R:47	L:71		100 KHZ REF #3
L:70	A:80			LOCAL LSD 8 ETA
L:71	L:69	L:73		100 KHZ REF #1
L:72	A:78			LOCAL LSD 4 ETA
L:73	L:71			100 KHZ REF #2
L:74	C:78			REMOTE LSD 4 ETA
L:75				
L:76	C:80			REMOTE LSD 2 ETA
L:77				
L:78	A:76			LOCAL LSD 2 ETA
L:79				
L:80	A:74			LOCAL LSD 1 ETA
L:81				
L:82	C:82			REMOTE LSD 1 ETA
L:83				+5V (Vcc)
L:84				+5V (Vcc)
L:85				GND
L:86				GND
M:1	S:42			GND
M:2				GND
M:3				+5V (Vcc 2)
M:4				+5V (Vcc 2)
M:5	M:19			-15 VDC
M:6				
M:7				LOCAL SIGNAL
M:8				5MHZ CLOCK RETURN
M:9	S:43			LOCAL ZERO CROSSING
M:10				C-SSS RESET
M:11	K:40			PHASE CODE
M:12	J:16	P:8		D20, D23 STROBE
M:13		K:42		PHASE CODE
M:14	T:26			STROBE INHIBIT
M:15				DERIVED ENVELOPE
M:16	K:7	P:52		MPT

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
M:17	R:62			+15 VDC
M:18				
M:19	R:60	M:5		-15 VDC
M:20				
M:21				
M:22				
M:23				
M:24				
M:25				
M:26				
M:27				
M:28				
M:29				
M:30				
M:31				
M:32	J:23	N:82		5 MHZ CLOCK
M:33				
M:34				
M:35				
M:36				
M:37				
M:38				
M:39				
M:40				
M:41				
M:42				
M:43				
M:44				
M:45				
M:46				
M:47				
M:48				
M:49				
M:50				
M:51				
M:52				
M:53				
M:54				
M:55				
M:56				
M:57				
M:58				
M:59				
M:60	K:41	P:44		LORTO RESET
M:61				
M:62		N:39		SLEW DIRECTION
M:63				
M:64				SLEW DIRECTION
M:65				

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
M:66		N:35		SLEW COMMAND
M:67				
M:68	R:65	K:33		SLEW PULSE
M:69				
M:70				
M:71				
M:72				
M:73		M:79		GND
M:74		M:77		GND
M:75		M:81		GND
M:76				
M:77	M:74			GND
M:78				
M:79	M:73			GND
M:80				
M:81	M:75			GND
M:82	M:86			GND
M:83				+5V (Vcc)
M:84				+5V (Vcc)
M:85				GND
M:86		M:82		GND
N:1		N:9		GND
N:2				GND
N:3		N:12		+5V (Vcc)
N:4				+5V (Vcc)
N:5				GATED 100 KHZ
N:6				100 KHZ, 100us STROBE
N:7		T:59		100 KHZ SQUAREWAVE
N:8				100 KHZ, 1us STROBE
N:9	N:1	N:15		100 KHZ GATING
N:10				100 KHZ SQUAREWAVE
N:11		R:25		GATED 1 MHZ
N:12	N:3	N:18		DIVIDER RESET
N:13				GATED 5 MHZ
N:14				BUFFERED 5 MHZ
N:15	N:9			5 MHZ GATING
N:16	N:40	T:49		BUFFERED 5 MHZ
N:17	N:18	N:19		1 MHZ GATING
N:18	N:12	N:17		COMPARATOR INHIBIT
N:19	N:17	N:21		P3 DECIMAL COUNTER BCD PARALLEL
N:20				COMPARATOR
N:21	N:19	N:23		P2 DECIMAL COUNTER BCD PARALLEL
N:22				B0 DIGITAL COMPARATOR BCD
N:23	N:21	N:25		P1 DECIMAL COUNTER BCD PARALLEL
N:24				B1 DIGITAL COMPARATOR BCD
N:25	N:23	N:29		P0 DECIMAL COUNTER BCD PARALLEL
N:26				B2 DIGITAL COMPARATOR BCD
N:27				PARALLEL ENTRY SHIFT PULSE

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
N:28				B3 DIGITAL COMPARATOR BCD
N:29	N:25	N:31		SHIFT PULSE
N:30				Q0 DECIMAL COUNTER BCD
N:31	N:31	N:33		PARALLEL ENTRY COMMAND
N:32				Q1 DECIMAL COUNTER BCD
N:33	N:33	N:37		SHIFT PULSE
N:34				Q2 DECIMAL COUNTER BCD
N:35	M:66			SHIFT PULSE
N:36				Q3 DECIMAL COUNTER BCD
N:37	N:33	N:41		SHIFT DIRECTION COMMAND
N:38				DECIMAL COUNTER TERM COUNT
N:39	M:62			SHIFT DIRECTION COMMAND
N:40	L:20	N:16		0-SHIFTED COUNTER SYNCH.
N:41	N:37			SHIFT DIRECTION COMMAND
N:42				
N:43				
N:44				
N:45				
N:46				
N:47				
N:48				
N:49				
N:50				
N:51				
N:52				
N:53				
N:54				
N:55				
N:56				
N:57				
N:58				
N:59				
N:60				
N:61				
N:62				
N:63				
N:64				
N:65				
N:66				
N:67				
N:68				
N:69				
N:70				
N:71				
N:72				
N:73				
N:74				
N:75				

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
N:76				
N:77	N:85			5 MHZ SINE WAVE
N:78				
N:79				5 MHZ SQUARE WAVE
N:80				PHASE SHIFTED 5 MHZ
N:81				5 MHZ SQUARE WAVE
N:82	M:32			5 MHZ SQUARE WAVE
N:83				+5V (Vcc)
N:84				+5V (Vcc)
N:85		N:77		GND
N:86				GND
P:1				GND
P:2				GND
P:3				+5V (Vcc)
P:4				+5V (Vcc)
P:5				
P:6				
P:7				
P:8	M:12			MAJORITY 100 KHZ
P:9				
P:10				
P:11				TRANSMITT INHIBIT
P:12		P:58		2 HZ
P:13				
P:14				
P:15				
P:16				
P:17				
P:18				10 HZ
P:19				
P:20				
P:21				
P:22	H:9	C:50		BLINK
P:23				
P:24		P:74		BLINK JUMPER
P:25				
P:26		T:40		TRANSMITT INHIBIT
P:27				
P:28				
P:29				
P:30				
P:31				
P:32				
P:33				
P:34		H:5		MASTER BLINK CODE
P:35				
P:36		H:7		SECONDARY BLINK CODE
P:37				

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
P:38				
P:39				
P:40				
P:41				
P:42				
P:43				
P:44	M:60			LORTO
P:45				
P:46		H:11		MASTER
P:47				
P:48		H:13		SECONDARY
P:49				
P:50				
P:51				
P:52	M:16			MPT
P:53				
P:54	L:50			REM/LOC SELECT
P:55				
P:56	H:15			BLINK SET
P:57				
P:58	P:12			2 HZ
P:59				
P:60	J:80	R:50		LAMP TEST
P:61				
P:62		A:54		BLINK LAMP
P:63				
P:64	A:60			LOCAL BLINK Sz
P:65				
P:66	A:50			LOCAL BLINK Sw
P:67				
P:68	C:64			REMOTE BLINK Sw
P:69				
P:70	C:62			REMOTE BLINK Sz
P:71				
P:72	A:56			LOCAL BLINK Sx
P:73				
P:74	P:24			BLINK JUMPER
P:75				
P:76	A:58			LOCAL BLINK Sy
P:77				
P:78	C:60			REMOTE BLINK Sy
P:79				
P:80	C:58			REMOTE BLINK Sx
P:81				
P:82				
P:83				+5V (Vcc)
P:84				+5V (Vcc)
P:85				GND
P:86				GND

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
R:1				GND
R:2				GND
R:3				+5V (Vcc)
R:4				+5V (Vcc)
R:5	S:77			RECORDER 2 +V,-I
R:6				
R:7		S:79		RECORDER 2 +I
R:8				
R:9				REC CHANNEL 1 REF.1
R:10				
R:11				REC CHANNEL 1 REF.2
R:12				
R:13				REC CHANNEL 1 REF.3
R:14				
R:15				
R:16				
R:17				
R:18	E:82	T:39		RECORDER 2 REF #1
R:19				
R:20	F:82	T:41		RECORDER 2 REF #2
R:21				
R:22	G:82	T:43		RECORDER 2 REF #3
R:23				
R:24				
R:25	N:11			RECORDER 2 VARIABLE
R:26				
R:27				REC CHANNEL 1 VARIABLE
R:28				
R:29				
R:30				
R:31				
R:32				UNUSED GATE 2 OUT
R:33				
R:34				UNUSED GATE 2 IN
R:35				REC CHANNEL 1 +V,-I
R:36	T:62	S:73		1 MHZ
R:37		S:75		1 MHZ NEU
R:38				UNUSED GATE 1 OUT
R:39				UNUSED GATE 3 IN
R:40				UNUSED GATE 1 IN
R:41				UNUSED GATE 3 IN
R:42				UNUSED GATE 1 IN
R:43				UNUSED GATE 3 OUT
R:44				UNUSED GATE 2 IN
R:45	R:53			DISABLE P C ALARM
R:46		S:19		100 KHZ
R:47	T:47	L:69		100 KHZ SQUAREWAVE
R:48		A:62		LOST XMTR DRIVE LAMP
R:49	K:42			PHASE CODE

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
R:50	P:60			LAMP TEST
R:51	R:86			100 KHZ GATING INTERVAL
R:52		J:10		LOST XMTR DRIVE
R:53	R:83	R:45		PHASE CODE MODE
R:54				
R:55	L:16			MPT RECLOCK
R:56				
R:57				
R:58		S:61	J2-DD	BLANKING
R:59	T:35			MPT
R:60	S:83	M:19		-15 VDC
R:61				RECLOCKED MPT
R:62	S:81	M:17		+15 VDC
R:63				MPT INHIBIT
R:64	T:18			EARLY TRIGGER
R:65		M:68		INTERVAL
R:66		S:27		-MPT
R:67				
R:68		S:25		+MPT
R:69				
R:70	S:49	T:8		+24 VDC
R:71				
R:72				+EARLY TRIGGER
R:73				
R:74				-EARLY TRIGGER
R:75				
R:76		S:33		+P.C. RESET TRIG
R:77				
R:78		S:35		-P.C. RESET TRIG
R:79				
R:80		S:29		+P.C. SET TRIG
R:81				
R:82		S:31		-P.C. SET TRIG
R:83		R:53		+5V (Vcc)
R:84				+5V (Vcc)
R:85				GND
R:86		R:51		GND
S:1			J1-E	GND/RECORDER
S:2				GND
S:3		D:25	J1-D	P0 COUNT BCD PARALLEL
S:4				GND
S:5		D:23	J1-B	P1 COUNT BCD PARALLEL
S:6				GND
S:7		D:26	J1-F	B2 DIGITAL COMPARE BCD
S:8				GND
S:9		D:28	J1-H	B3 DIGITAL COMPARE BCD
S:10				GND

Table 5.5. TD-1365/FPN-65 Timer Wire List (Continued)

PIN	FROM	TO	CABLES	WIRE NAME
S:11	D:30		J1-T	Q0 DECIMAL COUNTER BCD
S:12				GND
S:13	D:32		J1-V	Q1 DECIMAL COUNTER BCD
S:14				GND
S:15	D:34		J1-W	Q2 DECIMAL COUNTER BCD
S:16				GND
S:17	D:36		J1-Y	Q3 DECIMAL COUNTER BCD
S:18				GND
S:19	R:46		J1-J	100 KHZ
S:20				GND
S:21		S:22	J1-L	GND/100 KHZ
S:22	S:21			GND
S:23			J1-N	GND/100 KHZ
S:24				GND
S:25	R:68		J1-S	+XMTR TRIG
S:26				GND
S:27	R:66		J1-P	-XMTR TRIG
S:28				GND
S:29	R:80		J1-X	+P.C. SET
S:30				GND
S:31	R:82		J1-Z	-P.C. SET
S:32				GND
S:33	R:76		J1-e	+P.C. RESET
S:34				GND
S:35	R:78		J1-c	-P.C. RESET
S:36				GND
S:37	T:5		J1-m	+EARLY TRIG
S:38				GND
S:39	T:7		J1-p	-EARLY TRIG
S:40				GND
S:41			J1-s	GND8/EARLY TRIG
S:42		M:1		GND
S:43		M:9	J1-d	RF IN
S:44				GND
S:45	T:50		J1-n	PCI OUT
S:46				GND
S:47			J1-x	GND/5 MHZ SHLD
S:48				GND
S:49	A:81	R:70	J1-K	+24 VDC
S:50				GND
S:51			J1-y	GND/RF INPUT
S:52				GND
S:53	J:52		J1-f	MAJ LORTO OUT
S:54				GND
S:55		J:44	J1-j	MAJ LORTO IN
S:56				GND
S:57			J1-U	GND/XMTR TRIG
S:58				GND
S:59	J:12		J1-k	LOSS ALARM DRIVE

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
S:60				GND
S:61	R:58		J1-r	INTERVAL WAVEFORM
S:62				GND
S:63			J1-b	GND/PC SET
S:64				GND
S:65		D:77	J1-a	5 MHZ INPUT
S:66				GND
S:67		D:85	J1-EE	GND/OPR 1 MHZ
S:68				GND
S:69	A:6	J2-EE	J1-w	OPERATE LAMP
S:70				GND
S:71		A:2	J1-u	STANDBY LAMP
S:72				GND
S:73	R:36		J1-DD	1 MHZ OUT
S:74				GND
S:75	R:37		J1-BB	1 MHZ NEU
S:76				GND
S:77		R:5	J1-A	RECORDER 2 +V,-I
S:78				GND
S:79	R:7		J1-C	RECORDER 2 +I
S:80				GND
S:81		R:62		+15 VDC
S:82				GND
S:83		R:60		-15 VDC
S:84				GND
S:85				GND/PC RESET
S:86				GND
T:1	T:21	T:2	J2-B	GND
T:2	T:1			GND
T:3	T:4		J2-i	+5V (Vcc)
T:4	T:52	T:3		+5V (Vcc)
T:5	T:54	S:37		+ET/MPT
T:6				
T:7	T:56	S:39		-ET/MPT
T:8	R:70			+24 VDC
T:9				GND
T:10			J6	BLANKING IN
T:11	T:29			EMPT
T:12				
T:13				
T:14				ET-INT-L
T:15				
T:16				AUX-INT-L
T:17				
T:18		R:64		ET ALARM
T:19				
T:20			J2-z	GUARD-H
T:21	T:45	T:1		GND

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
T:22	K:33			LOCAL INTERVAL
T:23				
T:24				BLANK-L
T:25		T:46		GUARD HI
T:26		M:14		INHIBIT ERR SNS
T:27				
T:28	T:40			BLINK
T:29		T:11		EMPT
T:30				
T:31				MX-INT-L
T:32				
T:33				C-APT-L
T:34				
T:35		R:59		MPT
T:36				
T:37				TEST RESET
T:38	K:5			MPT9
T:39	R:18			1 MHZ
T:40	P:26	T:28		BLINK
T:41	R:20			1 MHZ
T:42				100 KHZ
T:43	R:22			1 MHZ
T:44		T:47		100 KHZ
T:45	T:48	T:21		GND
T:46	T:25	T:67		RESET
T:47	T:44	R:47		100 KHZ
T:48	T:85	T:45		RESET
T:49	N:16	T:58		5 MHZ
T:50		S:45	J2-CC	PCI
T:51				
T:52	T:83	T:4		+5V (Vcc)
T:53				
T:54		T:5		5 MHZ
T:55		K:48		1 MHZ
T:56		T:7		5 MHZ
T:57				
T:58	T:49			5 MHZ
T:59	N:7			100 KHZ SQUAREWAVE
T:60	K:20			PCI
T:61			J2-p	S24
T:62		R:36		1 MHZ
T:63			J2-q	S22
T:64				
T:65			J2-x	SHIFT
T:66				
T:67	T:46			STROBE
T:68				
T:69			J2-r	S28

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
T:70				
T:71			J2-s	RETARD
T:72				
T:73			J2-t	S11
T:74				
T:75			J2-u	S12
T:76				
T:77			J2-v	S18
T:78				
T:79			J2-w	S14
T:80				
T:81				TEST RESET
T:82				
T:83	T:84	T:52		+5V (Vcc)
T:84	L:3	T:83		+5V (Vcc)
T:85	T:86	T:48		GND
T:86	L:1	T:85	J2-A	GND
J1-A		S:77		RECORDER 2 +V,-I
J1-B		S:5		P1 COUNT BCD PARALLEL
J1-C	S:79			RECORDER 2 +I
J1-D		S:3		P0 COUNT BCD PARALLEL
J1-E	S:1			GND/RECORDER
J1-F		S:7		IN A2
J1-H		S:9		IN A3
J1-J	S:19			100 KHZ
J1-K	S:49			+24 VDC
J1-L		S:21		GND/100 KHZ
J1-N		S:23		GND/100 KHZ
J1-P	S:27			-XMTR TRIG
J1-S	S:25			+XMTR TRIG
J1-T	S:11			OUT A0
J1-U		S:57		GND/XMTR TRIG
J1-V	S:13			OUT A1
J1-W	S:15			OUT A2
J1-X	S:29			+P.C. SET
J1-Y	S:17			OUT A3
J1-Z	S:31			-P.C. SET
J1-a		S:65		5 MHZ
J1-b		S:63		GND/PC SET
J1-c	S:35			-P.C. RESET
J1-d		S:43		RF IN
J1-e	S:33			+P.C. RESET
J1-f	S:53			MAJ LORTO OUT
J1-h	S:85			GND/PC RESET
J1-j		S:55		MAJ LORTO IN
J1-k	S:59			LOSS ALARM DRIVE
J1-m	S:37			+EARLY TRIG

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
J1-n	S:45			PCI OUT
J1-p	S:39			-EARLY TRIG
J1-r	S:61			INTERVAL WAVEFORM
J1-s		S:41		GND/EARLY TRIG
J1-u		S:71		STANDBY LAMP
J1-w		S:69		OPERATE LAMP
J1-x		S:47		GND/5 MHZ SHLD
J1-y		S:51		GND/RF INPUT
J1-BB	S:75			1 MHZ NEU
J1-DD	S:73			1 MHZ OUT
J1-EE	S:67			GND/OPR 1 MHZ
J2-A	T:86			GND
J2-B	T:1			GND
J2-a	E:26			1 DRRG INTERVAL
J2-i	T:3			+5V (Vcc)
J2-p		T:61		S2 4
J2-q		T:63		S2 2
J2-r		T:69		S2 8
J2-s		T:71		RETARD
J2-t		T:73		S1 1
J2-u		T:75		S1 2
J2-v		T:77		S1 8
J2-w		T:79		S1 4
J2-x		T:65		SHIFT
J2-y		T:48		RESET
J2-z	T:20			GUARD
J2-CC	T:50			PCI
J2-DD	R:58			BLANKING
J2-EE		S:69		OPERATE LAMP
J3-A	C:85			GND
J3-B	C:86			GND
J3-C		C:81		CDA 0.02 1
J3-D		C:73		CDA 0.1 1
J3-E		C:71		CDA 0.1 2
J3-F		C:69		CDA 0.1 4
J3-G	C:36			CLEAR
J3-H	C:32			LOAD
J3-J	C:40			RESET TO EXTERNAL
J3-K		C:58		REMOTE BLINK Sx
J3-L		C:60		REMOTE BLINK Sy
J3-M		C:62		REMOTE BLINK Sz
J3-N		C:70		REMOTE MSD 4 ETA
J3-P		C:72		REMOTE MSD 2 ETA
J3-R		C:74		REMOTE MSD 1 ETA
J3-S		C:82		REMOTE LSD 1 ETA
J3-T	C:42			NO EXT AGMT LAMP

Table 5.5. TD-1365/FPN-65 Timer Wire List
(Continued)

PIN	FROM	TO	CABLES	WIRE NAME
J3-U		C:2		CDA 10K 8
J3-V		C:25		CDA 100K 1
J3-W		C:79		CDA 0.02 2
J3-X		C:77		CDA 0.02 4
J3-Y		C:75		CDA 0.02 8
J3-Z		C:63		CDA 1.0 2
J3-a		C:9		SHIFT RIGHT
J3-b		C:19		CDA 100K 8
J3-c		C:51		CDA 10 8
J3-d		C:49		CDA 100 1
J3-e		C:35		CDA 1K 8
J3-f		C:33		CDA 10K 1
J3-g		C:7		SHIFT LEFT
J3-h		C:64		REMOTE BLINK Sw
J3-i		C:66		LOSS XMTR DRIVE
J3-j		C:68		REMOTE MSD 8 ETA
J3-k		C:76		REMOTE LSD 8 ETA
J3-m		C:78		REMOTE LSD 4 ETA
J3-n		C:80		REMOTE LSD 2 ETA
J3-p	C:17			EXECUTE
J3-q		C:67		CDA 0.1 8
J3-r		C:65		CDA 1.0 1
J3-s		C:61		CDA 1.0 4
J3-t		C:59		CDA 1.0 8
J3-u		C:57		CDA 10 1
J3-v	C:44			CHECK TIMING LAMP
J3-w	C:46			ALARM DRIVER
J3-x		C:48		REM RESET TO EXT
J3-y		C:50		BLINK
J3-z	C:6			CLEAR
J3-AA	C:26			LOCAL/REMOTE
J3-BB		C:43		CDA 100 8
J3-CC		C:41		CDA 1K 1
J3-DD		C:11		EXECUTE
J6		T:10		BLANKING IN

6. PARTS LIST.

6.1. Introduction. Table 6.1 lists all of the major components of the Loran-C Timer Set (AN/FPN-54A and AN/FPN-65). Table 6.2 provides the parts listing of each unit of the Loran-C Timer Set. Table 6.3 lists the five-digit manufacturer codes and the respective manufacturers.

Table 6.1. LTS Reference Designations

UNIT	ASSEMBLY OR SUBASSEMBLY	REFERENCE DESIGNATION
CY-7529/FPN	Electrical Equipment Cabinet	1
TD-989A/FPN-54A or TD-1365/FPN-65	Loran-C Timer #1	1A1
	Card File Assembly	1A1A1
	Front Panel	1A1A2
	Timer Chassis	1A1A3
	4.5 to 5.5 VDC Power Supply	1A1A4
	28 VDC Power Supply	1A1A5
	±15 VDC Power Supply	1A1A6
	DC to DC Converter	1A1A7
C-8621A/FPN	Timer Set Control	1A2
	Chassis Assembly	1A2A8
TD-989A/FPN-54A or TD/1365/FPN-65	Loran-C Timer Set #2	1A3
	Card File Assembly	1A3A1
	Front Panel	1A3A2
	Timer Chassis	1A3A3
	4.5 to 5.5 VDC Power Supply	1A3A4
	28 VDC Power Supply	1A3A5
	±15 VDC Power Supply	1A3A6
	DC to DC Converter	1A3A7
PP-7839/G	CDED-312( ) DC Battery Backup Power Supply	1A4

Table 6.2. Parts List

REF SYMBOL	NAME AND DESCRIPTION	MFR OR SOURCE	MFR'S DATA
1	CY-7529/FPN Electrical Equipment Cabinet NOTE: Prefix all REF SYMBOLs with 1		
CY1	CABINET, Electrical Equipment	74156	PC-5213-CGV
E1	PLATE, Filler	EECEN	486-B-142
E2	SLIDE, Chassis, Non-tilting (4 ea)	05236	110QD-22-2
T1	TRANSFORMER, Isolation	80223	HIT-4
TB1	STRIP, Barrier, 15 Terminal	75382	21015
TB1E1	JUMPER, Barrier Strip	75382	601J
TB1E2 thru TB1E6	Same as TB1E1		
W101	HARNESS, 115 VAC Power	EECEN	486-D-140
W101P1	CONNECTOR, Plug, Female, 3-Pin	02660	MS3106A-14S-1S
W102	HARNESS, 115 VAC Interconnect, Power (2 ea)	EECEN	486-B-141
W102P1	CONNECTOR, Plug, Male, 3-Pin	02660	MS3106A-14S-1P
W102P2	Same as W101P1		
W103	HARNESS, 28 VDC Interconnect, Power, 3-Conductor (2 ea)	EECEN	486-B-141
W103P1	CONNECTOR, Plug, Male, 4-Pin	02660	MS3106A-14S-2P
W103P2	CONNECTOR, Plug, Female, 4-Pin	02660	MS3106A-14S-2S
W104	HARNESS, Timer Signal Interconnect, Hybrid Round (2 ea)	EECEN	W0486-24/ INTERCONNECT
W104P1	CONNECTOR, Plug, Male, 55-Pin	09922	MS3126F22-55P
W104P2	CONNECTOR, Plug, Female, 55-Pin	09922	MS3126F22-55S

Table 6.2. Parts List
(Continued)

REF SYMBOL	NAME AND DESCRIPTION	MFR OR SOURCE	MFR'S DATA
W105	HARNESS, 28 VDC Power	EECEN	486-D-140
W105P1	Same as W103P2		
1A1	TD-989A/FPN-54A or TD-1365/FPN-65 Loran-C Timer NOTE: Prefix all REF SYMBOLs with 1A1		
A1	ASSEMBLY, Timer Card File	EECEN	486-J-116
A1A	PRINTED CIRCUIT, Backplane Bus Bar	EECEN	W0486-20A/BUSBAR-C
A1A1A	HARNESS, Timer Front Panel Module	EECEN	W0486-21/FRONT PANEL
A1A1B	PRINTED CIRCUIT, Coding Delay Adjustment Module	EECEN	W0486-5A-CDA
A1A1C	Same as 1A1A1A1B		
A1A1D	PRINTED CIRCUIT, Phase Shift Module	EECEN	W0486-4A/PHASE SHIFT
A1A1E	PRINTED CIRCUIT, Digital Repetition Rate Generator Module	EECEN	W0486-3A/DRRG
A1A1F	Same as 1A1A1A1E		
A1A1G	Same as 1A1A1A1E		
A1A1H	PRINTED CIRCUIT, Program Module	EECEN	W0486-7/PROGRAM
A1A1I	Not used		
A1A1J	PRINTED CIRCUIT, Control Module	EECEN	W0486-12A/CONTROL
A1A1K	PRINTED CIRCUIT, Phase Code/ Multipulse Trigger Module	EECEN	W0486-30/PC/MPT
A1A1L	PRINTED CIRCUIT, Envelope Timing Adjustment Module	EECEN	W0486-11/ETA
A1A1M	PRINTED CIRCUIT, Error Sense Module	EECEN	W0486-10E/ERR SNS

Table 6.2. Parts List
(Continued)

REF SYMBOL	NAME AND DESCRIPTION	MFR OR SOURCE	MFR'S DATA
A1A1N	Same as 1A1A1A1D		
A1A1O	Not used		
A1A1P	PRINTED CIRCUIT, Loran-C Blink Code Generator Module	EECEN	W0486-6A/BLINK
A1A1Q	Not used		
A1A1R	PRINTED CIRCUIT, Interface Module	EECEN	W0486-8A/INTERFACE
A1A1S	HARNESS, Timer Signal Module	EECEN	W0486-22/SIGNAL
A1A2T	PRINTED CIRCUIT, Dual-Rate Interface/Communications Phase Module	EECEN	W0486-28B/DRINT/CP
A1C1	CAPACITOR, Tantalum, 22 uF, 35 VDC	56289	CSR13F226KP
A1P1 thru A1P5	Not used		
A1P6	CONNECTOR, BNC, RF Coaxial, Straight Plug	74868	15875
A1X1A	CONNECTOR, Edge, Termi Twist, One Piece Printed Circuit Double Loaded 43 Position, 86 Contact	00779	67015-6
A1X1B thru A1X1H	Same as 1A1A1X1A		
A1X1I	Not used		
A1X1J thru A1X1N	Same as 1A1A1X1A		
A1X1O	Not used		
A1X1P	Same as 1A1A1X1A		

Table 6.2. Parts List
(Continued)

REF SYMBOL	NAME AND DESCRIPTION	MFR OR SOURCE	MFR'S DATA
A1X1Q	Not used		
A1X1R and A1X1S	Same as 1A1A1X1A		
A1X2T	Same as 1A1A1X1A		
A2	ASSEMBLY, Timer Front Panel	EECEN	486-E-111
A2DS101	Not used		
A2DS102	SWITCH ASSEMBLY, Lighted	96182	10E-A1C1-F10-L(G)-N1-R1V12 CLEAR
A2DS102A	INDICATOR SUBASSEMBLY	96182	10E-A1C1
A2DS102B	SWITCH SUBASSEMBLY	96182	10E-F10
A2DS102C	FILTER, Light, Green (4 ea)	96182	10E-L(G)
A2DS102D	SCREEN, Display	96182	10E-N1
A2DS102E	LENS, Front, Engraved	96182	10E-R1V12 CLEAR
A2DS102F	GUARD, Switch, Clear Plastic	96182	10E-534
A2DS102I1	LAMP, 28 VDC, 0.040A	71744	CM387
A2DS102I2 and A2DS102I3	Not used		
A2DS102I4	Same as 1A1A2DS102I1		
A2DS1C3	SWITCH ASSEMBLY, Lighted	96182	10E-A1C1-F10-L(A)-N1-R1V12 LOAD
A2DS103A	Same as 1A1A2DS102A		
A2DS103B	Same as 1A1A2DS102B		
A2DS103C	FILTER, Light, Amber (4 ea)	96182	10E-L(A)

Table 6.2. Parts List
(Continued)

REF SYMBOL	NAME AND DESCRIPTION	MFR OR SOURCE	MFR'S DATA
A2DS103D	Same as 1A1A2DS102D		
A2DS103E	LENS, Front, Engraved	96182	10E-R1V12 LOAD
A2DS103F	Same as 1A1A2DS102F		
A2DS103I1	Same as 1A1A2DS102I1		
A2DS103I2 and A2DS103I3	Not used		
A2DS103I4	Same as 1A1A2DS102I1		
A2DS104	SWITCH ASSEMBLY, Lighted	96182	10E-A1C1-F10-L(A)-N1-R1V12 EXECUTE
A2DS104A	Same as 1A1A2DS102A		
A2DS104B	Same as 1A1A2DS102B		
A2DS104C	Same as 1A1A2DS103C (4 ea)		
A2DS104D	Same as 1A1A2DS102D		
A2DS104E	LENS, Front, Engraved	96182	10E-R1V12 EXECUTE
A2DS104F	Same as 1A1A2DS102F		
A2DS104I1	Same as 1A1A2DS102I1		
A2DS104I2 and A2DS104I3	Not used		
A2DS104I4	Same as 1A1A2DS102I1		
A2DS105	INDICATOR ASSEMBLY, Lighted	96182	10E-A2C1-L(R)-N1-R1V13 DRRG 1
A2DS105A	INDICATOR SUBASSEMBLY	96182	10E-A2C1

Table 6.2. Parts List
(Continued)

REF SYMBOL	NAME AND DESCRIPTION	MFR OR SOURCE	MFR'S DATA
A2DS105B	Not used		
A2DS105C	FILTER, Light, Red (4 ea)	96182	10E-L(R)
A2DS105D	Same as 1A1A2DS102D		
A2DS105E	LENS, Front, Engraved	96182	10E-R1V13 DRRG 1
A2DS105F	Not used		
A2DS105I1	Same as 1A1A2DS102I1		
A2DS105I2 and A2DS105I3	Not used		
A2DS105I4	Same as 1A1A2DS102I1		
A2DS106	INDICATOR ASSEMBLY, Lighted	96182	10E-A2C1-L(R)-N1-R1V13 DRRG 2
A2DS106A	Same as 1A1A2DS105A		
A2DS106B	Not used		
A2DS106C	Same as 1A1A2DS105C (4 ea)		
A2DS106D	Same as 1A1A2DS102D		
A2DS106E	LENS, Front, Engraved	96182	10E-R1V13 DRRG 2
A2DS106F	Not used		
A2DS106I1	Same as 1A1A2DS102I1		
A2DS1C6I2 and A2DS106I3	Not used		
A2DS106I4	Same as 1A1A2DS102I1		
A2DS107	INDICATOR ASSEMBLY, Lighted	96182	10E-A2C1-L(R)-N1-R1V13 DRRG 3

Table 6.2. Parts List
(Continued)

REF SYMBOL	NAME AND DESCRIPTION	MFR OR SOURCE	MFR'S DATA
A2DS107A	Same as 1A1A2DS105A		
A2DS107B	Not used		
A2DS107C	Same as 1A1A2DS105C (4 ea)		
A2DS107D	Same as 1A1A2DS102D		
A2DS107E	LENS, Front, Engraved	96182	10E-R1V13 DRRG 3
A2DS107F	Not used		
A2DS107I1	Same as 1A1A2DS102I1		
A2DS107I2 and A2DS107I3	Not used		
A2DS107I4	Same as 1A1A2DS102I1		
A2DS108	SWITCH ASSEMBLY, Lighted	96182	10E-A1C1-F10-L(R)-N1-R1V13 CHECK TIMING
A2DS108A	Same as 1A1A2DS102A		
A2DS108B	Same as 1A1A2DS102B		
A2DS108C	Same as 1A1A2DS105C (4 ea)		
A2DS108D	Same as 1A1A2DS102D		
A2DS108E	LENS, Front, Engraved	96182	10E-R1V13-CHECK TIMING
A2DS108F	Same as 1A1A2DS102F		
A2DS108I1	Same as 1A1A2DS102I1		
A2DS108I2 and A2DS108I3	Not used		

Table 6.2. Parts List
(Continued)

REF SYMBOL	NAME AND DESCRIPTION	MFR OR SOURCE	MFR'S DATA
A2DS108I4	Same as 1A1A2DS102I1		
A2DS109	SWITCH ASSEMBLY, Lighted	96182	10E-A1C1-F10-L(R)-N1-R1V14 RESET TO EXTERNAL
A2DS109A	Same as 1A1A2DS102A		
A2DS109B	See 1A1A2DS109		
A2DS109C	Same as 1A1A2DS105C (4 ea)		
A2DS109D	Same as 1A1A2DS102D		
A2DS109E	LENS, Front, Engraved	96182	10E-R1V14 RESET TO EXTERNAL
A2DS109F	Same as 1A1A2DS102F		
A2DS109I1	Samd as 1A1A2DS102I1		
A2DS109I2 and A2DS109I3	Not used		
A2DS109I4	Same as 1A1A2DS102I1		
A2DS110	SWITCH ASSEMBLY, Lighted	96182	10E-A1C1-F10-L(GGAA)-N2-R1V16 LOCAL/REMOTE
A2DS110A	Same as 1A1A2DS102A		
A2DS110B	Same as 1A1A2DS102B		
A2DS110C1	Same as 1A1A2DS102C (2 ea)		
A2DS110C2	Same as 1A1A2DS103C (2 ea)		
A2DS110D	SCREEN, Display	96182	10E-N2
A2DS110E	LENS, Front, Engraved	96182	10E-R1V16 LOCAL/REMOTE

Table 6.2. Parts List
(Continued)

REF SYMBOL	NAME AND DESCRIPTION	MFR OR SOURCE	MFR'S DATA
A2DS110F	SAME AS 1A1A2DS202F		
A2DS110I1 thru A2DS110I	Same as 1A1A2DS102I1		
A2DS111	INDICATOR ASSEMBLY, Lighted	96182	10E-A2C1-L(R)-N1 R1V14 NO EXTERNAL AGREEMENT
A2DS111A	Same as 1A1A2DS105A		
A2DS111B	Not used		
A2DS111C	Same as 1A1A2DS105C (4 ea)		
A2DS111D	Same as 1A1A2DS102D		
A2DS111E	LENS, Front, Engraved	96182	10E-R1V14 NO EXTERNAL AGREEMENT
A2DS111F	Not used		
A2DS111I1	Same as 1A1A2DS102I1		
A2DS111I2 and A2DS111I3	Not used		
A2DS111I4	Same as 1A1A2DS102I1		
A2DS112	INDICATOR ASSEMBLY, Lighted	96182	10E-A2C1-L(GGWW)-N2-R1V16 OPERATE/ STANDBY
A2DS112A	Same as 1A1A2DS105A		
A2DS112B	Not used		
A2DS112C1	Same as 1A1A2DS102C (2 ea)		
A2DS112C2	FILTER, Light, White (2 ea)	96182	10E-L(W)
A2DS112D	Same as 1A1A2DS110D		

Table 6.2. Parts List
(Continued)

REF SYMBOL	NAME AND DESCRIPTION	MFR OR SOURCE	MFR'S DATA
A2DS112E	LENS, Front, Engraved	96182	10E-R1V16 OPERATE/ STANDBY
A2DS112F	Not used		
A2DS112I1 thru A2DS112I4	Same as 1A1A2DS102I1		
A2DS113	INDICATOR ASSEMBLY, Lighted	96182	10E-A2C1-L(A)N1-R1V12 BLINK
A2DS113A	Same as 1A1A2DS105A		
A2DS113B	Not used		
A2DS113C	Same as 1A1A2DS103C (4 ea)		
A2DS113D	Same as 1A1A2DS102D		
A2DS113E	LENS, Front, Engraved	96182	10E-R1V12 BLINK
A2DS113F	Not used		
A2DS113I1	Same as 1A1A2DS102I1		
A2DS113I2 and A2DS113I3	Not used		
A2DS113I4	Same as1A1A2DS102I1		
A2DS114	SWITCH ASSEMBLY, Lighted	96182	90E-A1C4-J1(A)-L1-N1R12 W
A2DS114A	SWITCH, Push	96182	90E-A1C4
A2DS114B	FILTER, Indicator, Amber	96182	90E-JI(A)
A2DS114C	SCREEN, Display, Full	96182	90E-L1
A2DS114D	LENS, Front, Engraved	96182	90E-N1R12 W

Table 6.2. Parts List
(Continued)

REF SYMBOL	NAME AND DESCRIPTION	MFR OR SOURCE	MFR'S DATA
A2DS114I1 and A2DS114I2	Same as 1A1A2DS102I1		
A2DS115	SWITCH ASSEMBLY, Lighted	96182	90E-A1C4-J1-(A)-L1-N1R12 X
A2DS115A	Same as 1A1A2DS114A		
A2DS115B	Same as 1A1A2DS114B		
A2DS115C	Same as 1A1A2DS114C		
A2DS115D	LENS, Front, Engraved	96182	90E-N1R12 X
A2DS115I1 and A2DS115I2	Same as 1A1A2DS102I1		
A2DS116	SWITCH ASSEMBLY, Lighted	96182	90E-A1C4-J1(A)-L1-N1R12 Y
A2DS116A	Same as 1A1A2DS114A		
A2DS116B	Same as 1A1A2DS114B		
A2DS116C	Same as 1A1A2DS114C		
A2DS116D	LENS, Front, Engraved	96182	90E-N1R12 Y
A2DS116I1 and A2DS116I2	Same as 1A1A2DS102I1		
A2DS117	SWITCH ASSEMBLY, Lighted	96182	90E-A1C4-J1(A)-L1-N1R12 Z
A2DS117A	Same as 1A1A2DS114A		
A2DS117B	Same as 1A1A2DS114B		
A2DS117C	Same as 1A1A2DS114C		
A2DS117D	LENS, Front, Engraved	96182	90E-N1R12 Z

Table 6.2. Parts List
(Continued)

REF SYMBOL	NAME AND DESCRIPTION	MFR OR SOURCE	MFR'S DATA
A2DS117I1 and A2DS117I2	Same as 1A1A2DS102I1		
A2DS118	Not used		
A2DS119	INDICATOR ASSEMBLY, Lighted	96182	10E-A2C1-L(R)-N1-R1V14 NO TRANSMITTER DRIVE
A2DS119A	Same as 1A1A2DS105A		
A2DS119B	Not used		
A2DS119C	Same as 1A1A2DS105C (4 ea)		
A2DS119D	Same as 1A1A2DS102D		
A2DS119E	LENS, Front, Engraved	96182	10E-R1V14 NO TRANSMITTER DRIVE
A2DS119F	Not used		
A2DS119I1	Same as 1A1A2DS102I1		
A2DS119I2 and A2DS119I3	Not used		
A2DS119I4	Same as 1A1A2DS102I1		
A2DS120	SWITCH ASSEMBLY, Lighted	96182	90E-A1C2-J1(A)-L1-N1R13 LAMP TEST
A2DS120A	SWITCH, Push	96182	90E-A1C2
A2DS120B	Same as 1A1A2DS114B		
A2DS120C	Same as 1A1A2DS114C		
A2DS120D	LENS, Front, Engraved	96182	90E-N1R13 LAMP TEST
A2DS120I1 and A2DS120I2	Same as 1A1A2DS102I1		

Table 6.2. Parts List
(Continued)

REF SYMBOL	NAME AND DESCRIPTION	MFR OR SOURCE	MFR'S DATA
A2R1	RESISTOR, Fixed Composition 4.7 kOhm, 10%, 1/4 Watt	01121	RCR07G472JS
A2R2	Same as 1A1A2R1		
A2R3	RESISTOR, Fixed Composition 10 Ohm, 10%, 1/4 Watt	01121	RCR07G100JS
A2R4	RESISTOR, Fixed Composition 240 Ohm, 5%, 1/4 Watt	01121	RCR07G241JS
A2S101	SWITCH ASSEMBLY, Thumbwheel, 9 Section	07126	9-U-11 (REV.A)
A2S101A	SWITCH, Code Indicating, Thumbwheel, 8 position, +/-	07126	
A2S101B	SWITCH, Code Indicating, Thumbwheel, 10 position, 0-9	07126	
A2S101C thru A2S101H	Same as 1A1A2S101B		
A2S101I	Not used		
A2S101J	Same as 1A1A2S101B		
A2S102 thru A2S108	Not used		
A2S109	SWITCH, One Shot	91929	2D604
A2S110 thru A2S117	Not used		
A2S118	SWITCH ASSEMBLY, Thumbwheel, 2 Section	07126	9-U-12 (REV.A)
A2S118A and A2S118B	Same as 1A1A2S101B		

Table 6.2. Parts List
(Continued)

REF SYMBOL	NAME AND DESCRIPTION	MFR OR SOURCE	MFR'S DATA
A2XS101A	CONNECTOR, Edge, 10 Position	71785	50-10A-20
A2XS101B thru A2XS101H	Same as 1A1A2XS101A		
A2XS101I	Not used		
A2XS101J	Same as 1A1A2XS101A		
A2XS102 thru A2XS117	Not used		
A2XS118A and A2XS118B	Same as 1A1A2XS101A		
A3	ASSEMBLY, Timer Chassis	EECEN	486-J-103
A3J1	CONNECTOR, Receptacle, Female, Box Mounting Flange	09922	MS3122E 22 55S P/O 1A1A1A1S
A3J2	CONNECTOR, Receptacle, Female, Box Mounting Flange	09922	MS3122E 22 55 SX
A3J3	CONNECTOR, Receptacle, Female, Box Mounting Flange	09922	MS3122E 22 55A SY
A3J4	CONNECTOR, Receptacle, Male, Box Mounting Flange	02660	MS3102A14S-1P
A3J5	CONNECTOR, Receptacle, Male, Box Mounting Flange	71468	MS3102A14S-2P
A3J6	ADAPTER, Bulkhead, BNC, UG-492A/U	74868	31-220
A3TB1	STRIP, Barrier, 10 Terminal	75382	20010
A4	POWER SUPPLY, Regulated 4.5 to 5.5 VDC	09004	TMD-4.5-5.5-5.0
A5	POWER SUPPLY, Regulated 28 VDC +2 VDC, 4 Amp	97328	M28-0400

Table 6.2. Parts List
(Continued)

REF SYMBOL	NAME AND DESCRIPTION	MFR OR SOURCE	MFR'S DATA
A6	POWER SUPPLY, Regulated, Dual Output ±15 VDC, 0.30 Amp	80103	LXD-3-152R with LC-OV-11
A7	ASSEMBLY, DC to DC Converter	EECEN	486-D-118
A7A1	POWER SUPPLY, DC to DC Converter, 28 to 5.5 VDC, 4 Amp	11352	3050-28-105-OV(A)
A7CR1	DIODE, Silicon, 400 PIV, 12.0 Amp	02735	1N1204A
A7CR2	Same as 1A1A7CR1		
A7CR3	DIODE, Zener, 5.1 V, 50 Watt	04713	1N4552
A7E1	TERMINAL, Teflon, Press Fit	71279	4258-1 05-19
A7E2	Same as 1A1A7E1		
A7TB1	Same as 1A1A3TB1		
1A2	C-8621A/FPN TIMER SET CONTROL NOTE: Prefix all REF SYM with 1A2		
A8	ASSEMBLY, Timer Set Control Chassis	EECEN	486-J-130
A8A1	ALARM, Sonalert Pulsing, 2900 Hz, 6-28 VDC, 3-14 MA	90201	SC628W
A8A2	ALARM, Sonalert, 2900 Hz, 6-28 VDC, 3-14 MA	90201	SC628
A8AT1	ADAPTOR, Terminating Cap, BNC 51 Ohm	02660	357-25-51
A8AT2 thru A8AT4	Same as 1A2A8AT1		
A8CB1	CIRCUIT BREAKER, Lighted Pushbutton 5 Amp, 115 VAC		SEE BREAKDOWN
A8CB1A	Same as 1A1A2DS102A		
A8CB1B	CIRCUIT BREAKER SUBASSEMBLY	81541	APB-1RNS-1660-1
A8CB1C	Same as 1A1A2DS103C (4 ea)		

Table 6.2. Parts List
(Continued)

REF SYMBOL	NAME AND DESCRIPTION	MFR OR SOURCE	MFR'S DATA
A8CB1D	Same as 1A1A2DS102D		
A8CB1E	LENS, Front, Engraved	96182	10E-R1V13 TIMER 1/ 115 VAC
A8CB1F	Same as 1A1A2DS102F		
A8CB1I1	LAMP, Neon, 115 VAC	96182	10E-J4
A8CB1I2 and A8CB1I3	Not used		
A8CB1I	Same as 1A2A8CB1I1		
A8CB1R1	RESISTOR, Fixed Composition, 33 kOhm, 5%, 1/4 Watt	01121	RCR07G333JS
A8CB1R2	Same as 1A2A8CB1R1		
A8CB2	CIRCUIT BREAKER, Lighted Pushbutton 5 Amp, 115 VAC		SEE BREAKDOWN
A8CB2A	Same as 1A1A2DS102A		
A8CB2B	Same as 1A2A8CB1B		
A8CB2C	Same as 1A1A2DS103C (4 ea)		
A8CB2D	Same as 1A1A2DS102D		
A8CB2E	LENS, Front, Engraved	96182	10E-R1V13 TIMER 2/ 115 VAC
A8CB2F	Same as 1A1A2DS102F		
A8CB2I1	Same as 1A2A8CB1I1		
A8CB2I2 and A8CB2I3	Not used		
A8CB2I4	Same as 1A2A8CB1I1		
A8CB2R1	Same as 1A2A8CB1R1		

Table 6.2. Parts List
(Continued)

REF SYMBOL	NAME AND DESCRIPTION	MFR OR SOURCE	MFR'S DATA
A8CB2R2	Same as 1A2A8CB1R1		
A8CP1	T ADAPTER, BNC, UG 274C/U	02660	31-008
A8CP2 thru A8CP4	Same as 1A2A8CP1		
A8DC1	CIRCUIT BOARD, Diode Capacitor	EECEN	486-B-139
A8DC1C1	Same as 1A1A1C1		
A8DC1CR1	DIODE	03877	1N647
A8DC1CR2	Same as 1A2A8DC1CR1		
A8F1	FUSE, Cartridge, 2 Amp, 250 V, 3AG, SLO-BLO	75915	F02B250V2AS
A8F2	Same as 1A2A8F1		
A8F3	Same as 1A2A8F1, SPARE		
A8F4	Same as 112A8F1, SPARE		
A8J1	CONNECTOR, Receptacle, Male, Box Mounting Flange	09922	MS3122E 22-55P
A8J2	Same as 1A2A8J1		
A8J3	CONNECTOR, Receptacle, Female, Box Mounting Flange	02660	MS3102A 14S-2S
A8J4	CONNECTOR, Receptacle, UHF-Twin Contact, UG-103/U	02660	83-22R
A8J5	Same as 1A2A8J4		
A8J6	CONNECTOR, Receptacle, Female, Box Mounting Flange	02660	MS3102A 14S-1S
A8J7	CONNECTOR, Socket, Twinax Square Flange, UG-422/U	74868	6225

Table 6.2. Parts List
(Continued)

REF SYMBOL	NAME AND DESCRIPTION	MFR OR SOURCE	MFR'S DATA
A8J8 thru A8J11	Same as 1A2A8J7		
A8J12	Same as 1A1A3J5		
A8J13	CONNECTOR, Receptacle, Panel, UHF, SO-239A	74868	83-798
A8J14	P/O 1A2A8Z1		
A8J15	Same as 1A1A3J4		
A8J16	Same as 1A2A8J6		
A8J17	Same as 1A2A8J4		
A8J18	Same as 1A2A8J4		
A8J19	Same as 1A2A8J3		
A8J20 thru A8J24	Same as 1A2A8J7		
A8J25	Same as 1A1A3J4		
A8J26	CONNECTOR, Receptacle, Bulkhead BNC, UG492D/U	74868	31-3220
A8J27	Same as 1A2A8J26		
A8J28	CONNECTOR, Receptacle, Bulkhead, UG-1094/U	02660	31-221
A8J29	CONNECTOR, Receptacle, Male, Box Mounting Flange	09922	MS3112E 8-3P
A8J30 thru A8J32	Same as 1A2A8J28		
A8J33	Same as 1A2A8J29		

Table 6.2. Parts List
(Continued)

REF SYMBOL	NAME AND DESCRIPTION	MFR OR SOURCE	MFR'S DATA
A8M1	METER, Panel, 0-30 VDC, 1 kOhm/V, 1-1/2"	55026	1212C-9544
A8M2	Same as 1A2A8M1		
A8P1A	CONNECTOR, T-Bar	14195	88631-G76
A8P2B	Same as 1A2A8P1A		
A8P3C	Same as 1A2A8P1A		
A8P4A	Same as 1A2A8P1A		
A8P5B	Same as 1A2A8P1A		
A8P6C	Same as 1A2A8P1A		
A8P7	Same as 1A1A1P6		
A8P8	Same as 1A1A1P6		
A8P9 thru A8P25	Not used		
A8P26	Same as 1A1A1P6		
A8P27	Same as 1A1A1P6		
A8R1	See A8CB2R1		
A8R2	See A8CB2R1		
A8R3	Not used		
A8R4	RESISTOR, Fixed Composition, 51 Ohm, 5%, 1/4 Watt	01121	RCR07G510JS
A8R5	Same as 1A2A8R4		
A8S1	SWITCH, Toggle, T-Bar, 36 PDT	14195	832G-36CR
A8S2	SWITCH ASSEMBLY, Lighted	96182	90E-A1C4-J1(R)-L1-N1R14 AUDIO ALARM INHIBIT

Table 6.2. Parts List
(Continued)

REF SYMBOL	NAME AND DESCRIPTION	MFR OR SOURCE	MFR'S DATA
A8S2A	Same as 1A1A2DS114A		
A8S2B	FILTER, Indicator, Red	96182	90E-JI(R)
A8S2C	Same as 1A1A2DS114C		
A8S2D	LENS, Front, Engraved	96182	90E-N1R14 AUDIO ALARM INHIBIT
A8S2I1 and A8S2I2	Same as 1A1A2DS102I1		
A8XF1	HOLDER, Fuse	75915	FHN20G
A8XF2	Same as 1A2A8XF1		
A8XF3	Same as 1A2A8XF1, SPARE		
A8XF4	Same as 1A2A8XF1, SPARE		
A8Z1	POWER DIVIDER/COMBINER, 2-Way	32252	B-HJ-235
1A3	SAME AS 1A1 NOTE: Prefix all REF SYM with 1A3		
1A4	PP-7839/G POWER SUPPLY	19397	312( )

Table 6.3. List of Manufacturers

EECEN	USCG Electronics Engineering Center P. O. Box 60 Wildwood, NJ 08260-0060
00779	Amp Inc. P. O. Box 3608 Harrisburg, PA 17105
01121	Allen-Bradley Co. 1201 South 2nd Street Milwaukee, WI 53204
02660	Bunker Ramo-Eltra Corp. Amphenol Division 2801 S. 25th Avenue Broadview, IL 60153
02735	RCA Corp. Solid State Division Route 202 Somerville, NJ 08876
03877	Incon Transitron Electronics Corp. 316 Ash Street Reading, MA 01867
04713	Motorola Semiconductor Products Sales Subsidiary of Motorola Inc. 4828 E. McDowell Road Phoenix, AZ 85008
07126	Becton Dickson and Co. The Digitran Co. Division 855 S. Arroyd Parkway Pasadena, CA 91105
09004	Transistor Devices Inc. 85 Horsehill Road Cedar Knolls, NJ 07927

Table 6.3. List of Manufacturers
(Continued)

09922	Burndy Corp. Richards Avenue Norwalk, CT 06856
11352	Tecnetics Inc. 6287 Arapahoe Avenue P. O. Box 910 Boulder, CO 80302
14195	T-BAR Inc. 141 Danbury Road Wilton, CT 06897
19397	Tracor Inc. Corporate Headquarters 6500 Tracor Lane Austin, TX 78721
32252	Olektron Corp. 61 Sutton Road Webster, MA 01570
55026	American Gage and machine Co. Simpson Electric Co. Division 853 Dundee Avenue Elgin, IL 60120
56289	Sprague Specialties Co. 87 Marshall Street North Adams, MA 01247
71279	Midland-Ross Corp. Cambion Division One Alewife Place Cambridge, MA 02140
71468	ITT Cannon Electric Division of International Telephone and Telegraph Corporation 10550 Talbert Avenue P. O. Box 8040 Fountain Valley, CA 92708

Table 6.3. List of Manufacturers
(Continued)

71744	General Instrument Corp. Lamp Division/Worldwide 4433 N. Ravenswood Avenue Chicago, IL 60640
74156	Par-Metal Products 1260 Atlantic Avenue Brooklyn, NY 11216
74868	Bunker Ramo-Eltra Corp. Amphenol Division RF Operations 33 E. Franklin Street Danbury, CT 06810
75382	Kulka Electric Corp. Subsidiary of North American Philips Corp. 520 S. Fulton Avenue Mt Vernon, NY 10551
75915	Tracor Littlefuse Inc. 800 E. Northwest Highway Desplains, IL 60016
80103	Veeco Instruments Inc. Lambda Electronics Division 515 Broad Hollow Road Melville, NY 11746
80223	TRW Inc. TRW Inductive Products 150 Varick Street New York, NY 10013
81541	Airpax Electronics Inc. Woods Road Cambridge, MD 21613

Table 6.3. List of Manufacturers
(Continued)

90201	Mallory Capacitor Co. Subsidiary of Emhart Industries Inc. 4760 Kentucky Avenue P. O. Box 372 Indianapolis, IN 46206
91929	Honeywell Inc. Micro Switch Division 11 W. Spring Street Freeport, IL 61032
96182	Master Specialties Co. 1640 Monrovia Costa Mesa, CA 92627
97328	Universal Electronics Corp. Chatsworth, CA

7. DIAGRAMS AND SCHEMATICS.

7.1. Introduction. The following is a list of diagrams and schematics:

Figure	Title
7.1	Loran-C Timer Functional Block Diagram
7.2	W0486-3A/DRRG Block Diagram
7.3	W0486-3A/DRRG Schematic Diagram
7.4	W0486-3A/DRRG Parts Locator
7.5	W0486-4A/Ø-SHIFT Block Diagram
7.6	W0486-4A/Ø-SHIFT Schematic Diagram
7.7	W0486-4A/Ø-SHIFT Parts Locator
7.8	W0486-5A/CDA Block Diagram
7.9	W0486-5A/CDA Schematic Diagram
7.10	W0486-5A/CDA Parts Locator
7.11	W0486-6A/BLINK Block Diagram
7.12	W0486-6A/BLINK Schematic Diagram
7.13	W0486-6A/BLINK Parts Locator
7.14	W0486-7/PROGRAM Parts Locator
7.15	W0486-8A/INTERFACE Block Diagram
7.16	W0486-8A/INTERFACE Schematic Diagram
7.17	W0486-8A/INTERFACE Parts Locator
7.18	W0486-10E/ERR SNS Block Diagram
7.19	W0486-10E/ERR SNS Schematic Diagram
7.20	W0486-10E/ERR SNS Parts Locator
7.21	W0486-11/ETA Block Diagram
7.22	W0486-11/ETA Schematic Diagram
7.23	W0486-11/ETA Parts Locator
7.24	W0486-12A/CONTROL Block Diagram
7.25	W0486-12A/CONTROL Schematic Diagram
7.26	W0486-12A/CONTROL Parts Locator
7.27	W0486-28B/DRINT/CP Block Diagram
7.28	W0486-28B/DRINT/CP Schematic Diagram
7.29	W0486-28B/DRINT/CP Parts Locator
7.30	W0486-30/PC/MPT Block Diagram
7.31	W0486-30/PC/MPT Schematic Diagram
7.32	W0486-30/PC/MPT Parts Locator
7.33	Loran-C Timer Set Control Schematic Diagram
7.34	Special Symbols

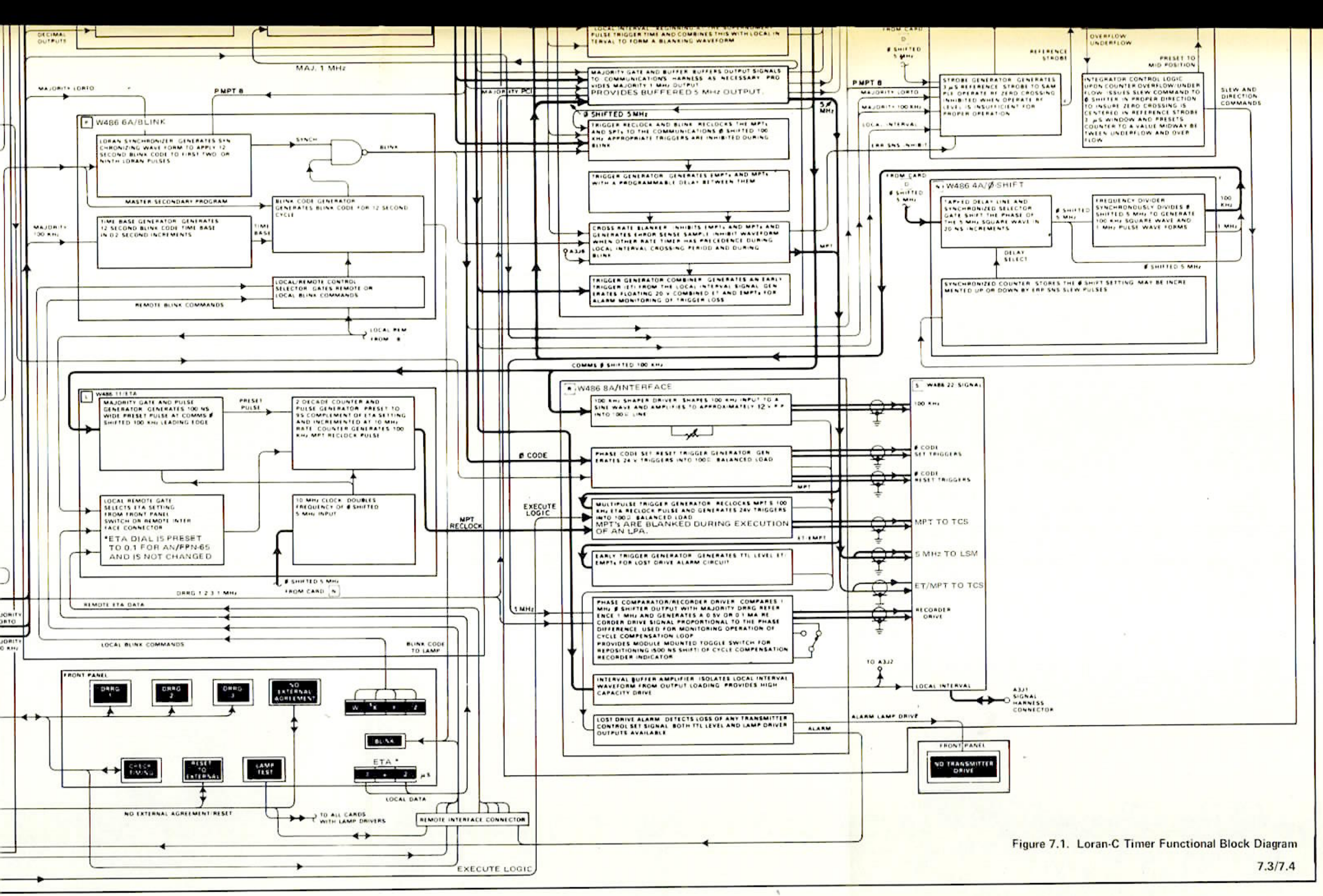


Figure 7.1. Loran-C Timer Functional Block Diagram

CONTROL WAVEFORM

K W486-30/PC/MPT

X100 X10 X1 μs

0 0 0 REFERENCE STROBE ADJUSTMENT

PHASE CODE GENERATOR DEVELOPS MAJORITY PCI AND GATES THIS WITH 1000 μS INCREMENTS FROM INTERVAL GENERATOR AND PROGRAM CARD INPUTS TO GENERATE STANDARD LORAN C PHASE CODE. SWITCH (S4) TUBE/5SX WHEN IN THE 5SX POSITION DELAYS MPT'S AND EXTENDS LOCAL INTERVAL WAVEFORM.

MAJORITY PCI

Ø CODE

PCI

1000 μS INCREMENTS

LOCAL INTERVAL

MAJORITY LORTO

CONTROL SHAPING GATES PRODUCE LOCAL INTERVAL AND MODULE CONTROL INFORMATION FROM DRRG AND PROGRAM CARD DATA

CONTROL DATA

MULTIPULSE TRIGGER GENERATOR PRODUCES COARSE TIMED 200 NS FALSE MULTIPULSE TRIGGERS. MPTR IS USED FOR 1RF SNS CONTROL. MPTS IS USED FOR TRANSMITTER CONTROL SET TRIGGERS

P MPT 8

P MPT 9

TRANSMITTER INTERFACE

A3J2

PCI FROM CARD 1

COMMS HARNESS

TIMER STATUS OF STANDBY

5 W486 22 SIGNAL

OPERATE RT

COMM DATA

MAJ 1 MHz

MAJORITY PCI

Ø CODE

Ø SHIFTED 5 MHz

1 W486 28B/DRINT/CP

DIGITAL PHASE SHIFTER ADVANCES OR RETARDS THE 100 KHz SIGNAL IN 0.2 μS INCREMENTS IN RESPONSE TO COMMANDS RECEIVED FROM THE COMMUNICATIONS MODULATORS.

100 KHz

BLANKING WAVEFORM GENERATOR GENERATES a 400 μS

M W486 10E/ERR SNS

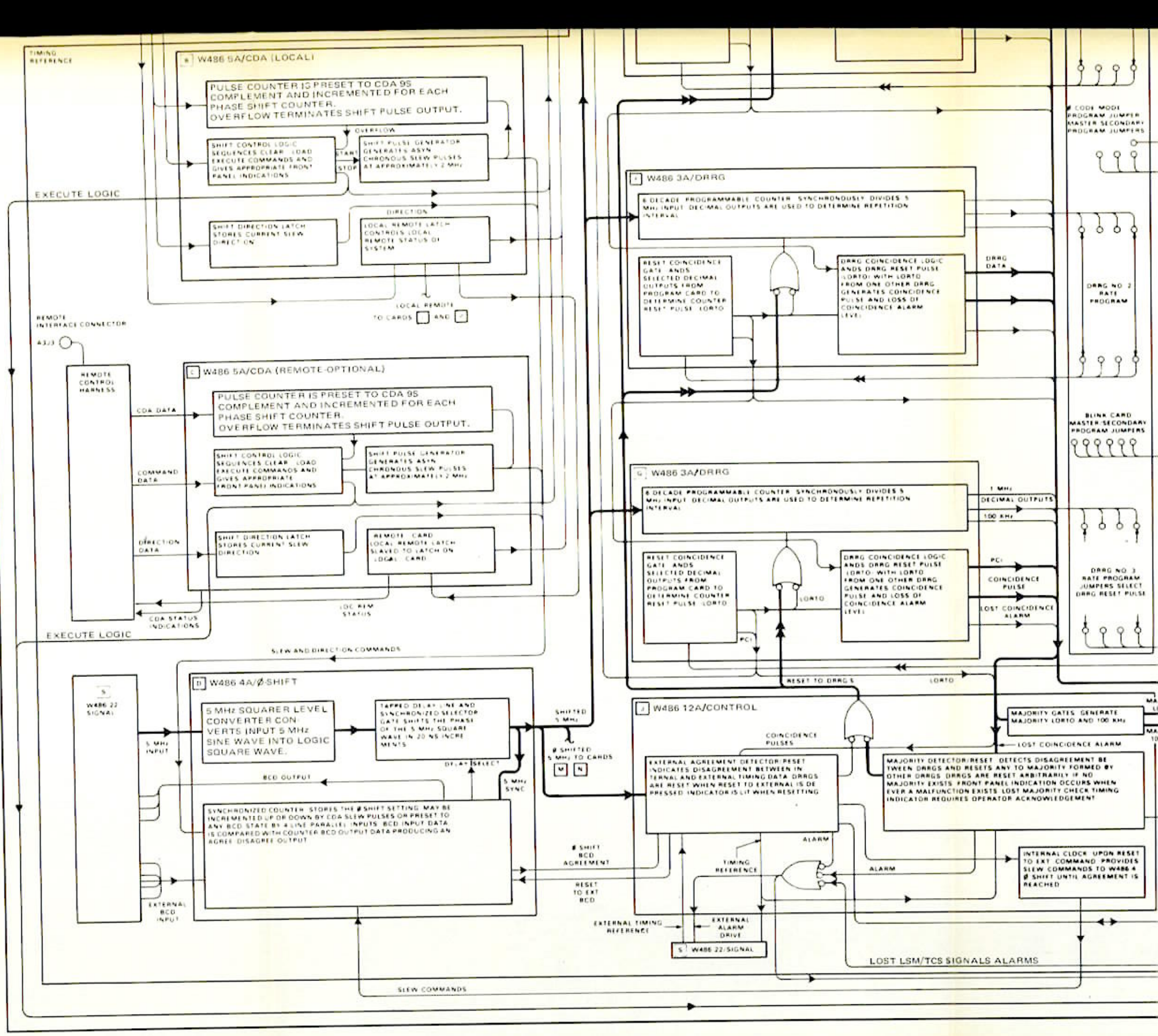
THRESHOLD DETECTOR HARD-LIMITS OPERATE RF AND REMOVES PHASE CODE

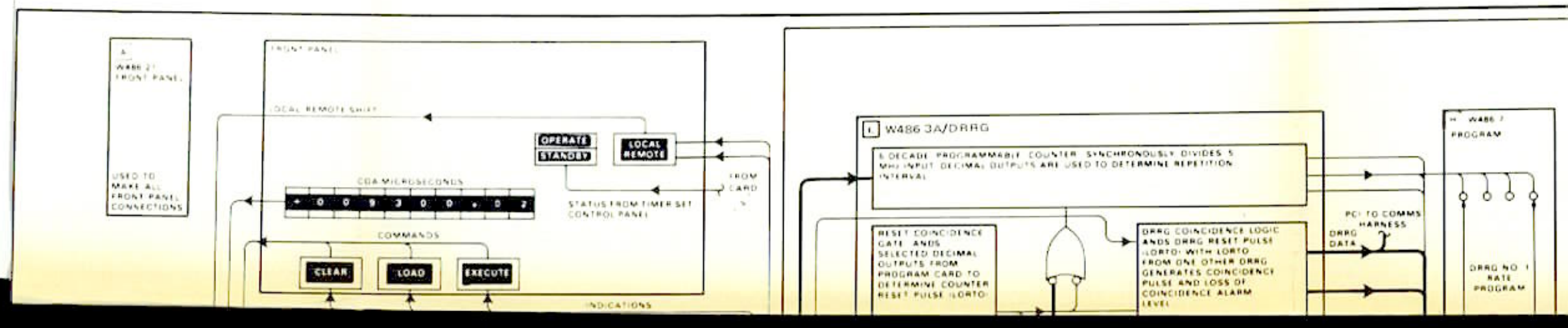
HARD LIMITED RF ZERO CROSSING

DIGITAL INTEGRATOR REPEATEDLY MEASURES THE TIME FROM THE LEFT EDGE OF THE REFERENCE STROBE TO THE ZERO CROSSING AND SUBTRACTS THE TIME FROM THE ZERO CROSSING TO THE RIGHT EDGE OF THE REFERENCE STROBE WHEN THE POLARITY OF THE DIFFERENCE IS CONSISTENT. AN UP/DOWN COUNTER WILL OVERFLOW OR UNDERFLOW INTEGRATOR TIME CONSTANT IS MODULUS OF UP/DOWN COUNTER PROGRAMMED UPON INSTALLATION

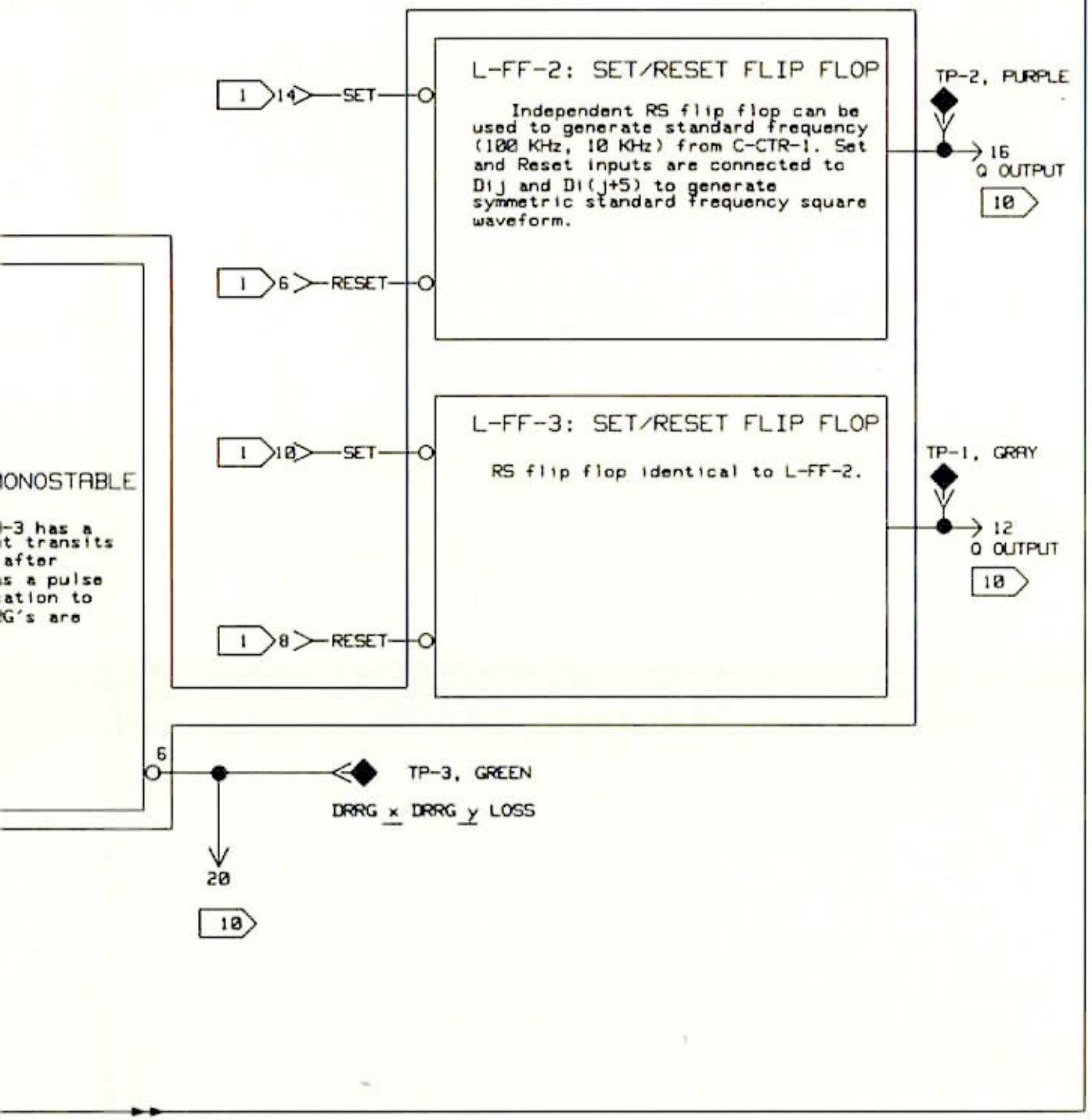
TIME CONSTANT PROGRAM JUMPERS

STROBE INHIBIT


TIMING REFERENCE
B W486 5A/CDA (LOCAL)
PULSE COUNTER IS PRESET TO CDA 95 COMPLEMENT AND INCREMENTED FOR EACH PHASE SHIFT COUNTER. OVERFLOW TERMINATES SHIFT PULSE OUTPUT.
OVERFLOW
SHIFT CONTROL LOGIC SEQUENCES CLEAR - LOAD EXECUTE COMMANDS AND GIVES APPROPRIATE FRONT PANEL INDICATIONS
START
STOP
SHIFT PULSE GENERATOR GENERATES ASYNCHRONOUS SLEW PULSES AT APPROXIMATELY 2 MHz
EXECUTE LOGIC
SHIFT DIRECTION LATCH STORES CURRENT SLEW DIRECTION
DIRECTION
LOCAL REMOTE LATCH CONTROLS LOCAL REMOTE STATUS OF SYSTEM
LOCAL REMOTE
TO CARDS K AND J
REMOTE INTERFACE CONNECTOR
A3J3
REMOTE CONTROL HARNESS
C W486 5A/CDA (REMOTE-OPTIONAL)
CDA DATA
PULSE COUNTER IS PRESET TO CDA 95 COMPLEMENT AND INCREMENTED FOR EACH PHASE SHIFT COUNTER. OVERFLOW TERMINATES SHIFT PULSE OUTPUT.
COMMAND DATA
SHIFT CONTROL LOGIC SEQUENCES CLEAR - LOAD EXECUTE COMMANDS AND GIVES APPROPRIATE FRONT PANEL INDICATIONS
SHIFT PULSE GENERATOR GENERATES ASYNCHRONOUS SLEW PULSES AT APPROXIMATELY 2 MHz
DIRECTION DATA
SHIFT DIRECTION LATCH STORES CURRENT SLEW DIRECTION
REMOTE - CARD LOCAL REMOTE LATCH SLAVED TO LATCH ON LOCAL - CARD
LOC REM STATUS
CDA STATUS INDICATIONS
EXECUTE LOGIC
SLEW AND DIRECTION COMMANDS
S W486 22 SIGNAL
H W486 4A/Ø SHIFT
5 MHz SQUARER LEVEL CONVERTER CONVERTS INPUT 5 MHz SINE WAVE INTO LOGIC SQUARE WAVE.
TAPPED DELAY LINE AND SYNCHRONIZED SELECTOR GATE SHIFTS THE PHASE OF THE 5 MHz SQUARE WAVE IN 20 NS INCREMENTS
5 MHz INPUT
DELAY SELECT
BCD OUTPUT
SYNCHRONIZED COUNTER STORES THE Ø SHIFT SETTING. MAY BE INCREMENTED UP OR DOWN BY CDA SLEW PULSES OR PRESET TO ANY BCD STATE BY 4 LINE PARALLEL INPUTS. BCD INPUT DATA IS COMPARED WITH COUNTER BCD OUTPUT DATA PRODUCING AN AGREE-DISAGREE OUTPUT
5 MHz SYNC
SHIFTED 5 MHz
Ø SHIFTED 5 MHz TO CARDS M N
EXTERNAL BCD INPUT
Ø SHIFT BCD AGREEMENT
RESET TO EXT BCD
SLEW COMMANDS
A W486 3A/DRRG
6 DECADE PROGRAMMABLE COUNTER SYNCHRONOUSLY DIVIDES 5 MHz INPUT. DECIMAL OUTPUTS ARE USED TO DETERMINE REPETITION INTERVAL
RESET COINCIDENCE GATE ANDS SELECTED DECIMAL OUTPUTS FROM PROGRAM CARD TO DETERMINE COUNTER RESET PULSE LORTO
DRRG COINCIDENCE LOGIC ANDS DRRG RESET PULSE LORTO WITH LORTO FROM ONE OTHER DRRG GENERATES COINCIDENCE PULSE AND LOSS OF COINCIDENCE ALARM LEVEL
DRRG DATA
CODE MODE PROGRAM JUMPER MASTER SECONDARY PROGRAM JUMPERS
DRRG NO. 2 RATE PROGRAM
G W486 3A/DRRG
6 DECADE PROGRAMMABLE COUNTER SYNCHRONOUSLY DIVIDES 5 MHz INPUT. DECIMAL OUTPUTS ARE USED TO DETERMINE REPETITION INTERVAL
1 MHz DECIMAL OUTPUTS
100 KHz
RESET COINCIDENCE GATE ANDS SELECTED DECIMAL OUTPUTS FROM PROGRAM CARD TO DETERMINE COUNTER RESET PULSE LORTO
LORTO
DRRG COINCIDENCE LOGIC ANDS DRRG RESET PULSE LORTO WITH LORTO FROM ONE OTHER DRRG GENERATES COINCIDENCE PULSE AND LOSS OF COINCIDENCE ALARM LEVEL
PCI
COINCIDENCE PULSE
LOST COINCIDENCE ALARM
DRRG NO. 3 RATE PROGRAM JUMPERS SELECT DRRG RESET PULSE
BLINK CARD MASTER SECONDARY PROGRAM JUMPERS
RESET TO DRRG'S
LORTO
J W486 12A/CONTROL
COINCIDENCE PULSES
LOST COINCIDENCE ALARM
MAJORITY GATES GENERATE MAJORITY LORTO AND 100 KHz
EXTERNAL AGREEMENT DETECTOR-RESET INDICATES DISAGREEMENT BETWEEN INTERNAL AND EXTERNAL TIMING DATA. DRRGS ARE RESET WHEN RESET TO EXTERNAL IS DEPRESSED. INDICATOR IS LIT WHEN RESETTING
MAJORITY DETECTOR-RESET DETECTS DISAGREEMENT BETWEEN DRRGS AND RESETS ANY TO MAJORITY FORMED BY OTHER DRRGS. DRRGS ARE RESET ARBITRARILY IF NO MAJORITY EXISTS. FRONT PANEL INDICATION OCCURS WHENEVER A MALFUNCTION EXISTS. LOST MAJORITY CHECK TIMING INDICATOR REQUIRES OPERATOR ACKNOWLEDGEMENT
ALARM
TIMING REFERENCE
INTERNAL CLOCK UPON RESET TO EXT COMMAND PROVIDES SLEW COMMANDS TO W486 4 Ø SHIFT UNTIL AGREEMENT IS REACHED
EXTERNAL TIMING REFERENCE
EXTERNAL ALARM DRIVE
S W486 22 SIGNAL
LOST LSM/TCS SIGNALS ALARMS

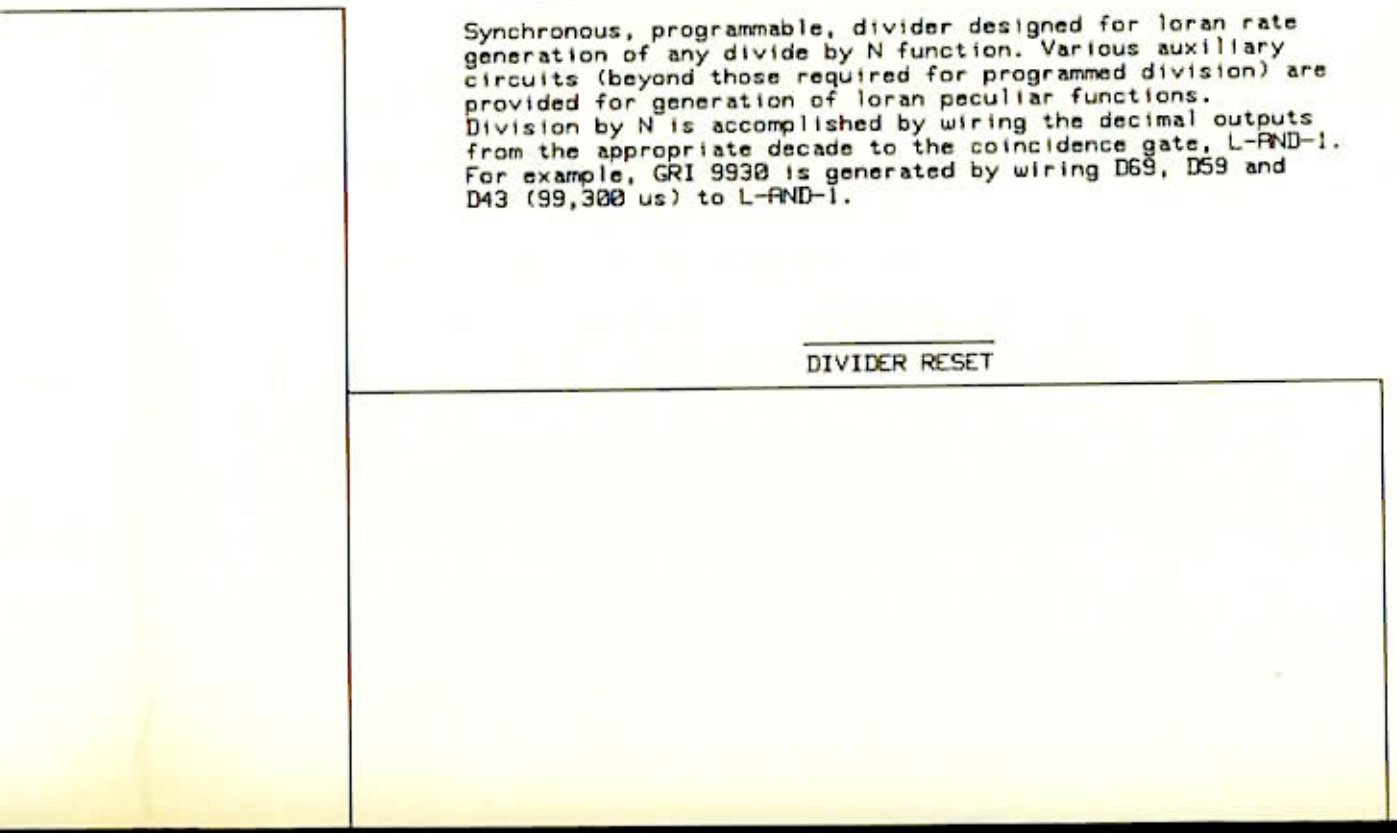


FRONT PANEL
USED TO MAKE ALL FRONT PANEL CONNECTIONS
FRONT PANEL
LOCAL REMOTE SHIFT
OPERATE
STANDBY
LOCAL REMOTE
FROM CARD
CDA MICROSECONDS
STATUS FROM TIMER SET CONTROL PANEL
COMMANDS
CLEAR
LOAD
EXECUTE
INDICATIONS
W486 3A/DRRG
6 DECADE PROGRAMMABLE COUNTER SYNCHRONOUSLY DIVIDES 5 MHz INPUT DECIMAL OUTPUTS ARE USED TO DETERMINE REPETITION INTERVAL
RESET COINCIDENCE GATE ANDS SELECTED DECIMAL OUTPUTS FROM PROGRAM CARD TO DETERMINE COUNTER RESET PULSE (LORTO)
DRRG COINCIDENCE LOGIC ANDS DRRG RESET PULSE (LORTO) WITH LORTO FROM ONE OTHER DRRG GENERATES COINCIDENCE PULSE AND LOSS OF COINCIDENCE ALARM LEVEL
PCI TO COMMS HARNESS
DRRG DATA
PROGRAM
DRRG NO 1 RATE PROGRAM


L-FF-2: SET/RESET FLIP FLOP
Independent RS flip flop can be used to generate standard frequency (100 KHz, 10 KHz) from C-CTR-1. Set and Reset inputs are connected to Dij and Di(j+5) to generate symmetric standard frequency square waveform.
1 14 SET
1 6 RESET
TP-2, PURPLE
16
Q OUTPUT
10
L-FF-3: SET/RESET FLIP FLOP
RS flip flop identical to L-FF-2.
1 10 SET
1 8 RESET
TP-1, GRAY
12
Q OUTPUT
10
5
TP-3, GREEN
DRRG x DRRG y LOSS
20
10

DIGITAL REPETITION RATE GENERATOR (DRRG)

Synchronous, programmable, divider designed for loran rate generation of any divide by N function. Various auxiliary circuits (beyond those required for programmed division) are provided for generation of loran peculiar functions. Division by N is accomplished by wiring the decimal outputs from the appropriate decade to the coincidence gate, L-AND-1. For example, GRI 9930 is generated by wiring D69, D59 and D43 (99,300 us) to L-AND-1.



OCK
RM

82 5
COUNT ENABLE OUTPUT (CEO)

D2 PRESET 66 1

64 62 1

DIVIDER CONTROL (DC)

1 36

10 26

TP-5, YELLOW
ø CODE INTERVAL

ø RESET

C-COL-1: COINCIDENCE LOGIC

Monitors timing agreement between this and one other DRRG module. LORTO pulses are logically ANDed. If in coincidence, a signal is sent to the control module (J card). If not, a signal is sent to Majority Detector and Reset Section on the Control module (J card). Also defines PCI A and B.

L-FF-1: COMPLEMENTING FLIP-FLOP

Divides reset triggers by two to define phase code interval A and B in Loran-C applications. External asynchronous reset is provided.

22 DRRG x DRRG y

TP-4, BLUE
DRRG x DRRG y

1

78 CHECK INTERVAL

80 CHECK LORTO

18 DRRG ø

L-AND-3: COINCIDENCE GATE

AND's L-AND-1 with three external inputs. Normally used to generate TRUE coincidence pulse between this DRRG and another DRRG in Loran applications.
For Loran C, local and remote Phase Code are connected to the noninverting inputs. Output is TRUE pulse marking coincidence of DRRG counter reset pulses. Pulse occurs only if DRRG's synchronized.

L-MMV-1: RETRIGGERABLE M

Output is FALSE when L-AND recurring output pulse. Outpu TRUE approximately 3 seconds L-AND-3 output ceases. Used a loss detector on Loran applic indicate local and remote DRR not synchronized.

38 R0 RATE SET

40 R1 RATE SET

54 R3 RATE SET

42 R2 RATE SET

L-AND-1: COINCIDENCE GATE

AND gate output is TRUE transition which occurs approximately 60 ns after clock transition defining programmed count. Output goes FALSE one clock period after TRUE transition. All unused inputs must be grounded.

TP-6, ORANGE
DRRG LORTO

L-AND-2: COINCIDENCE GATE

AND gate provides FALSE scope trigger at test point. TRIGGER SET (T1) input usually connected to least significant decade, one count earlier than RATE SET (R1) input to provide early scope triggers.

56
T1 TRIG. SET

TP-7, RED
SCOPE TRIGGER

10 LORTO OUTPUT 24

L-OR-1: RESET OR GATE

OR's L-AND-1 output pulse with external FALSE reset pulse. To obtain unambiguous reset of C-CTR-1, external reset pulse must be wider than 20 ns and one negative transition of C-CTR-1 clock.

EXTERNAL RESET 60

1

ure 7.2. W0486-3A/DRRG Block Diagram
/7.6

C-CTR-1: SYNCHRONOUS, SIX-DECADE DIVIDER

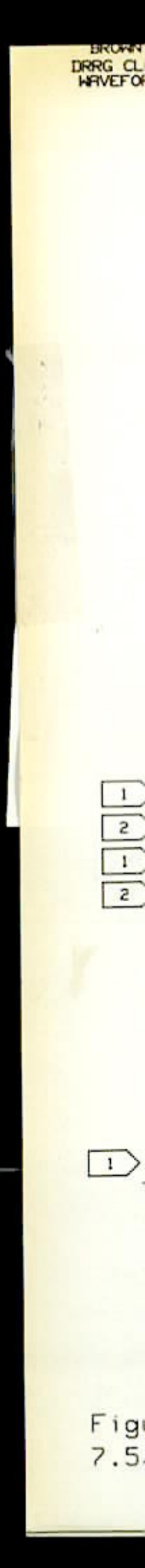
Each decade operates in BCD format and is continously decoded into its decimal state. Decoded decimal outputs are available at terminals labeled Dij where i represents the decade number and j the jth decimal state of the decade. All decades are clocked synchronously, there is approximately 50 ns delay from negative input clock transition to change of state of Dij output.

C-CTR-1 accepts either 5 MHz or 1 Mhz input. When using 5 Mhz, the DIVIDER SELECT (D2P0) input is tied to Vcc, and the first decade is normally programmed to divide by 5 by connecting D14 to D2 COUNT ENABLE (D2CE). The unused D2CE should be tied to Vcc or the used D2CE. This passes a carry pulse to D2 every five input clock transitions. This technique insures synchronous operation of all six decades.

Programmable division (i.e. generation of a Loran Repetition Rate) is accomplished by wiring the desired reset count from decoded outputs of C-CTR-1 to L-AND-1. When this count is reached, C-CTR-1 is set to a parallel data mode (counting is inhibited) and the next clock transition loads 1 into the Least Significant Decade and 0 in all other decades. This value disables L-AND-1 (its inputs no longer equal the wired in count) which then returns C-CTR-1 to synchronous count mode. This initiates a new count sequence which will end when C-CTR-1 again reaches the programmed count. The reset pulse from L-OR-1 which causes this parallel load operation is equal to the clock period and is delayed approximately 75 ns from the negative clock transition which defines the programmed count wired to L-AND-1.

For 1 MHz operation, one or both D2CE inputs are grounded, and D2P0 input is grounded. This removes the first divider from the counting chain and causes a one to be loaded into the least significant bit of divider D2 during reset.

INPUT
2
74



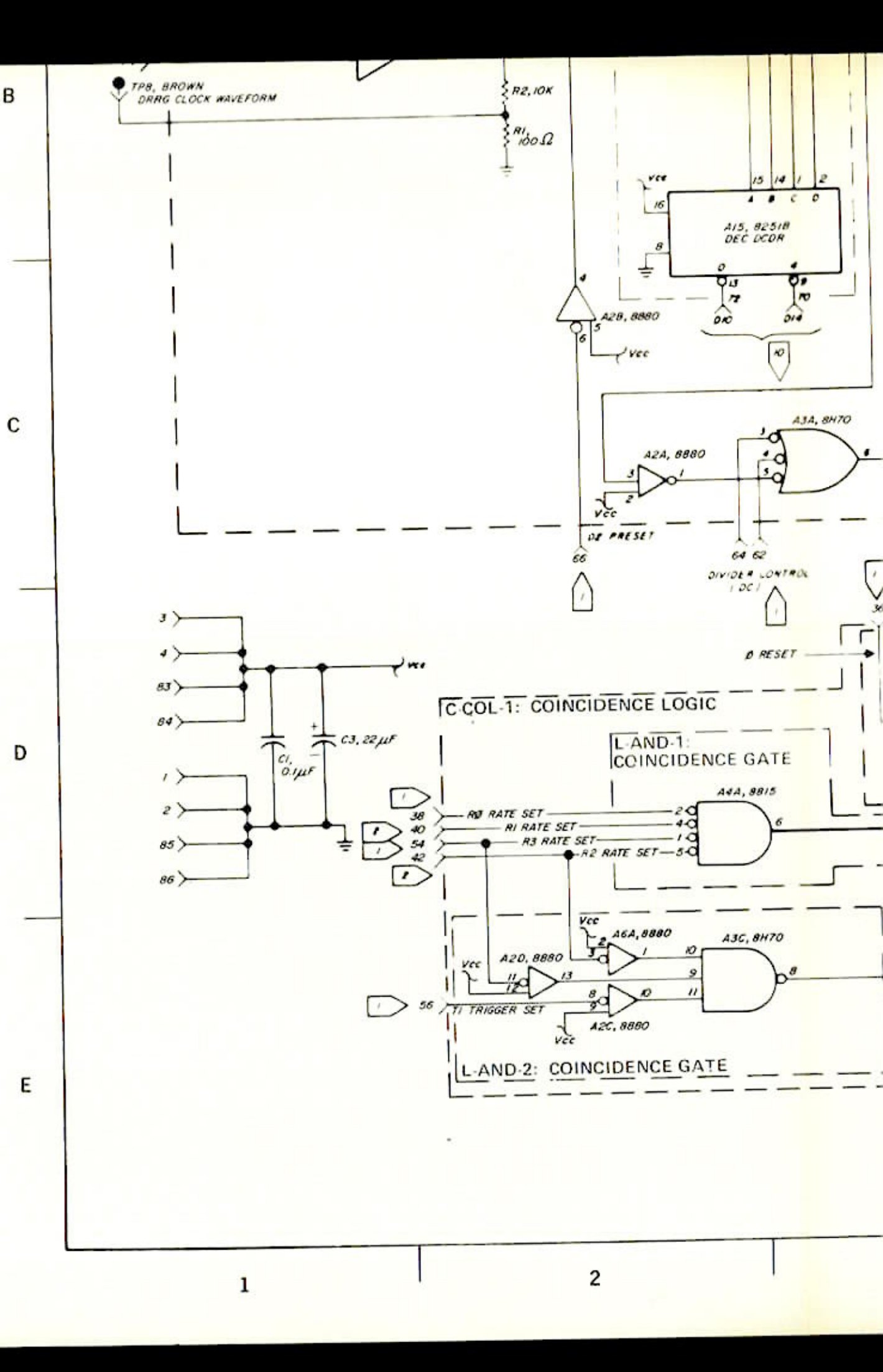
Figu
7.5

CLOCK

TP-8,

PART LOCATION INDEX

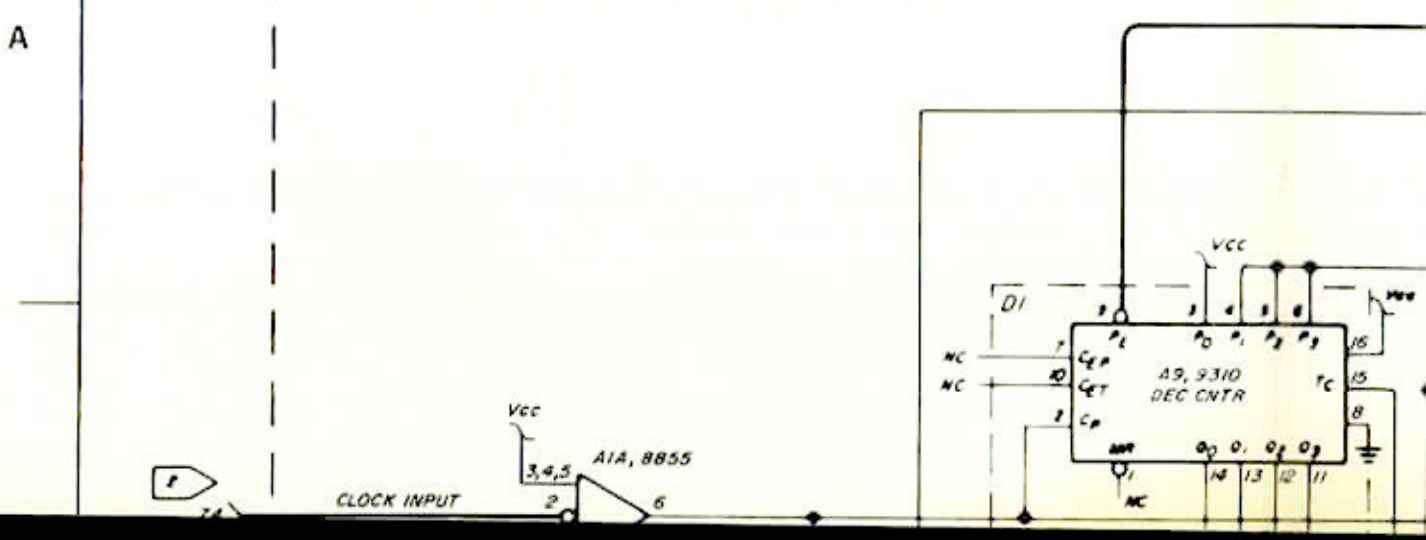
REF. DESIG.	LOCATION	REF. DESIG.	LOCATION
A1A	1B	A16	3B
A1B	7A	A17	4B
A2A	2C	A18	5B
A2B	2C	A19	6B
A2C	2E	A20	6B
A2D	2E		
A3A	3C	C1	1D
A3B	4E	C2	5D
A3C	2E	C3	1D
A4A	2D		
A4B	4D	E1	NOT SHOWN
A5A	3D	E2	NOT SHOWN
A5B	NOT USED	E3	NOT SHOWN
A6A	2E		
A6B	4D	Q1	6D
A6C	5D		
A6D	4D	R1	2B
A7	5D	R2	2B
A8A	7C	R3	5D
A8B	7D	R4	6D
A8C	7E		
A8D	7D	TP1	7D
A9	2B	TP2	7C
A10	3B	TP3	6D
A11	4B	TP4	5D
A12	5B	TP5	3D
A13	6B	TP6	4D
A14	6B	TP7	3E
A15	2B	TP8	1B
		TP9	7B



1 2

A

C-CTR-1: SYNCHRONOUS, SIX-DECADE DIVIDER



A16, 8251B DEC DCDR

A17, 8251B DEC DCDR

A18, 8251B DEC DCDR

A19, 8251B DEC DCDR

A20, 8251B DEC DCDR

Pin No's D00 D29 D30 D39 D40 D49 D50 D59 D60 D69

82 COUNT ENABLE OUTPUT (CEO)

TP5, YELLOW @ CODE INTERVAL

L-FF-1: COMPLEMENTING FLIP-FLOP

A5A, 8824 JK

TP4, BLUE DRRG X DRRG Y

L-AND-3: COINCIDENCE GATE

A4B, 8815

A6C, 8880

L-MMV-1: RETRIGGERABLE MONOSTABLE

A7, 9601, RSS

R3, 470K

R4, 10K

Q1, 2N3643

C2, 22pF

TP3, GREEN DRRG X DRRG Y LOSS

78 CHECK INTERVAL

80 CHECK LORTO

18 DRRG Ø

A6D, 8880

A6B, 8880

TP7, RED SCOPE TRIGGER

LORTO OUTPUT

60 EXTERNAL RESET

TP6, ORANGE DRRG LORTO

L-OR-1: RESET OR GATE

A3B, 8H70

L-FF-2: SET/RESET FLIP-FLOP

A8A, 8880

SET

RESET

A8D, 8880

TP2, PURPLE

16 Q OUTPUT

L-FF-3: SET/RESET FLIP-FLOP

A8B, 8880

SET

RESET

A8C, 8880

TP1, GRAY

12 Q OUTPUT

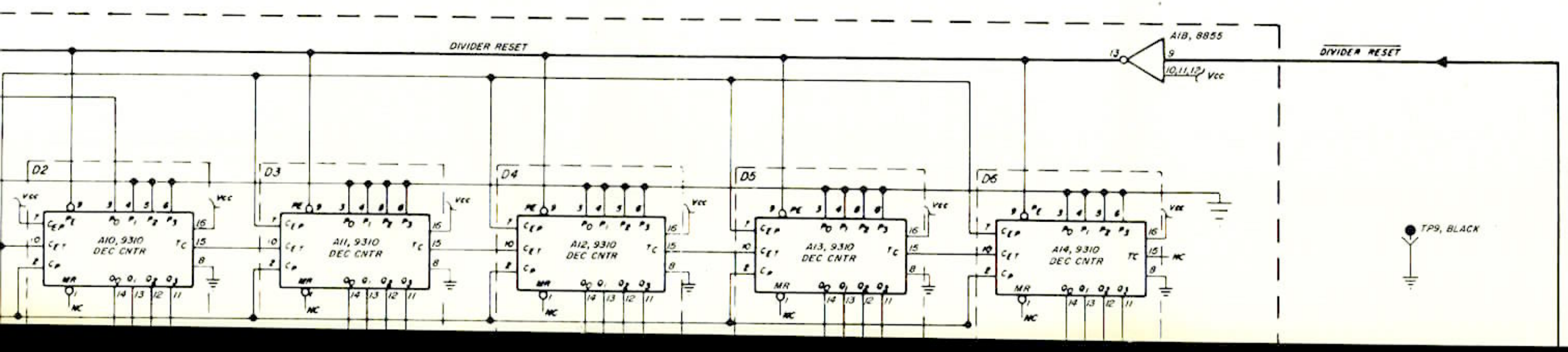
NOTE: UNUSED INPUTS OF ALL 8880's and 8855's ARE TIED TO Vcc.

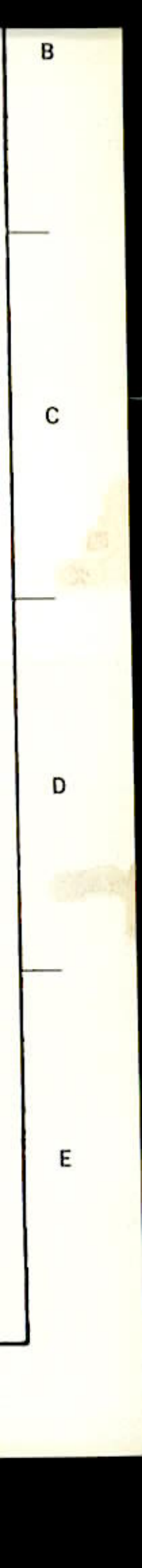
NC = NO CONNECTION

Figure 7.3. W0486-3A/DRRG Schematic Diagram

3 4 5 6 7 8

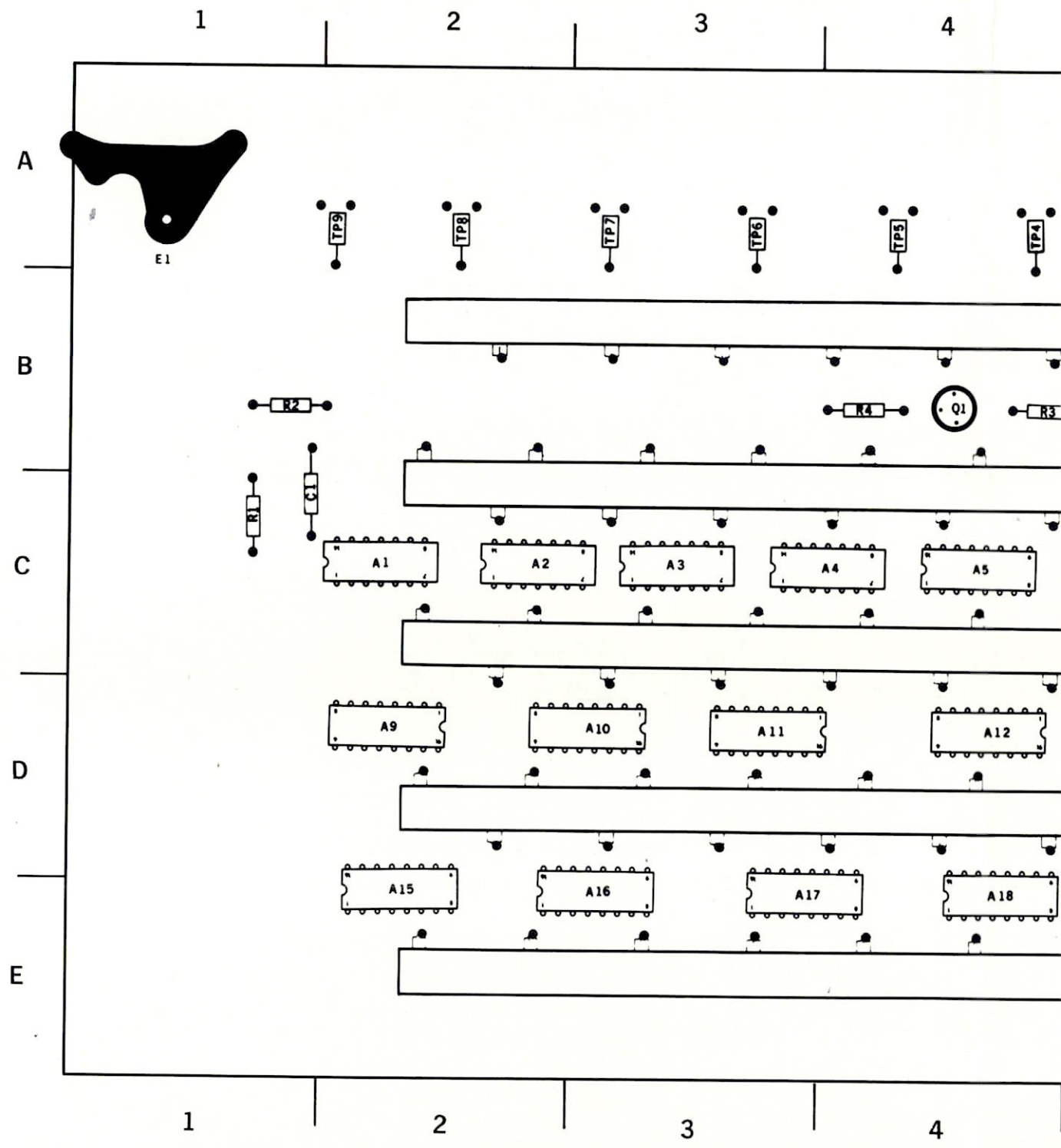
3 4 5 6 7 8


DIVIDER RESET
A1B, 8855
13
9
10,11,12
Vcc
DIVIDER RESET
D2
D3
D4
D5
D6
A10, 9310
DEC CNTR
A11, 9310
DEC CNTR
A12, 9310
DEC CNTR
A13, 9310
DEC CNTR
A14, 9310
DEC CNTR
Vcc
MR
TC
NC
TP9, BLACK


B
C
D
E


A

PART LOCATION INDEX	
REF. DESIG.	LOCATION
A1	2C
A2	2C
A3	3C
A4	4C
A5	4C
A6	5C
A7	5C
A8	6C
A9	2D
A10	3D
A11	3D
A12	4D
A13	5D
A14	6D
A15	2E
A16	3E
A17	3E
A18	4E
A19	5E
A20	6E
C1	1C
C2	5B
C3	7D
E1	1A
E2	7A
E3	7C
Q1	4B
R1	1C
R2	1B
R3	4B
R4	4B
TP1	6A
TP2	6A
TP3	5A
TP4	4A
TP5	4A
TP6	3A
TP7	3A
TP8	2A
TP9	2A



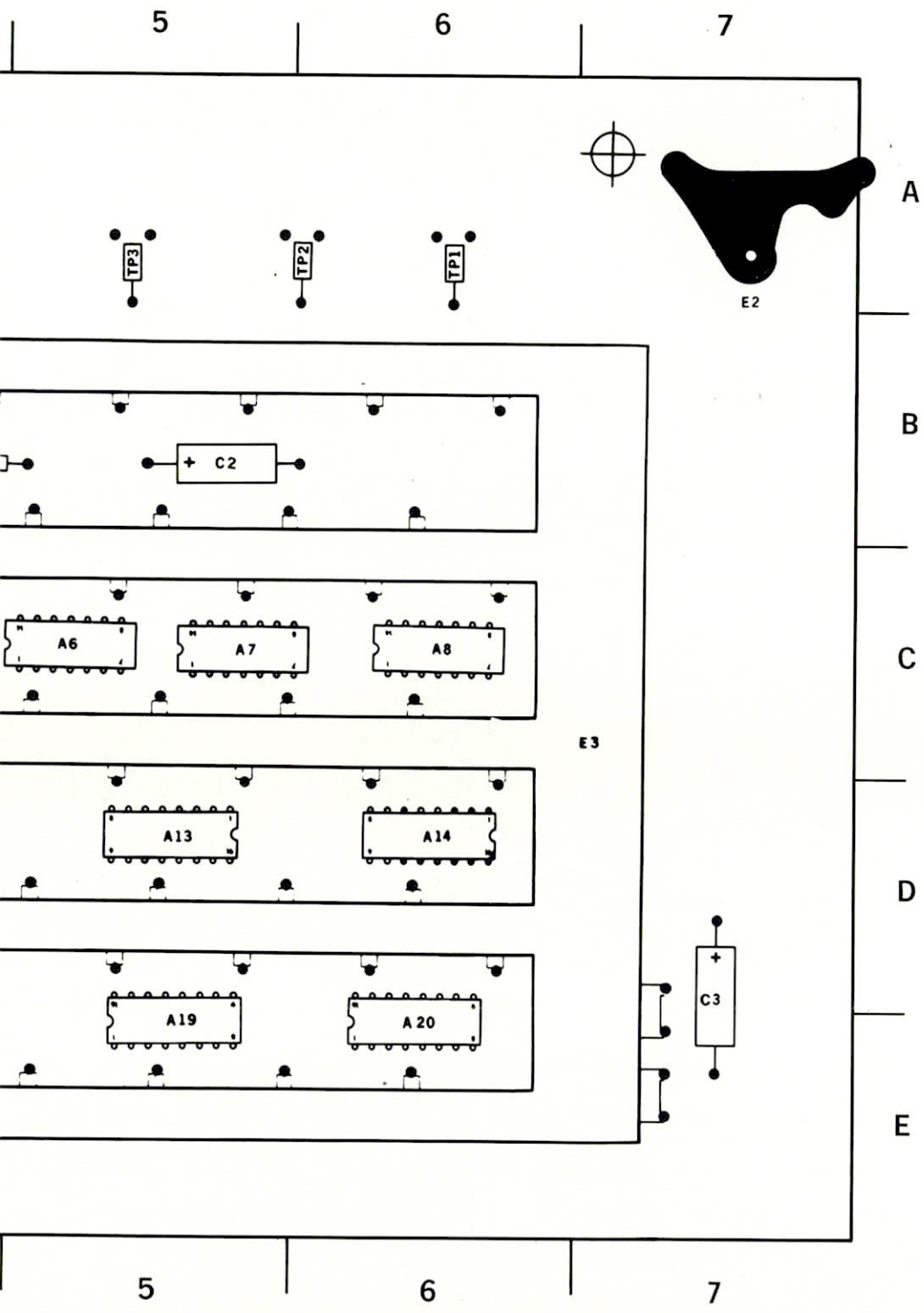


Figure 7.4. W0486-3A/DRRG Parts Locator

) 5 MHz
/ line N-DL-1.

Inverts and amplifies Ø-shifted 5 MHz from L-SEL-1 sufficiently to drive multiple DRRG'S through twisted-pair interconnections.

BUFFERED 5 MHz OUTPUT
16 → 30

Ø-SHIFTED 5 MHz OUTPUT
80 → 6

or to detect loss of
ed 5 MHz to clock

L-BUF-2: SYNCH BUFFER

Provides inverted output to C-DIV-1 and synch, waveform to L-SYN-1 and Q-RST-1 from Ø-shifted 5 MHz output of L-SEL-1.

30 → 32 → 34 → 36 → 38 → 10

L-BUF-2: 5 MHz OUTPUT BUFFER

Provides buffered output of Ø shifted 5 MHz opposite in phase to that provided by C-DPS-1 (L-BUF-3).

BUFFERED 5 MHz OUTPUT
14 → 30

GATED 5 MHz OUTPUT
13 → 10

GATED 1 MHz OUTPUT
11 → 10

GATED Ø2 100 KHz OUTPUT
5 → 10

Ø1 100 KHz OUTPUT
7 → 8

100 KHz, 1 us STROBE OUTPUT
8 → 9

100 kHz, 100 ns STROBE OUTPUT
6 → 10

Ø KHz STROBE GATING

puts of L-DIV-1 and L-DIV-2
wide and 100 ns wide FALSE
KHz rate.

L-GAT-2: OUTPUT GATING

NAND's 100 KHz Ø1 and 1 MHz pulse with external inputs to provide gated outputs.

33

HIFT DIRECTION

OMMAND INPUTS

41

SD)

39

1

37

1

40

Ø-SHIFTED 5 MHz
COUNTER SYNCH.
INPUT FROM
PIN 16

31

2

25

2

23

21

19

22

1

24

26

28

L-SYN-2: COUNTER SYNCHRONIZER

Uses interlocked "D" flip-flops and an "RS" latch to synchronize any input to L-CTR-1 with the 5 MHz output. This ensures that set-up/release times of L-CTR-1 and L-SYN-1 are met under all conditions of operation.

L-SYN-1: Ø-SELECT SYNCH

Uses 10 "D" flip-flops to synchronize any change in Ø-shift as selected by the state of L-CTR-1 with the output 5 MHz to ensure that no spurious transients occur during the switching process.

L-SEL-1: PHASE SELECT GATING

Selects the output (phase-shifted
from one tap of a 10-tap 200 ns dela

Q-RST-1: SYNCH RESET

Uses voltage doubler and transist
shifted 5 MHz and substitute unshift
(L-SYN-1).

L-CTR-1: DECADE COUNTER

Stores the decimal number corresponding to the selected phase of N-DL-1. L-CTR-1 has up/down count and parallel BCD data entry capabilities accessible through L-SYN-2 which may be used to change the stored decimal number and change the selected phase. L-CTR-1 BCD outputs buffered by A28 for use external to board.

(L-CMP-1): DIGITAL COMPARATOR

Compares the 4-line BCD output of L-CTR-1 with
externally supplied 4-line BCD (positive logic).
L-CMP-1 output is TRUE for agreement, FALSE
otherwise.

L-CMP-1 is intended for comparison between L-CTR-1 of two W-486 Ø-SHIFT modules when redundancy is employed at this level.

When the COMPARATOR INHIBIT input is FALSE, COMPARATOR OUTPUT is TRUE regardless of the BCD inputs.

C-DIV-1: FREQUENCY DIVIDER

Synchronously divides and gates the 5 MHz output of C-DPS-1 to produce 1 MHz and 100 KHz waveforms.

18

1

15

17

9

2

12

L-BUF-1: 5 MHz DIVIDER BUFFER

Buffers 5 MHz input to L-DIV-1 and L-DIV-2.

L-DIV-1: QUINARY DIVIDER

Synchronously divides 5 MHz to produce 200 ns pulses at 1 MHz rate.

L-DIV-2: BIQUINARY DIVIDER

Divides 1 MHz output of L-DIV-1 to produce 100 KHz square waves and 200 KHz gating waveform. Division is synchronous with 5 MHz from C-DPS-1.

L-GAT-1: 10

Combines out
to provide lus
strobes at 100

gure 7.5. W0486-4A/Ø-SHIFT Block Diagram



SH

CO

(S

[

[

Fig

7.

5 MHz
line N-DL-1.

or to detect loss of
ed 5 MHz to clock

Inverts and amplifies Ø-shifted 5 MHz from L-SEL-1 sufficiently to drive multiple DRRG'S through twisted-pair interconnections.

BUFFERED 5 MHz OUTPUT
16 → 30

Ø-SHIFTED 5 MHz OUTPUT
80 → 6

L-BUF-2: SYNCH BUFFER

Provides inverted output to C-DIV-1 and synch, waveform to L-SYN-1 and O-RST-1 from Ø-shifted 5 MHz output of L-SEL-1.

30 → 32 → 34 → 36 → 38 → 10

L-BUF-2: 5 MHz OUTPUT BUFFER

Provides buffered output of Ø shifted 5 MHz opposite in phase to that provided by C-DPS-1 (L-BUF-3).

BUFFERED 5 MHz OUTPUT
14 → 30

GATED 5 MHz OUTPUT
13 → 10

GATED 1 MHz OUTPUT
11 → 10

GATED Ø2 100 KHz OUTPUT
5 → 10

Ø1 100 KHz OUTPUT
7 → 8

100 KHz, 1 us STROBE OUTPUT
8 → 9

100 kHz, 100 ns STROBE OUTPUT
6 → 10

Ø KHz STROBE GATING

puts of L-DIV-1 and L-DIV-2
wide and 100 ns wide FALSE
KHz rate.

L-GAT-2: OUTPUT GATING

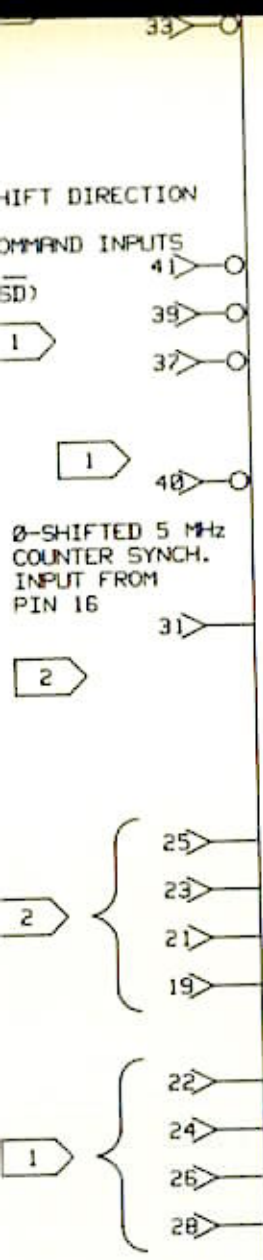
NAND's 100 KHz Ø1 and 1 MHz pulse with external inputs to provide gated outputs.

→ 81 [9]

→ 79 [10]

hm impedance delay line
ate 10 phases of the
se is ultimately
L-SEL-1. N-DL-1
ination and a 24 ohm

L-BUF-3: 5 MHz OUTPUT BUFFER



L-SYN-2: COUNTER SYNCHRONIZER

Uses interlocked "D" flip-flops and an "RS" latch to synchronize any input to L-CTR-1 with the 5 MHz output. This ensures that set-up/release times of L-CTR-1 and L-SYN-1 are met under all conditions of operation.

L-SYN-1: Ø-SELECT SYNCH

Uses 10 "D" flip-flops to synchronize any change in Ø-shift as selected by the state of L-CTR-1 with the output 5 MHz to ensure that no spurious transients occur during the switching process.

L-SEL-1: PHASE SELECT GATING

Selects the output (phase-shifted from one tap of a 10-tap 200 ns dela

Q-RST-1: SYNCH RESET

Uses voltage doubler and transist shifted 5 MHz and substitute unshift (L-SYN-1).

L-CTR-1: DECADE COUNTER

Stores the decimal number corresponding to the selected phase of N-DL-1. L-CTR-1 has up/down count and parallel BCD data entry capabilities accessible through L-SYN-2 which may be used to change the stored decimal number and change the selected phase. L-CTR-1 BCD outputs buffered by A28 for use external to board.

(L-CMP-1): DIGITAL COMPARATOR

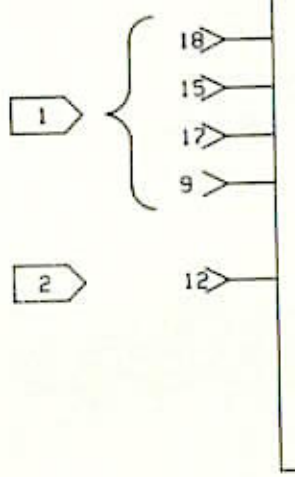
Compares the 4-line BCD output of L-CTR-1 with externally supplied 4-line BCD (positive logic). L-CMP-1 output is TRUE for agreement, FALSE otherwise.

L-CMP-1 is intended for comparison between L-CTR-1 of two W-486 Ø-SHIFT modules when redundancy is employed at this level.

When the COMPARATOR INHIBIT input is FALSE, COMPARATOR OUTPUT is TRUE regardless of the BCD inputs.

C-DIV-1: FREQUENCY DIVIDER

Synchronously divides and gates the 5 MHz output of C-DPS-1 to produce 1 MHz and 100 KHz waveforms.



L-BUF-1: 5 MHz DIVIDER BUFFER

Buffers 5 MHz input to L-DIV-1 and L-DIV-2.

L-DIV-1: QUINARY DIVIDER

Synchronously divides 5 MHz to produce 200 ns pulses at 1 MHz rate.

L-DIV-2: BIQUINARY DIVIDER

Divides 1 MHz output of L-DIV-1 to produce 100 KHz square waves and 200 KHz gating waveform. Division is synchronous with 5 MHz from C-DPS-1.

L-GAT-1: 10

Combines ou to provide lus strobes at 100

gure 7.5. W0486-4A/Ø-SHIFT Block Diagram

C-SQA-1: 5MHz SQUARER-LEVEL CONVERTER

Converts low-level (1 Volt p-p into 1000 ohm load) 5 MHz sine wave into fast risetime 5 MHz square wave compatible with digital logic elements. Input series resistor and diode limiter provide input overload protection and ensure 1000 ohm or greater input impedance. Normal (Ø1) and inverted (Ø2) outputs are provided.

77

C-DPS-1: DIGITAL PHASE SHIFTER

Provides digitally controlled phase shift of rectangular 5 MHz input waveform. Phase shift is variable in discrete steps of 20 ns. Normal and high driving capability inverted outputs are available.

82

Control of phase shift is provided by three SHIFT PULSE (SP) and three SHIFT DIRECTION (SD) inputs. The trailing edge of an asynchronous FALSE pulse on any SP input will cause one 20 ns shift. The shift will be to the right (later) in time when any SD input is FALSE, otherwise the shift will be to the left (earlier) in time.

The phase shift is implemented by selecting the output (phase shifted) 5MHz from one tap of a 10-tap 200 ns delay line,,N-DL-1. This selection is accomplished by L-SEL-1 and controlled by the state of decimal counter L-CTR-1.

SD and SP inputs control the state of L-CTR-1. L-SYN-1 synchronizes any change in L-CTR-1 state with the shifted 5 MHz output. This ensures that no spurious output will occur during change in phase shift.

2

HIFT PULSE

NPUTS ($\overline{SP}$)

29

35

2

L-BUF-1: DELAY LINE BUFFER

Inverts and amplifies input 5 MHz square wave to drive 50 ohm impedance of N-DL-1.

N-DL-1: TAPPED DELAY

Uses a standard 200 ns, 50 oh
with taps at each 20 ns to gener
input 5 MHz square wave. One pha
selected as the 5 MHz output by
includes a 51 ohm resistive term
back-matching resistor.

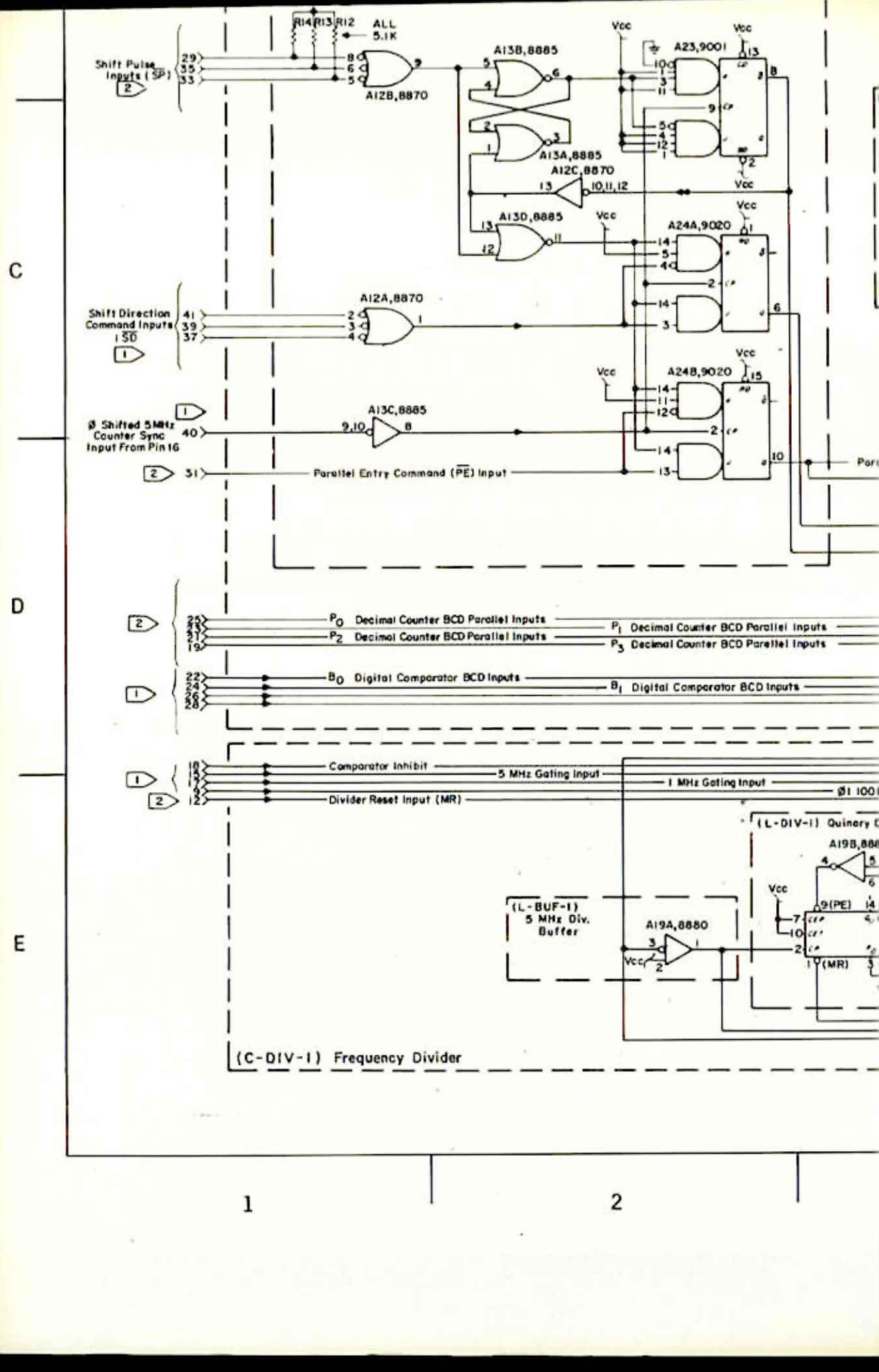


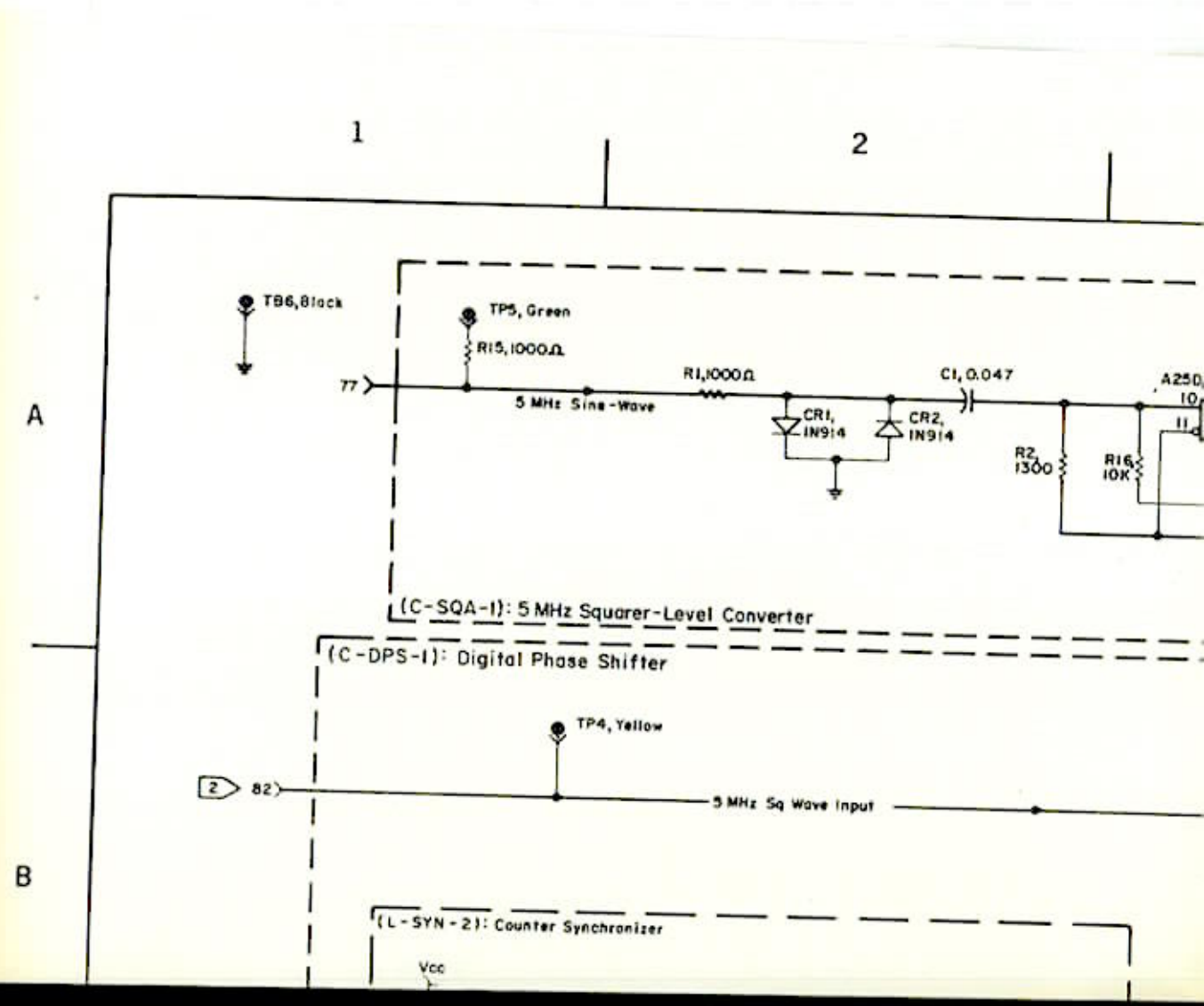
NI

HS

PART LOCATION INDEX

REF.DESIG.	LOCATION	REF.DESIG.	LOCATION	REF.DESIG.	LOCATION
A1A	3B	A21	4E	CR4	6C
A1B	3B	A22A	7E		
A2A	6C	A22B	7E	E1	NOT SHOWN
A2B	6C	A22C	7E	E2	NOT SHOWN
A3	6C	A23	2C	E3	NOT SHOWN
A4	6C	A24A	2C	E4	NOT SHOWN
A5A	5C	A24B	2C		
A5B	5C	A25A	3A	Q1	4A
A6A	4C	A25B	3A	Q2	6C
A6B	5C	A25C	4A		
A7A	4C	A25D	3A	R1	2A
A7B	4C	A26A	4A	R2	2A
A8A	4C	A26B	5A	R3	3A
A8B	4C	A27A	7D	R4	3A
A9A	3C	A27B	NOT USED	R5	4A
A9B	3C	A27C	NOT USED	R6	4A
A10	4C	A27D	8C	R7	3A
A11	4D	A28A	6D	R8	6B
A12A	1C	A28B	6D	R9	7B
A12B	1B	A28C	6D	R10	6C
A12C	2C	A28D	6D	R11	6C
A13A	2C			R12	1B
A13B	2B	C1	2A	R13	1B
A13C	1C	C2	3A	R14	1B
A13D	2C	C3	3A	R15	1A
A14	5D	C4	6C	R16	3A
A15A	NOT USED	C5	6C		
A15B	6D	C6	8A	TP1	8E
A15C	6D	C7	8A	TP2	8E
A16A	7C	C8	8A	TP3	8C
A16B	8D	C9	8A	TP4	1B
A16C	7D	C10	8A	TP5	1A
A16D	7D	C11	8B	TP6	1A
A17A	7C	C12	8B		
A17B	7D	C13	8B	Z1	6B
A18A	7E	C14	8B		
A18B	7E	C15	8B		
A18C	7C	C16	8B		
A19A	2E	C17	8B		
A19B	3E				
A19C	4E	CR1	2A		
A19D	4E	CR2	2A		
A20	3E	CR3	6C		




1
2
A
B
TB6, Black
TP5, Green
R15, 1000Ω
77
5 MHz Sine-Wave
R1, 1000Ω
CR1, IN914
CR2, IN914
C1, 0.047
R2, 1300
R16, 10K
(C-SQA-1): 5 MHz Squarer-Level Converter
(C-DPS-1): Digital Phase Shifter
TP4, Yellow
2
82
5 MHz Sq Wave Input
(L-SYN-2): Counter Synchronizer
Vcc

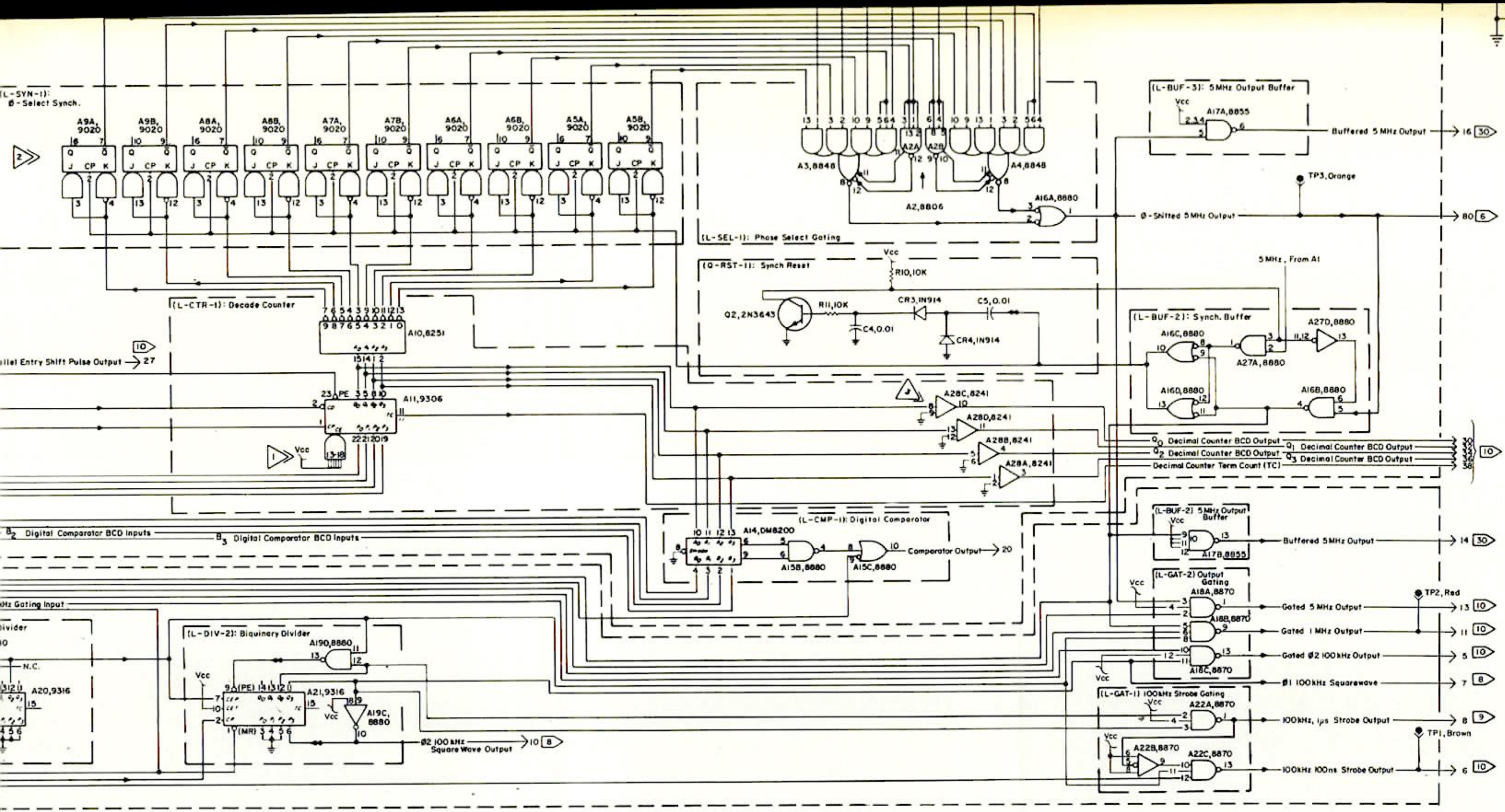
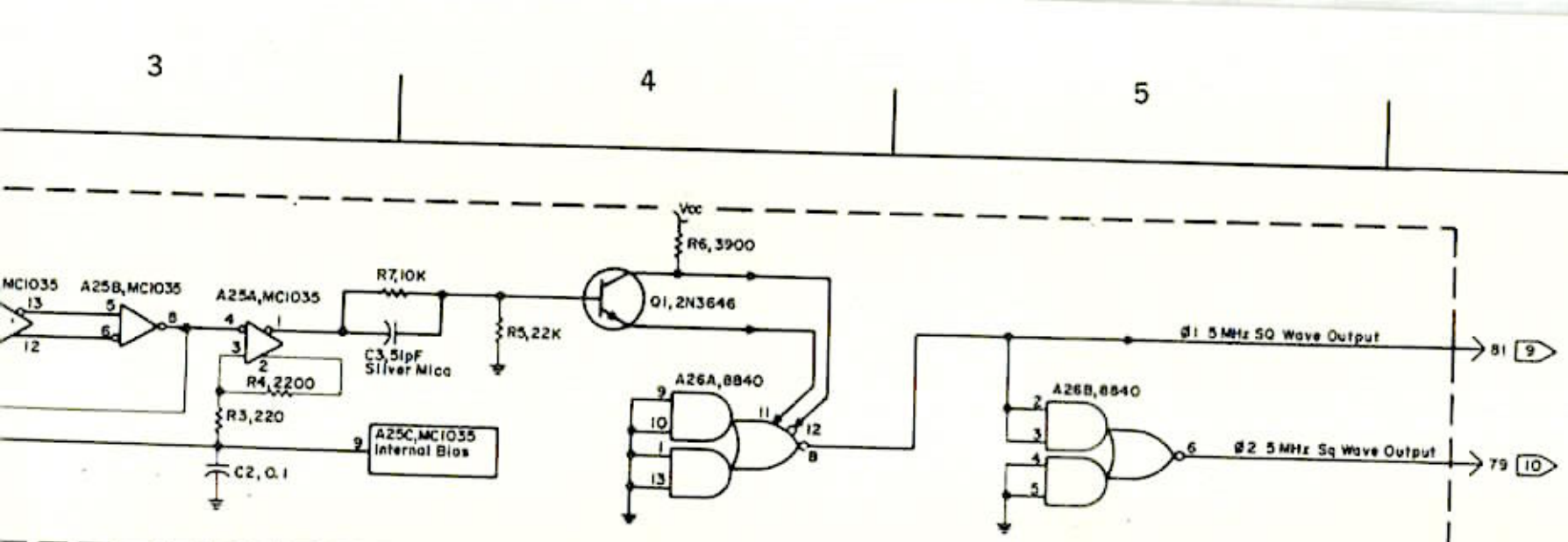


Figure 7.6. W0486-4A/Ø-SHIFT Schematic Dia

3 4 5 6 7 8

3 4 5 6 7 8

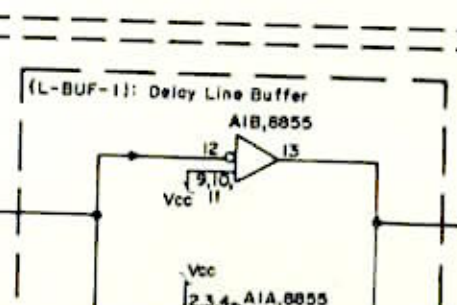


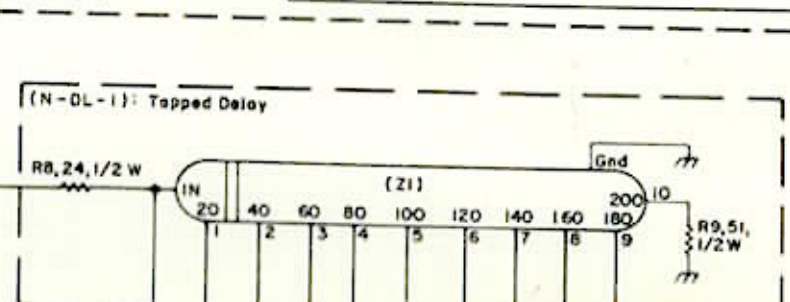
Power Connections – All IC's		
Package	Vcc	Ground
14-Pin	Pin 14	Pin 7
16-Pin	Pin 16	Pin 8
24-Pin	Pin 24	Pin 12

Notes:
1. All Unused Nand Gate Inputs Are Connected To Vcc. All Unused Nor Gate Inputs Are Connected To Ground.
2. All Resistors Are 1/4 Watt, 5% Carbon Composition Unless Noted. All Values In Ohms Unless Noted.
3. All Whole Number Capacitor Values Are Picofarads. All Decimal Values Are Microfarads Unless Noted.

Flag Notes
1. Count Enable Pins 13-18 Tied To Vcc
2. Pins 1, 5, 11, 14, 15, 16 Tied To Vcc Pin 8 To Ground
3. Exclusive or Gates With One Input Grounded Used For Non-Inverting Buffer Pins 2, 5, 7, 9, 12 Grounded

3 +5V
4 +5V
83 +5V
84 +5V
1
2
85
86



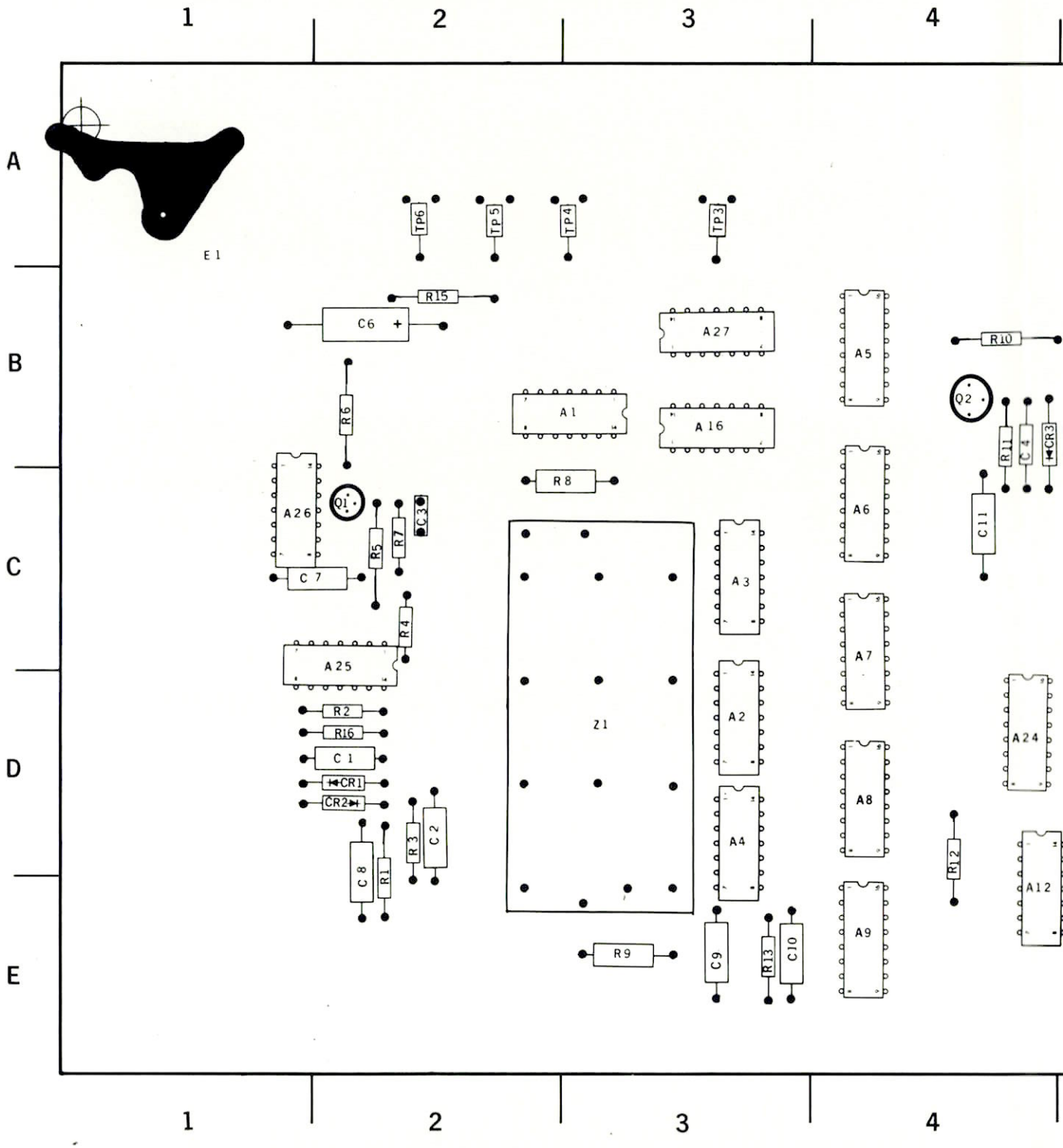




gram
7.14

Vcc
C6, 22μF
C7, 0.1μF
C8, 0.1μF
C9, 0.1μF
C10, 0.1μF
C11, 0.1μF
C12, 0.1μF
C13, 0.1μF
C14, 0.1μF
C15, 0.1μF
C16,
A
B

PART LOCATION INDEX			
REF. DESIG.	LOCATION	REF. DESIG.	LOCATION
A1	3B	C15	6B
A2	3D	C16	7C
A3	3C	C17	7D
A4	3D		
A5	4B	CR1	2D
A6	4C	CR2	2D
A7	4C	CR3	4B
A8	4D	CR4	5B
A9	4E		
A10	5C	E1	A1
A11	5C	E2	A7
A12	4E	E3	NOT SHOWN
A13	5E	E4	NOT SHOWN
A14	6D		
A15	6C	Q1	2C
A16	3B	Q2	4B
A17	5B		
A18	5B	R1	2E
A19	6B	R2	2D
A20	6B	R3	2D
A21	6B	R4	2C
A22	7C	R5	2C
A23	5D	R6	2B
A24	4D	R7	2C
A25	2C	R8	3C
A26	1C	R9	3E
A27	3B	R10	4B
A28	5D	R11	4B
		R12	4D
C1	2D	R13	3E
C2	2D	R14	5E
C3	2C	R15	2B
C4	4B	R16	2D
C5	5B		
C6	2B	TP1	6A
C7	2C	TP2	5A
C8	2D	TP3	3A
C9	3E	TP4	3A
C10	3E	TP5	2A
C11	4C	TP6	2A
C12	5B		
C13	5D	Z1	3D
C14	6C		



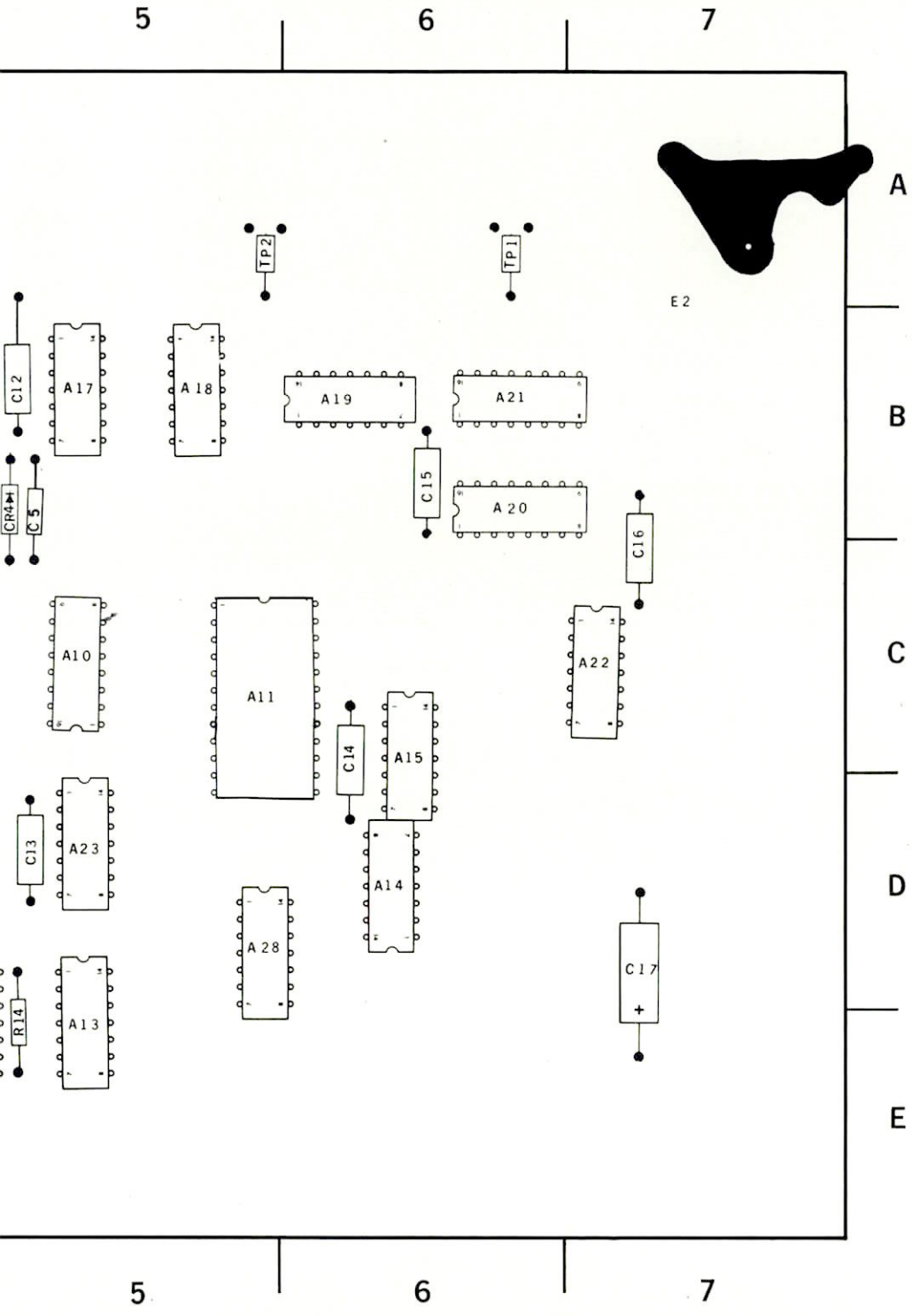
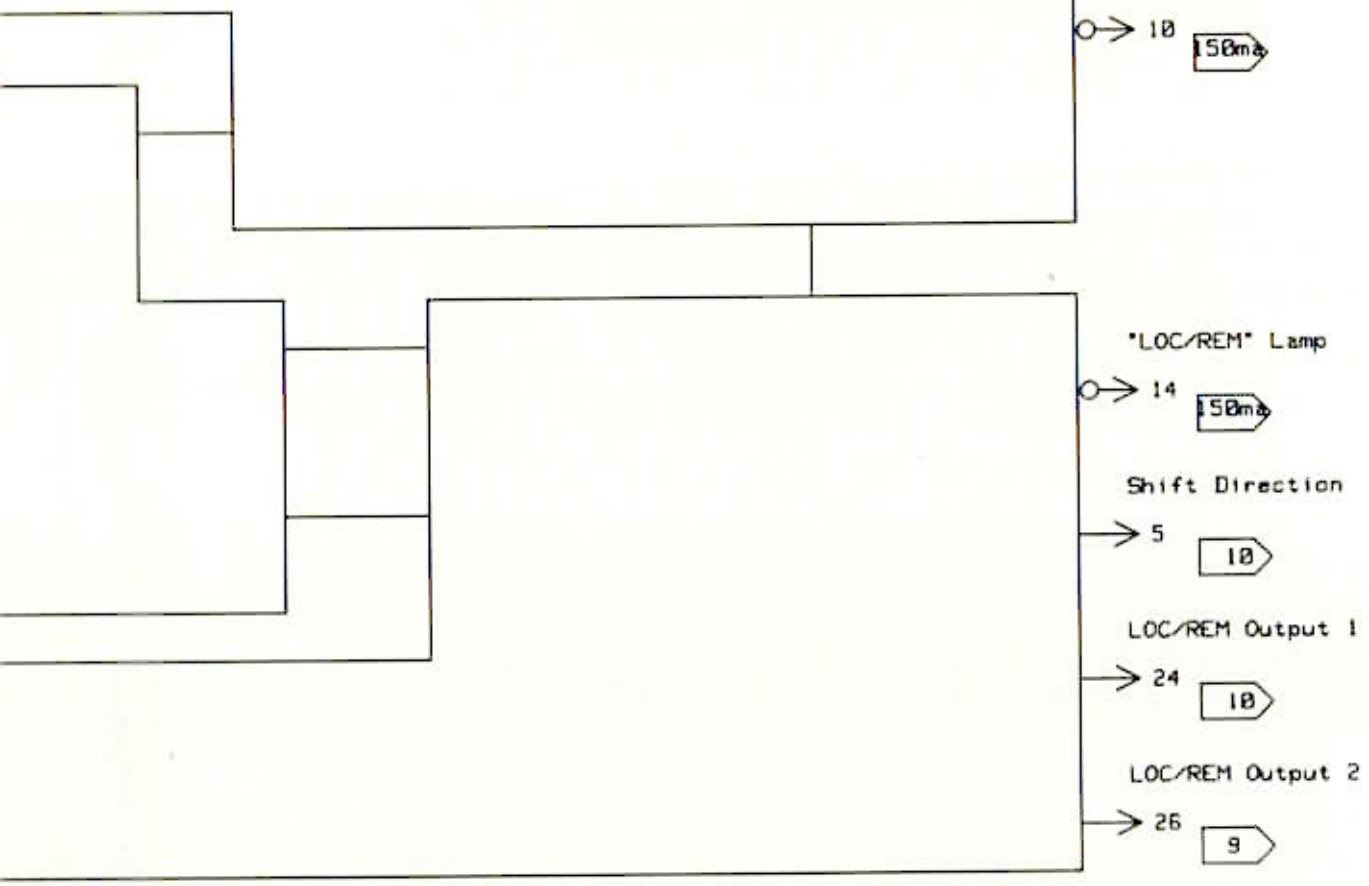


Figure 7.7. W0486-4A/Ø SHIFT Parts Locator


6
9
"LOAD" Logic
38
1
"EXECUTE" Logic
17
9
TP-1, YELLOW
34
29
Shift Pulse To Ø-Shifter
"CLEAR" Lamp
12
150mA
"LOAD" Lamp
8
150mA
"EXECUTE" Lamp
10
150mA
"LOC/REM" Lamp
14
150mA
Shift Direction
5
10
LOC/REM Output 1
24
10
LOC/REM Output 2
26
9

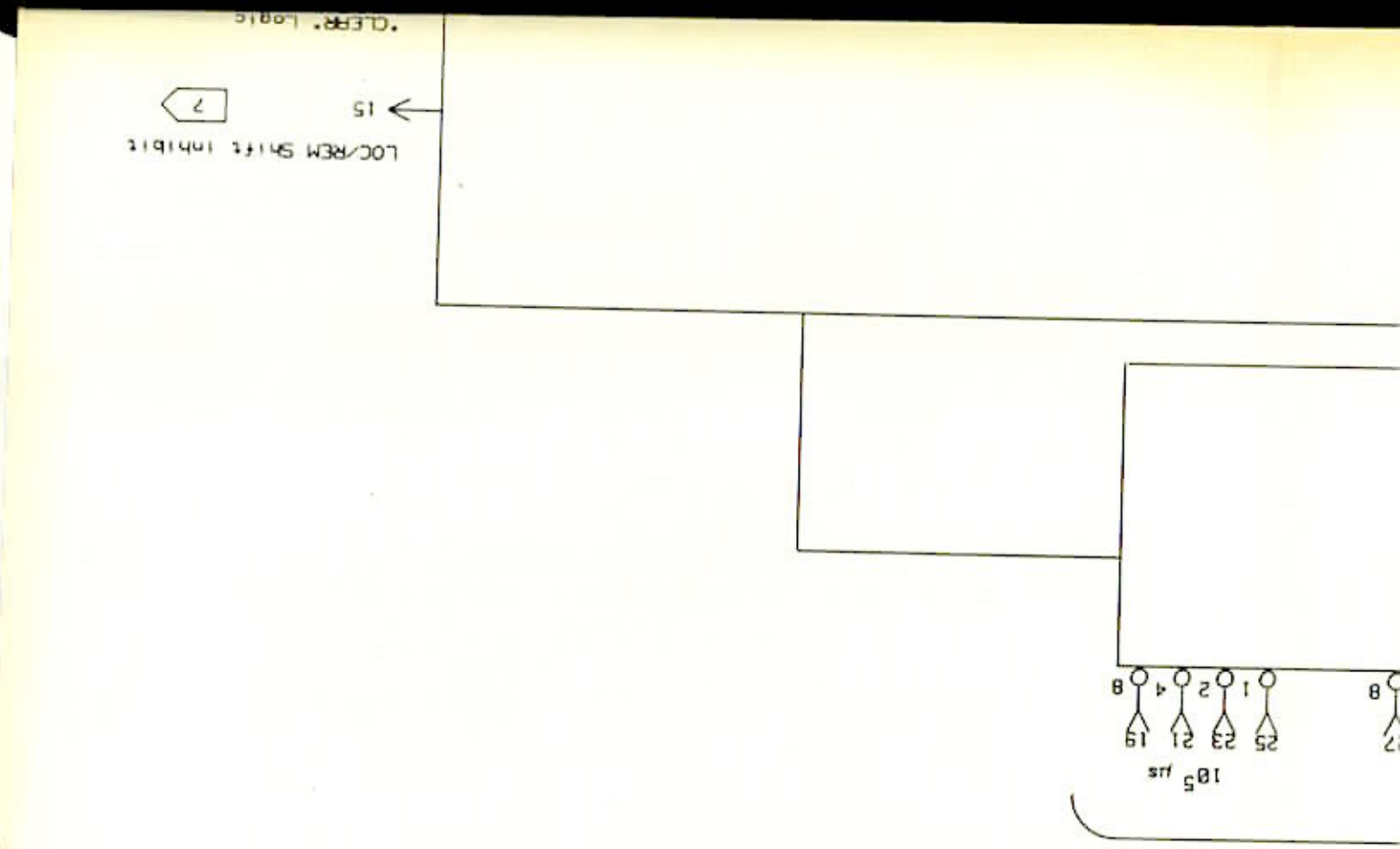


FIGURE 7.8

L-OSC-1: SHIFT PULSE GENERATOR

Generates FALSE going 200 ns wide pulses at approximately 1 MHz rate when enabled during LOAD and EXECUTE modes. During LOAD, pulses are output to L-CNTR-1 only, during EXECUTE, pulses are output to L-CNTR-1 and clock PULSE TO PHASE SHIFTER outputs.

Both logic and lamp driver outputs indicate the state of L-SCL-1, a lamp test input activates all lamp drivers while held FALSE.

36 "CLEAR" Command

32 "LOAD" Command

C7,0.1

11 "EXECUTE" Command

C6,0.1

L-LCH-2: SHIFT DIRECTION LATCH

Follows state of slew direction inputs during LOAD. During CLEAR and EXECUTE, state of latch is held independent of input. Latch state is to control slew direction output when card is designated active by L-LCH-1.

7 Shift Left Command

9 Shift Right Command

22 LOC/REM Secondary Input 1

13 LOC/REM Shift Inhibit

L-LCH-1: LOCAL/ REMOTE LATCH

Stores status of card and controls all signal and indicator outputs of card. Latch is active on card designated by external wiring as LOCAL and may be toggled by LOC/REM shift inputs when L-SCL-1 is in CLEAR state and LOC/REM SHIFT INHIBIT input is TRUE. L-LCH-1 on REMOTE designated card is slaved to the opposite state of L-LCH-1 on LOCAL card. Either the LOCAL or REMOTE designated card was control, depending on the state of L-LCH-1 on the LOCAL card. The card not in control is held in the CLEAR state. Card status is indicated by LOC/REM lamp driver and logic outputs.

20 LOC/REM Shift

28 LOC/REM Shift

C4,0.1

30 LOC/REM Shift

C5,0.1

18 LOC/REM Secondary Input 2

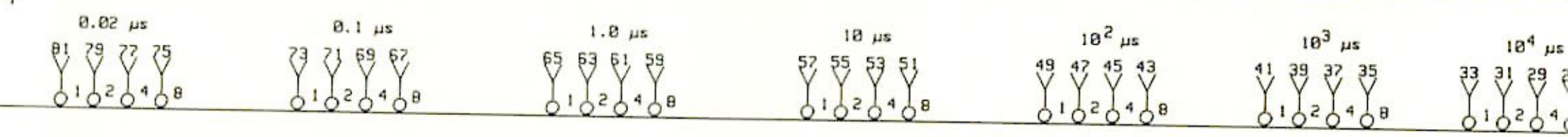
16 Lamp Test

C8,0.1

e 7.8. W0486-5A/CDA Block Diagram

/7.18

9's Complement BCD Inputs (Active Low) [1]



L-CNTR-1: PULSE COUNTER

Is preset to 9's complement of desired number of 20 ns pulse increments (output pulses) during LOAD mode. Least significant stage is preset to 4's complement of least significant digit and operates as a divide by 5. During EXECUTE mode L-CNTR-1 counts the shift pulses output to phase shifter. EARLY CARRY line goes TRUE one count previous to full scale count (99999994) enabling L-SCL-1 to transit synchronously from EXECUTE to CLEAR on the next pulse.

L-SCL-1: SHIFT CONTROL LOGIC

Sequences and controls the LOAD, EXECUTE, and CLEAR functions. Momentary LOW input to the CLEAR COMMAND input will force the logic to the inactive CLEAR state at any time. Momentary LOW input to the LOAD COMMAND input will transit the logic to the LOAD condition, starting L-OSC-1, loading L-CNTR-1 and L-LCH-2 and disabling L-LCH-1. Momentary LOW input to the EXECUTE COMMAND input will synchronously transit the logic to the EXECUTE mode, outputting slew pulses until L-CNTR-1 generates EARLY CARRY then next pulse transits L-SCL-1 synchronously to the CLEAR state. If EXECUTE COMMAND is given when L-CNTR-1 CARRY output is HIGH, indicating a CDR of zero logic transits to CLEAR without outputting slew pulse. Logic transitions are limited to the sequences:

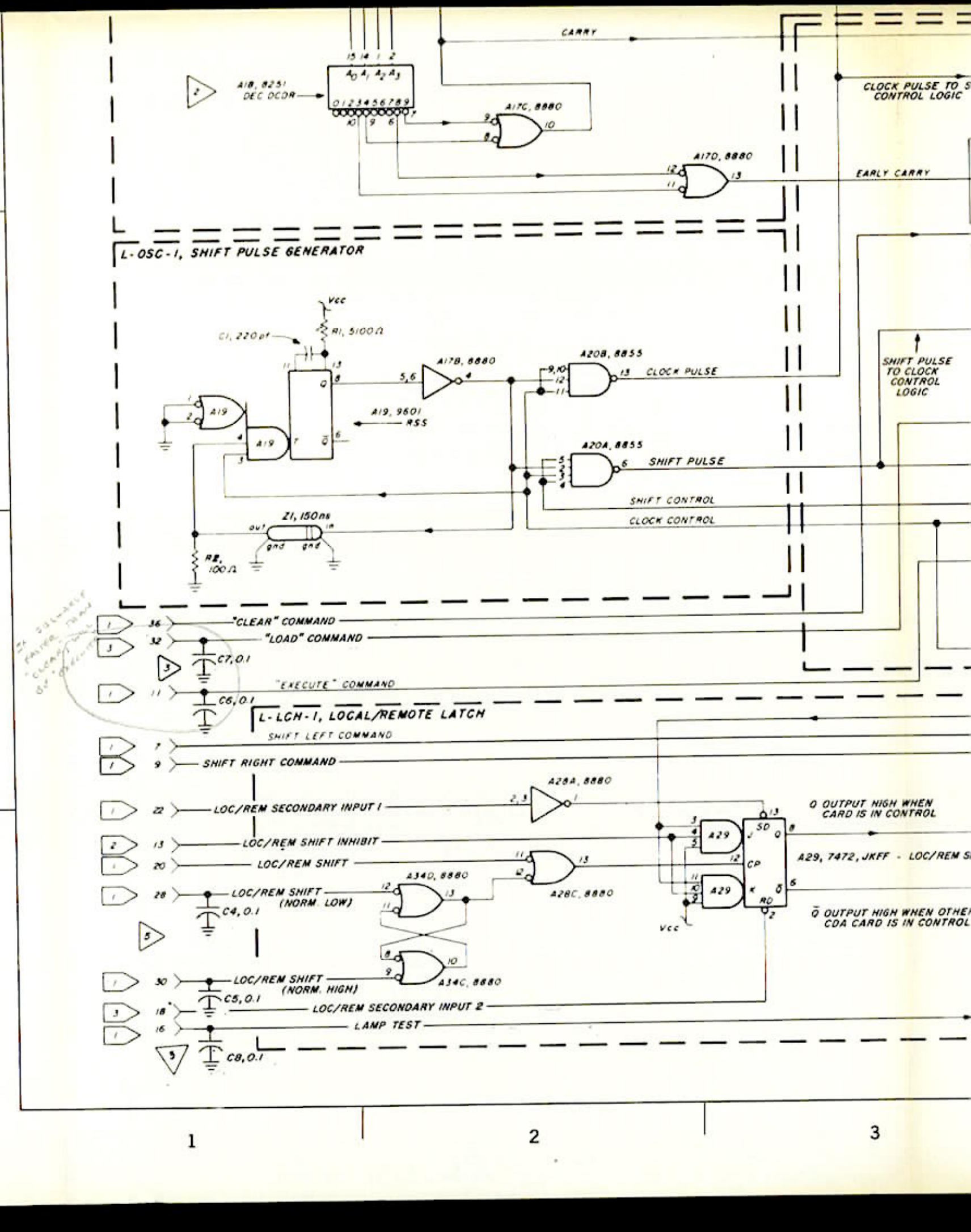
CLEAR → LOAD → EXECUTE

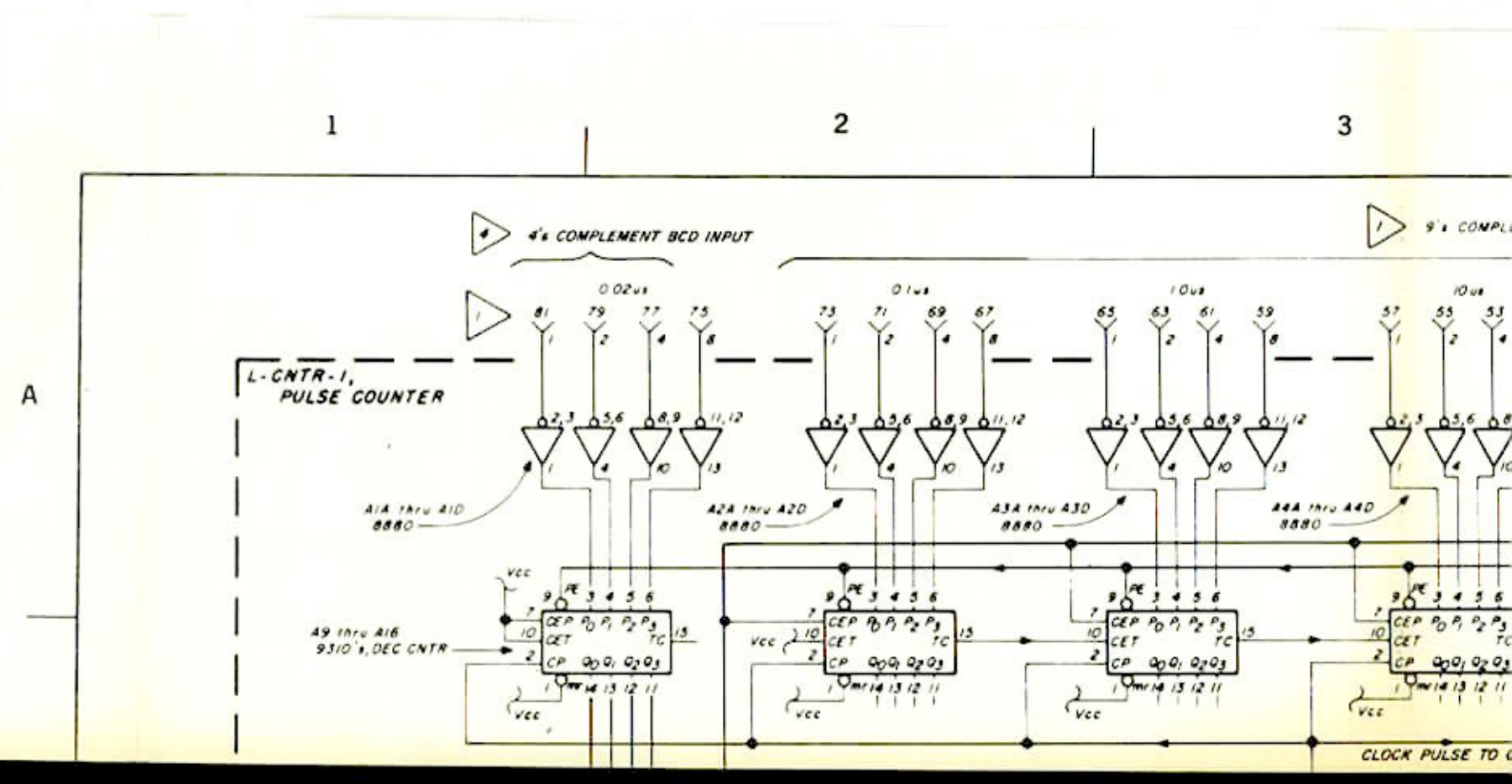


Figur
7.17

PART LOCATION INDEX

REF. DESIG.	LOCATION	REF. DESIG.	LOCATION
A1A	1A	A22	4C
A1B	2A	A23	5C
A1C	2A	A24A	6C
A1D	2A	A24B	6C
A2A	2A	A24C	6D
A2B	2A	A24D	6C
A2C	2A	A25A	6D
A2D	2A	A25B	6C
A3A	3A	A26A	6E
A3B	3A	A26B	NOT USED
A3C	3A	A26C	3D
A3D	3A	A26D	3D
A4A	3A	A27A	5E
A4B	3A	A27B	5D
A4C	3A	A28A	2D
A4D	3A	A28B	7E
A5A	4A	A28C	2E
A5B	4A	A29	3E
A5C	4A	A30	7D
A5D	4A	A31	7D
A6A	4A	A32	7D
A6B	4A	A33	7E
A6C	4A	A34A	NOT USED
A6D	4A	A34B	NOT USED
A7A	5A	A34C	2E
A7B	5A	A34D	2E
A7C	5A	A35A	4D
A7D	5A	A35B	4C
A8A	5A	A35C	4B
A8B	5A		
A8C	5A	C1	1C
A8D	6A	C2	6A
A9	2B	C3	6A
A10	2B	C4	1E
A11	3B	C5	1E
A12	3B	C6	1D
A13	4B	C7	1D
A14	4B	C8	1E
A15	5B	C9	7A
A16	5B	C10	7A
A17A	NOT USED	C11	7D
A17B	2C	C12	7D
A17C	2B	C13	7D
A17D	3B	C14	7D
A18	2B		
A19	1C	E1	NOT SHOWN
A20A	2C	E2	NOT SHOWN
A20B	2C	E3	NOT SHOWN
A21A	3C		
A21B	4C	R1	1C
A21C	3B	R2	1D
		TP1	7C
		TP2	6B
		Z1	1D




1
2
3
A
4's COMPLEMENT BCD INPUT
9's COMPL
0.02us
0.1us
1.0us
10us
L-CNTR-1,
PULSE COUNTER
A1A thru A1D
8880
A2A thru A2D
8880
A3A thru A3D
8880
A4A thru A4D
8880
A9 thru A16
9310's, DEC CNTR
Vcc
CLOCK PULSE TO

L-SCL-1, SHIFT CONTROL LOGIC

TERMINAL COUNT

LOAD COMMAND

LOC/REM. SHIFT (NORMALLY LOW)

LOC/REM. SHIFT (NORMALLY HIGH)

LOC / REM SHIFT INHIBIT

"CLEAR" LOGIC

"LOAD" LOGIC

"EXECUTE" LOGIC

TP-1, YELLOW

SHIFT PULSE TO Ø - SHIFTER

"CLEAR" LAMP

"LOAD" LAMP

"EXECUTE" LAMP

"LOC/REM" LAMP

SHIFT DIRECTION

LOC/REM OUTPUT 1

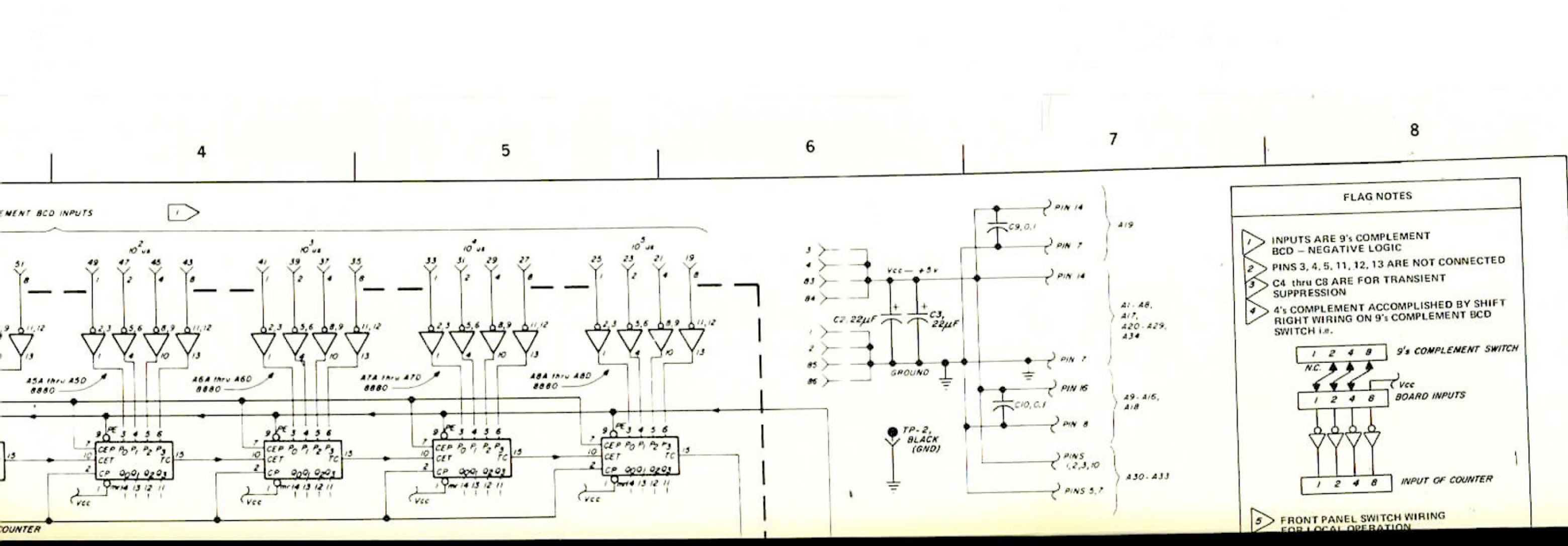
LOC/REM OUTPUT 2

L-LCH-2, SHIFT DIRECTION LATCH

LOC / REM

Figure 7.9. W0486-5A/CDA Schematic Diagram

4 5 6 7 8



FLAG NOTES

1. INPUTS ARE 9's COMPLEMENT BCD – NEGATIVE LOGIC
2. PINS 3, 4, 5, 11, 12, 13 ARE NOT CONNECTED
3. C4 thru C8 ARE FOR TRANSIENT SUPPRESSION
4. 4's COMPLEMENT ACCOMPLISHED BY SHIFT RIGHT WIRING ON 9's COMPLEMENT BCD SWITCH i.e.

5. FRONT PANEL SWITCH WIRING FOR LOCAL OPERATION

B

C

D

E

A

	LOCATION
	2B
	1D
	7E
	4C
	4C
	7C
	3C
	7C
	1B
	2C
	6B
	6C
	6D
	6E
	1A
	7A
	6C
	2B
	1B
	2A
	2A
	1B

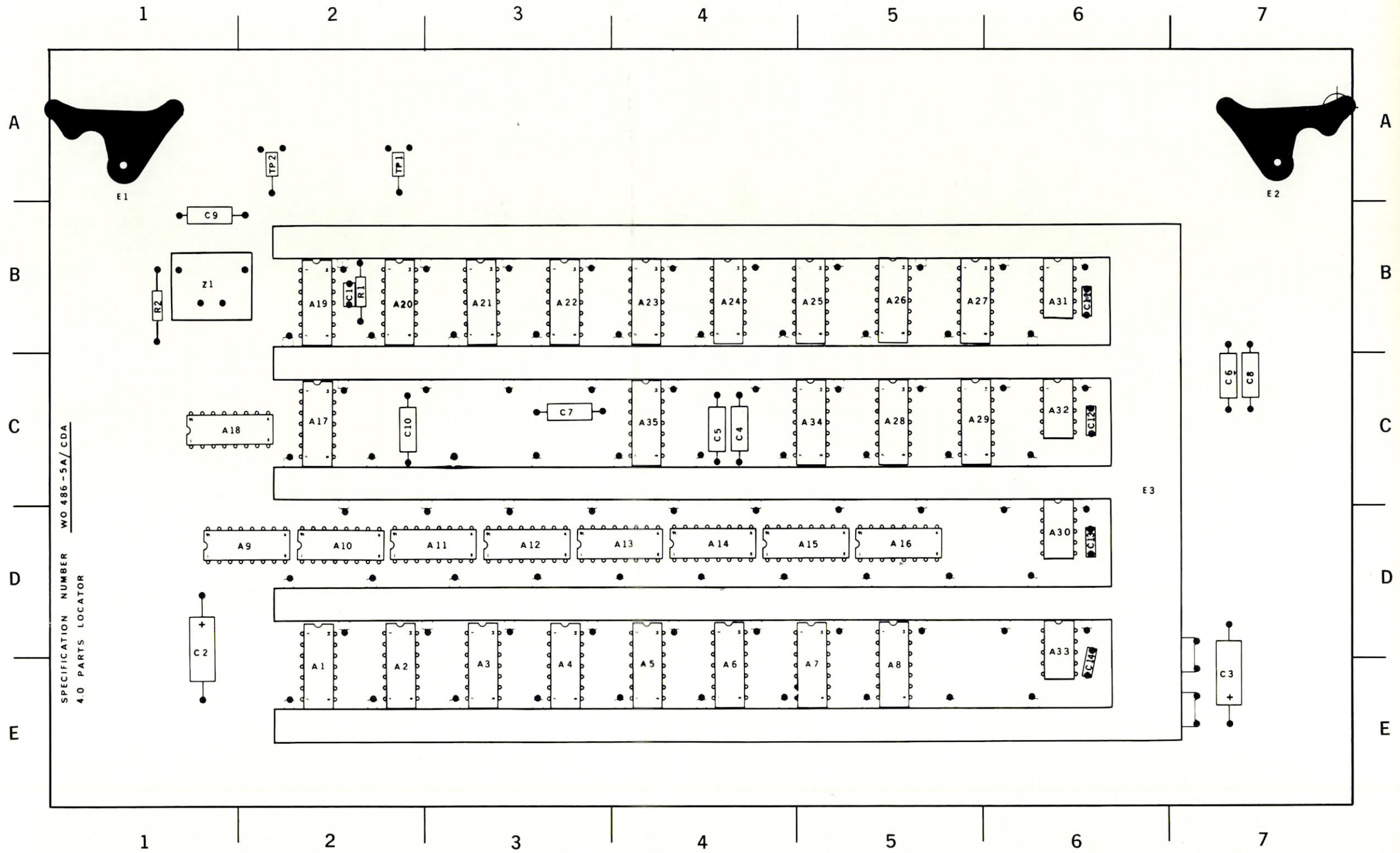
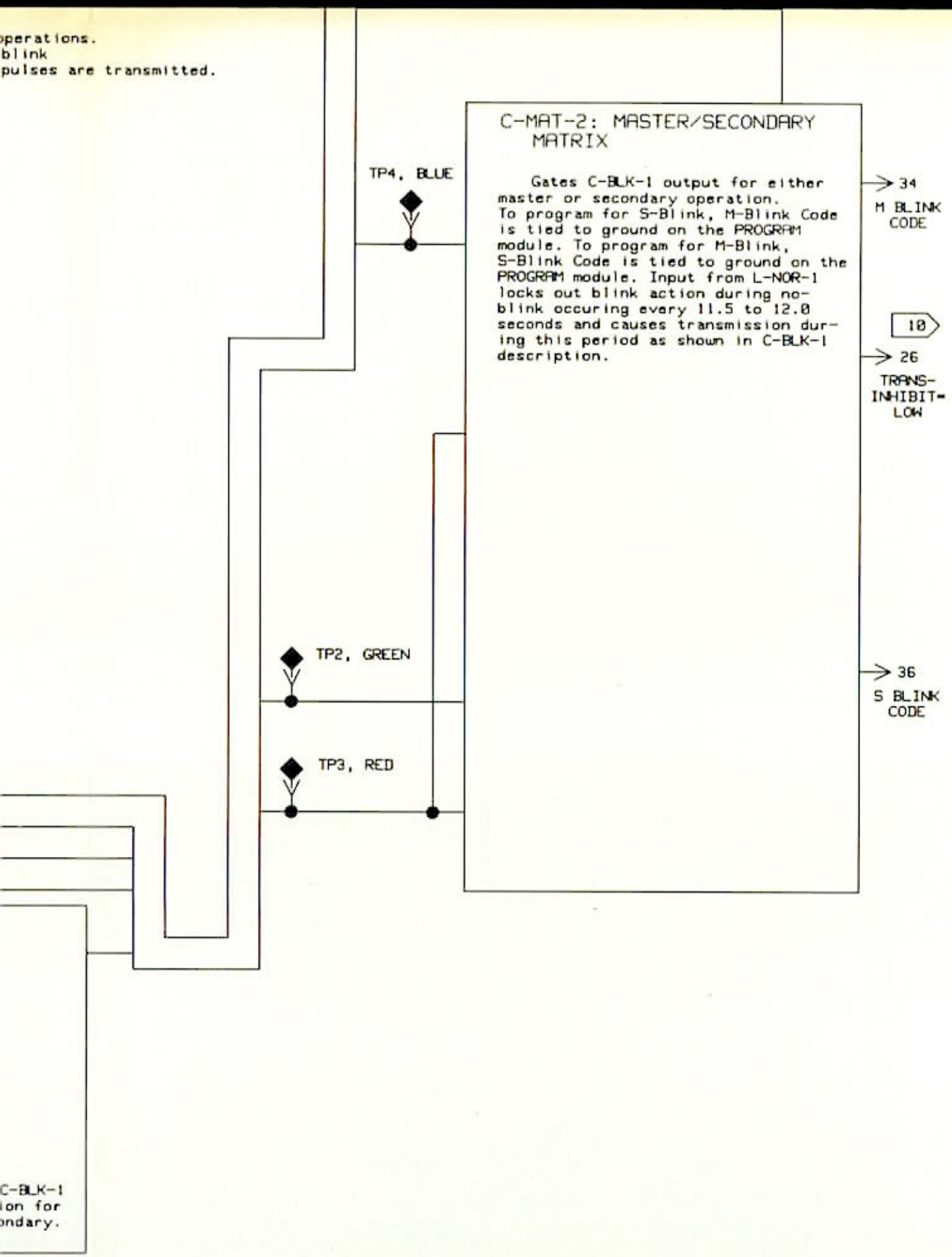


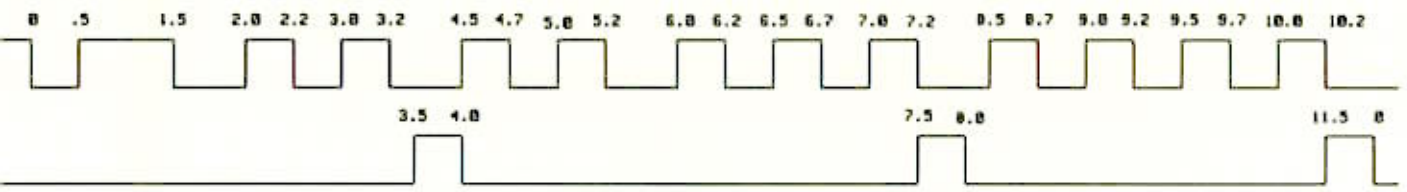
Figure 7.10. W0486-5A/CDA Parts Locator

PART LOCATION INDEX		
REF. DESIG.	LOCATION	REF. DESIG.
A1	2E	C1
A2	2E	C2
A3	3E	C3
A4	3E	C4
A5	4E	C5
A6	4E	C6
A7	5E	C7
A8	5E	C8
A9	1D	C9
A10	2D	C10
A11	3D	C11
A12	3D	C12
A13	4D	C13
A14	4D	C14
A15	5D	
A16	5D	E1
A17	2C	E2
A18	1C	E3
A19	2B	
A20	2B	R1
A21	3B	R2
A22	3B	
A23	4B	TP1
A24	4B	TP2
A25	5B	
A26	5B	Z1
A27	5B	
A28	5C	
A29	5C	
A30	6D	
A31	6B	
A32	6C	
A33	6E	
A34	5C	
A35	4C	

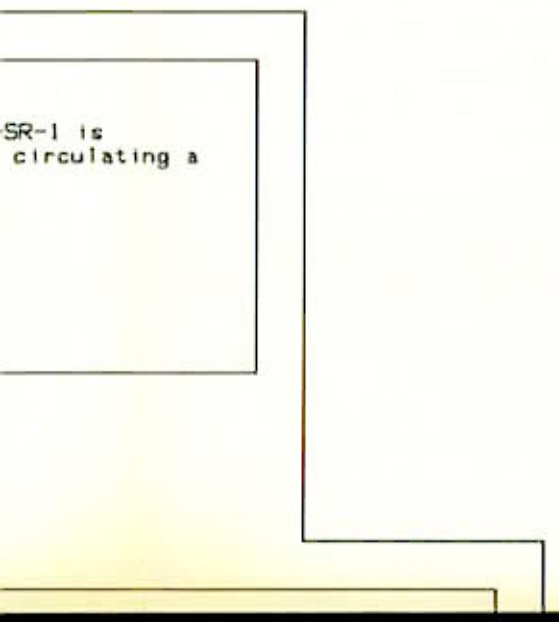
operations.
blink
pulses are transmitted.



MASTER BLINK (NINTH PULSE)



SLAVE BLINK (FIRST TWO PULSES)



MOTE
BLINK 1

CAL
BLINK 1

MOTE 1

CAL 1

MOTE 1

CAL 1

MOTE 1

CAL 1

MOTE
CAL
LECT

1

OTE=LOW

C-SEL-1: LOCAL/REMOTE CONTROL SELECTOR

Selects blink command from either remote or local source. Blink is actuated by a FALSE level on blink command input. Remote command selection designated by FALSE level on REMOTE/LOCAL input.

L-NOR-1: OR GATE

OR's Sx through Sw blink command output of C-SEL-1 to determine that blink is to be initiated. Output enables C-SR-2 to generate blink time base. Feedback from Q24 resets C-SR-1 every 12 seconds to insure single true bit circulates in C-SR-1.

C-MAT-1: BLINK LOGIC MATRIX

Encodes C-SR-1 time base and blink control designation to generate coarse timed blink waveform for both Master and Secondary C-CTR-1 output used to resolve 0.5 second time base from C-SR-1 to 0.2 and 0.3 consecutive increments as shown in C-BLK-1 master waveform is TRUE during periods when ninth pulse is transmitted. Secondary blink waveform is FALSE during periods when first two

C-DVR-1: BLINK DRIVER

Displays master or secondary outputs, blink waveform according to wired connections to C-MAT-1.

1
22
BLINK
GIC - L

92
62
BLINK
LAMP

C-CTR-2: THREE-BIT COUNTER

Counter is cleared by each LORTO pulse. Counter counts multipulse triggers to determine second and eighth trigger for secondary and master operation respectively. Latch is wired to set on slightly delayed second or eighth trigger, generating synchronizing waveform. Synchronizing waveform disables C-MAT-2 after first two pulses during secondary operation or enables C-MAT-2 after eight pulses for master operation.

C-BLK-2: BLINK CODE SYNCHRONIZER

Generates blink synchronizing waveform to enable
at the appropriate time during ninth pulse transmiss
master or first two multipulse transmissions for sec

re 7.11. W0486-6A/BLINK Block Diagram

/7.24

C-BLK-1: BLINK CODE GENERATOR

Generates coarse timed blink waveform for both master ninth pulse blink and secondary first two multipulse blink. This waveform is generated by circulating shift register C-SR-1 and repeats every 12 seconds. Each second is resolved into alternating 0.2 and 0.3 second segments and these are used to define the respective ON/OFF blink periods. The coarse timed waveform is shown below.

2

MJRTY 8
100 KHz

C-CTR-1: 2 Hz DIVIDER

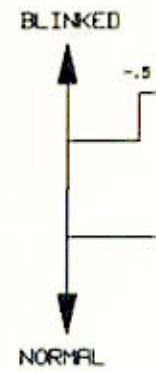
Generates 2 Hz clock for C-SR-1. Output is asymmetric (40% duty cycle) for use by C-MAT-1 in defining 0.2 and 0.3 second intervals of basic 0.5 second clock period.

2

2 Hz 58

C-SR-1: TIME BASE SHIFT REGISTER

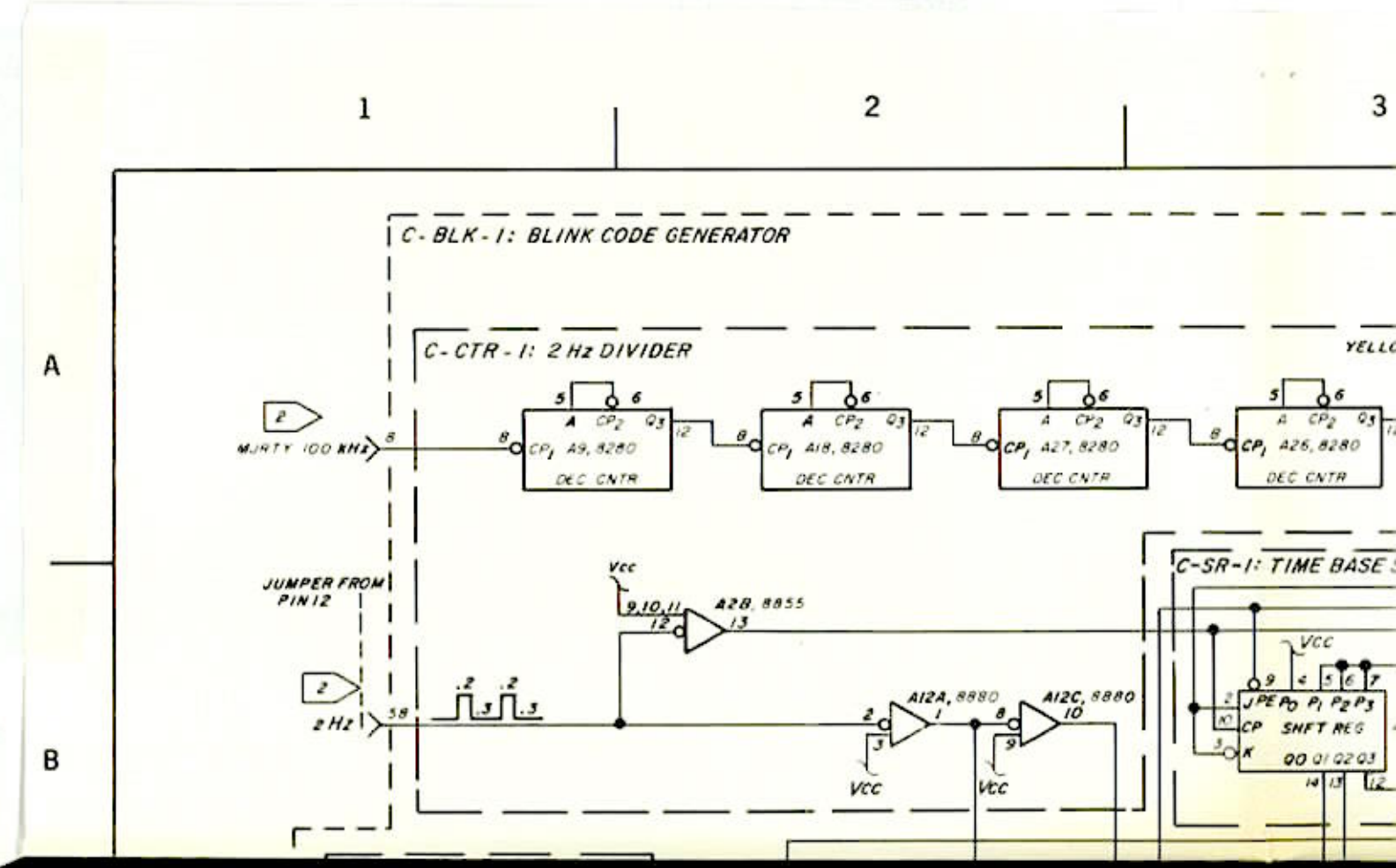
Operated as ring counter to generate blink time base in 0.5 second increments. During no blink condition (L-NOR-1 output FALSE) C- in static parallel entry mode with 100...0 loaded. When blink initiated C-SR-1 operates in serial shift with output coupled to input, single TRUE bit as a ring counter.



C-MAT-1: BLINK LOGIC MATRIX

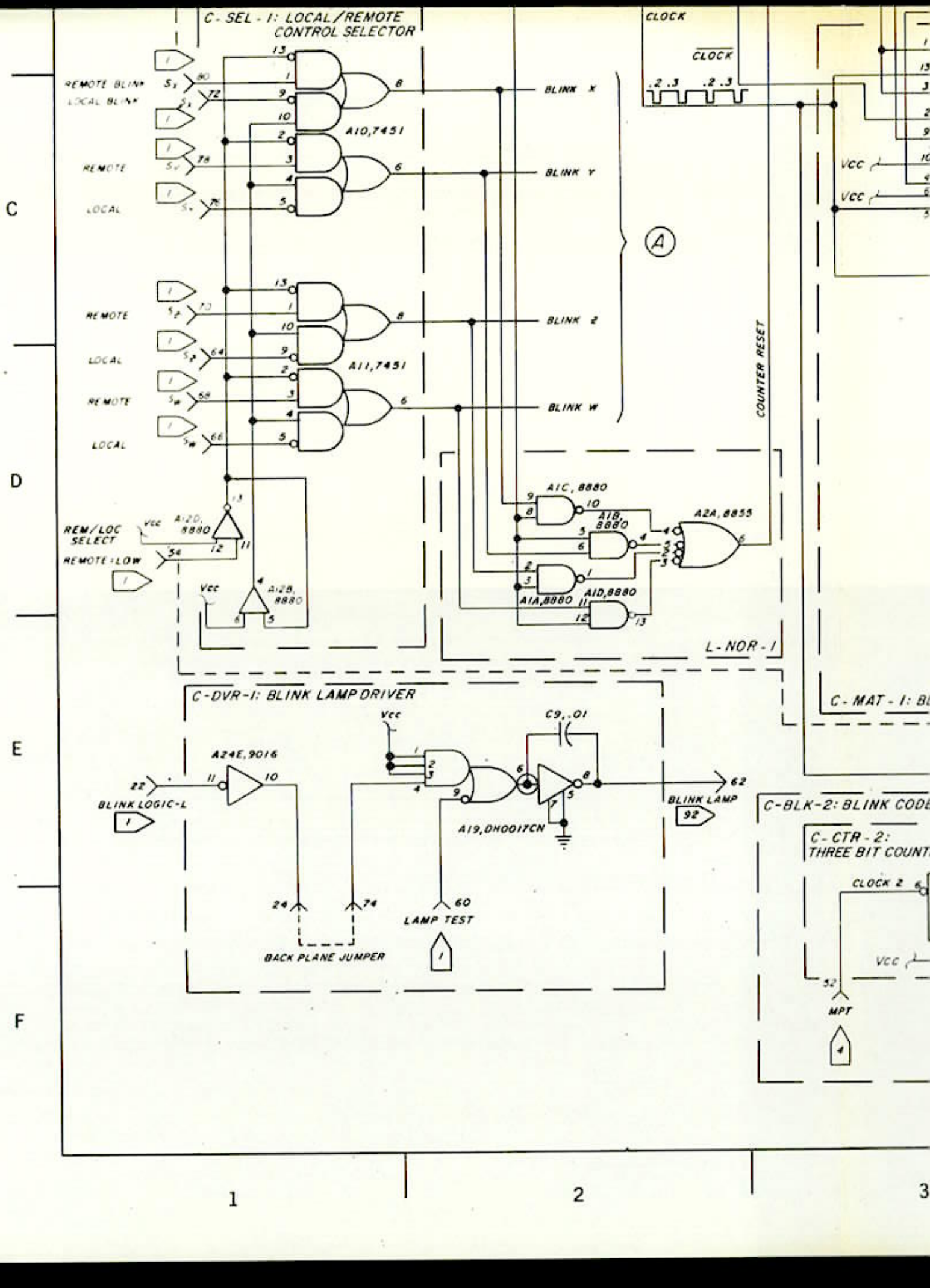


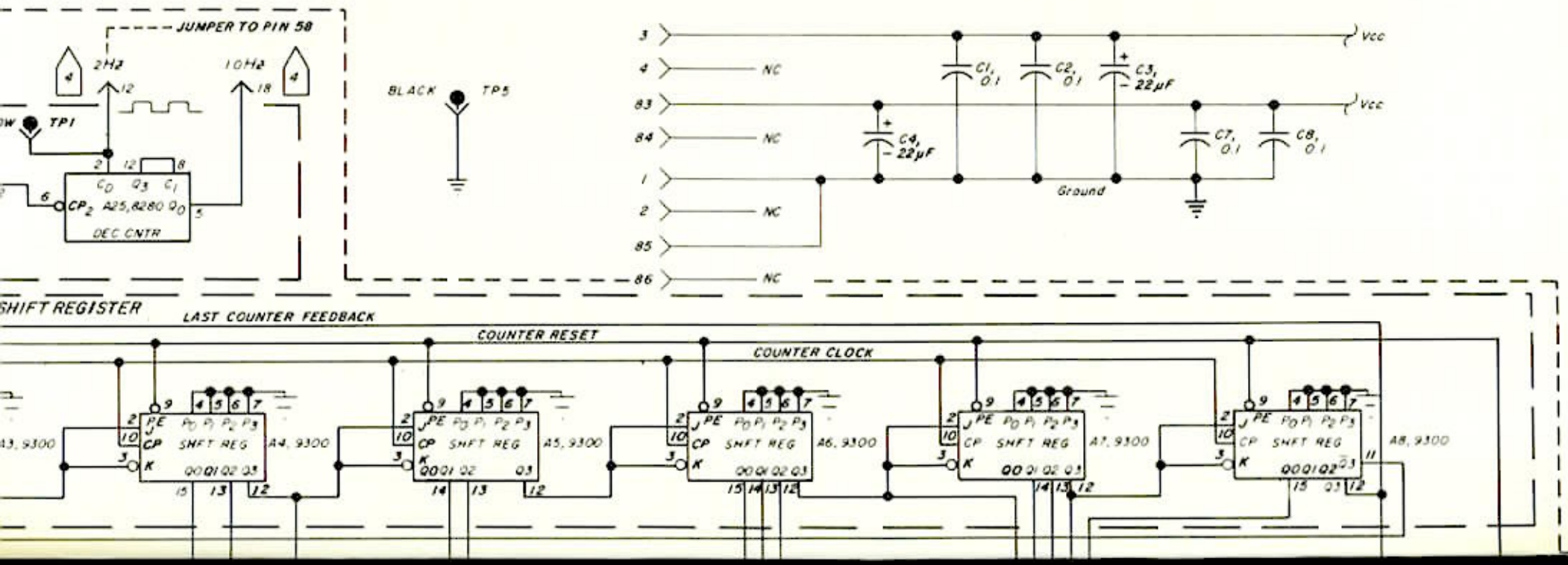
Figu
7.23


1
2
3
A
B
C-BLK-1: BLINK CODE GENERATOR
C-CTR-1: 2 Hz DIVIDER
YELL
MURTY 100 KHz
A9, 8280
A18, 8280
A27, 8280
A26, 8280
DEC CNTR
JUMPER FROM PIN 12
2 Hz
Vcc
A28, 8855
A12A, 8880
A12C, 8880
C-SR-1: TIME BASE
SHFT REG

PART LOCATION INDEX

REF. DESIG.	LOCATION	REF. DESIG.	LOCATION
A1A	2D	A22B	8D
A1B	2D	A22C	8C
A1C	2D	A22D	7C
A1D	2E	A23	7C
A2A	2D	A24A	6C
A2B	2B	A24B	6C
A3	3B	A24C	6C
A4	3B	A24D	7C
A5	4B	A24E	1E
A6	5B	A24F	6D
A7	5B	A25	3A
A8	6B	A26	3A
A9	1A	A27	2A
A10	1C		
A11	1D	C1	5A
A12A	2B	C2	5A
A12B	1D	C3	6A
A12C	2B	C4	5A
A12D	1D	C5	4F
A13	7E	C6	6E
A14	3C	C7	6A
A15	4C	C8	6A
A16	5D	C9	2E
A17	6D		
A18	2A	E1	NOT SHOWN
A19	2E	E2	NOT SHOWN
A20	3F		
A21A	7E	R1	4F
A21B	5E	R2	4F
A21C	5E		
A21D	8D	TP1	3A
A22A	8E	TP2	7E
		TP3	7E
		TP4	7C
		TP5	4A




JUMPER TO PIN 58
2Hz
10Hz
TP1
DEC CNTR
BLACK
TP5
NC
C1, 0.1
C2, 0.1
C3, 22µF
C4, 22µF
C7, 0.1
C8, 0.1
Vcc
Ground
SHIFT REGISTER
LAST COUNTER FEEDBACK
COUNTER RESET
COUNTER CLOCK
SHFT REG
A4, 9300
A5, 9300
A6, 9300
A7, 9300
A8, 9300

A14, 8848

A15, 8840

A16, 8848

A17, 8848

X

Y

Z

W

A24B, 9016

A24C, 9016

A24A, 9016

A24F, 9016

NC

A23, 8848

A13, 8848

A220, 9002

BLUE

TP4

GREEN

TP2

RED

TP3

A24D

A22C, 9002

A22B, 9002

A210, 946

TRANS-
INHIBIT + LOW

34
M BLINK CODE

36
S BLINK CODE

A22A, 9002

A21A, 946

C-MAT-2:
MASTER/SECONDARY MATRIX

(A)

LINK LOGIC MATRIX

E SYNCHRONIZER

A21B, 946

A21C, 946

CONTROL
WAVEFORM

C6, 0.1

A20, 8281
BIN CNTR

STROBE

CLEAR

VCC

R2 10K, 1/4 W

R1 10K
1/4 W

C5,
500 pF

44 CLEAR

LORTO

56 SET INPUT

46

48 M SECONDARY

Figure 7.12. W0486-6A/BLINK Schematic Diagram

4 5 6 7 8


A
B

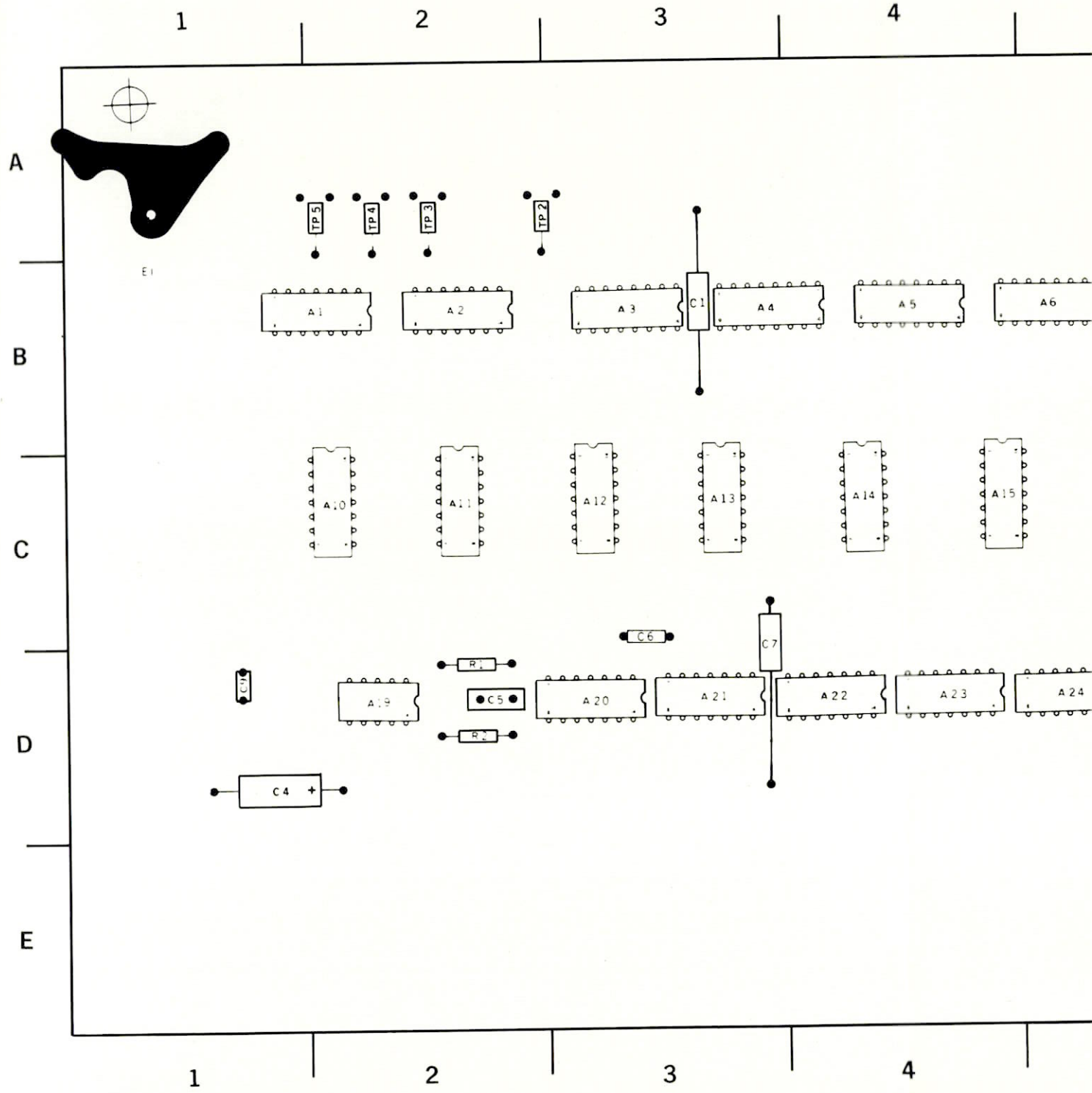
C

D

E

F

PART LOCATION INDEX	
REF. DESIG.	LOCATION
A1	2B
A2	2B
A3	3B
A4	3B
A5	4B
A6	5B
A7	5B
A8	6B
A9	6B
A10	2C
A11	2C
A12	3C
A13	3C
A14	4C
A15	4C
A16	5C
A17	6C
A18	6C
A19	2D
A20	3D
A21	3D
A22	4D
A23	4D
A24	5D
A25	5D
A26	6D
A27	6D
C1	3B
C2	5B
C3	7B
C4	1D
C5	2D
C6	3C
C7	3C
C8	5C
C9	1D
E1	1A
E2	7A
R1	2D
R2	2D
TP1	6A
TP2	2A
TP3	2A
TP4	2A
TP5	2A



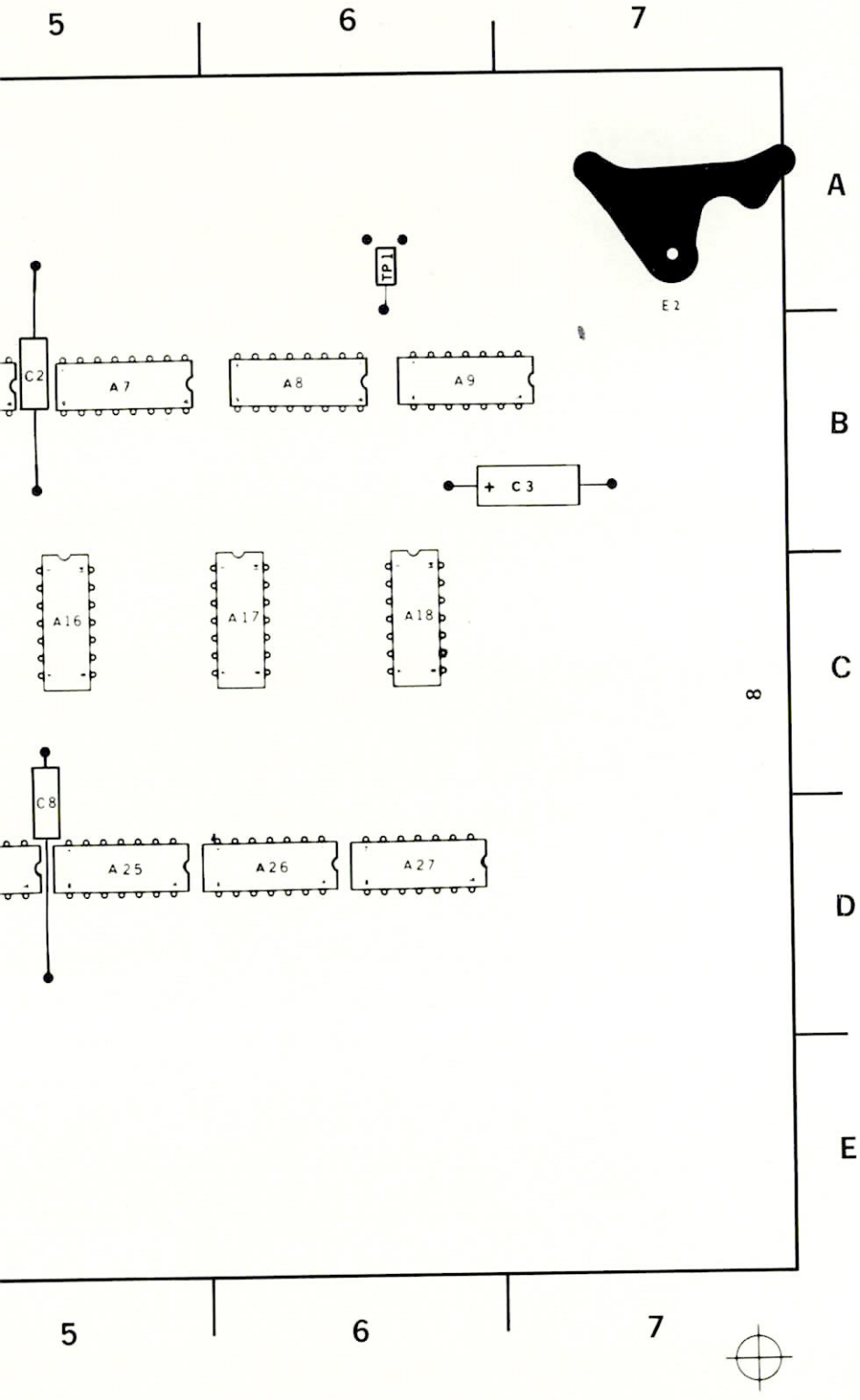


Figure 7.13. W0486-6A/BLINK Parts Locator

4. PARTS LOCATOR

■ = Forked terminal location

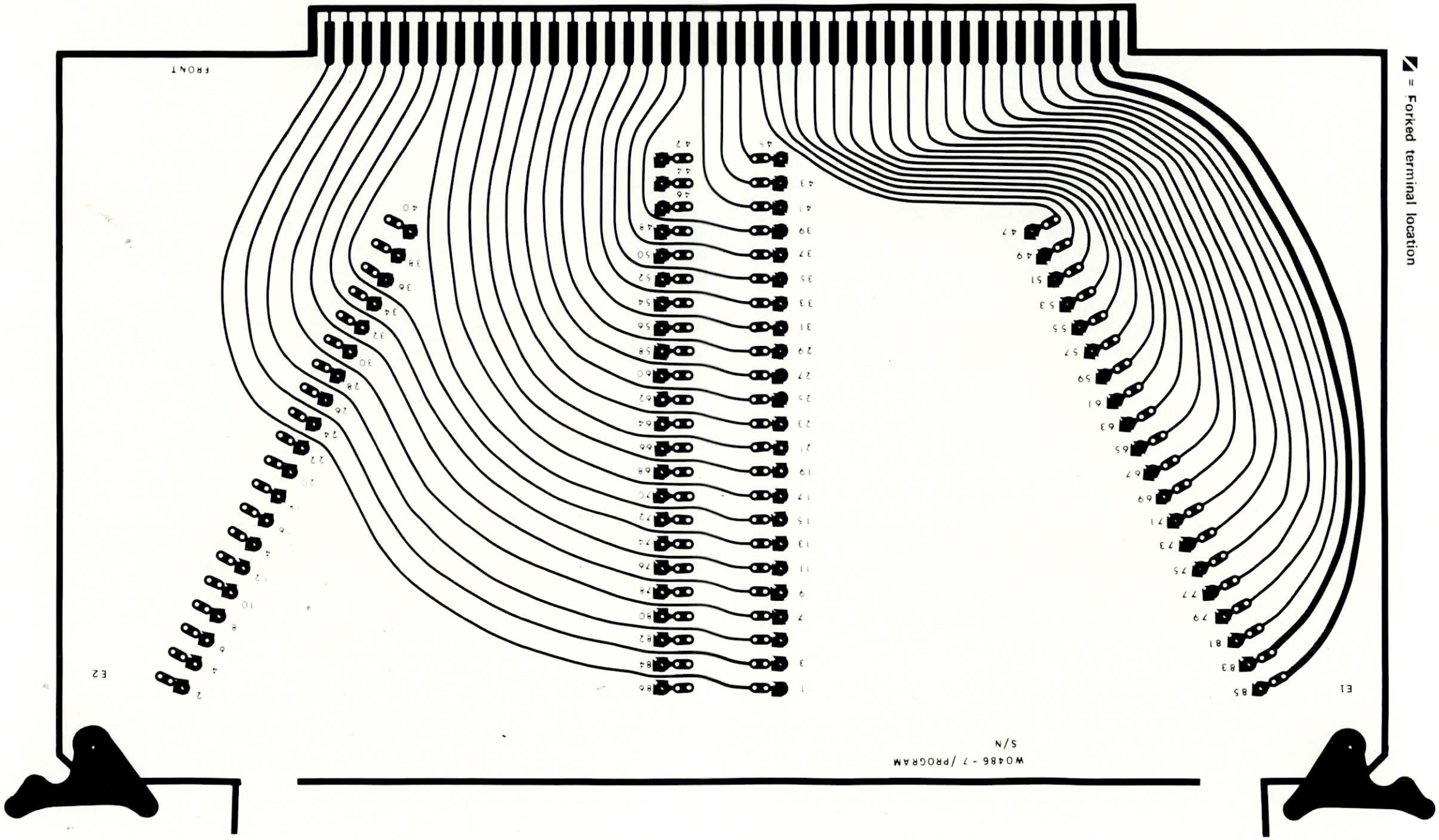
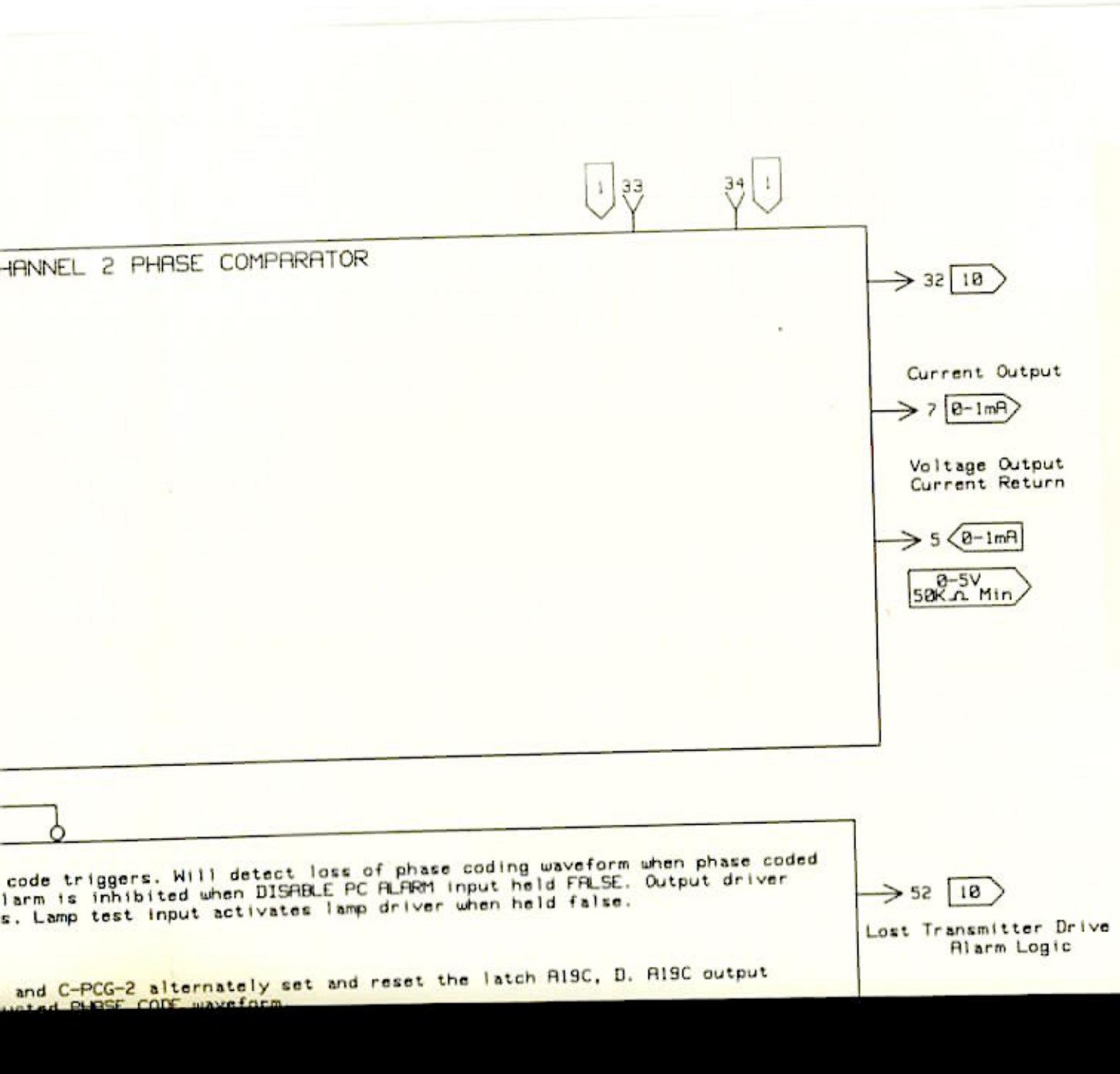


Figure 7.14. W0486-7/PROGRAM Parts Locator


1
33
34
1
HANNEL 2 PHASE COMPARATOR
32
10
Current Output
7
0-1mA
Voltage Output
Current Return
5
0-1mA
0-5V
50KΩ Min
code triggers. Will detect loss of phase coding waveform when phase coded
larm is inhibited when DISABLE PC ALARM input held FALSE. Output driver
s. Lamp test input activates lamp driver when held false.
and C-PCG-2 alternately set and reset the latch A19C, D. A19C output
52
10
Lost Transmitter Drive
Alarm Logic

and A19C output is randomly TRUE or FALSE. A6D output from C-CSL-1 is
CODE waveform depending on the state of A19C, D.
pproximately 3 second runout. A15 Q output remains TRUE so long as A10B
TRUE if A15 is not retriggered. With DISABLE PC ALARM input TRUE, A16B
RM LOGIC and LOST TRANSMITTER DRIVE LAMP outputs to go FALSE. With
e affected by A15.

t drives Q1 into conduction when 100 KHz is present. Q1 collector pulls
ic. Loss of 100 KHz causes Q1 cutoff and prevents A12 from triggering.
N.

d applied to A12 input logic. A12 input logic is satisfied only during

IV Trigger Loss

The EARLY TRIGGER MONITOR pulse (occuring at the beginning of the INTERVAL waveform resets the latch A19A, B. This disables A12 input logic. The MPT MONITOR pulse sets the A19A, B latch if all other inputs to A12 are enabled, this transition triggers the single-shot.
A12 must be triggered at least once each 3 seconds, this required:

1. 100 KHz output be present
2. BLANKING present
3. EARLY TRIGGER and MPT must reset then set A19A, B.

(These conditions must be simultaneously present such that A12 input logic is alternately disabled then enabled. If these conditions are not met, A12 delay runs out and Q goes FALSE causing LOST TRANSMITTER DRIVE ALARM LOGIC output and LOST TRANSMITTER DRIVE LAMP outputs to go FALSE, giving an ALARM indication.

Lost Transmitter Drive Lamp

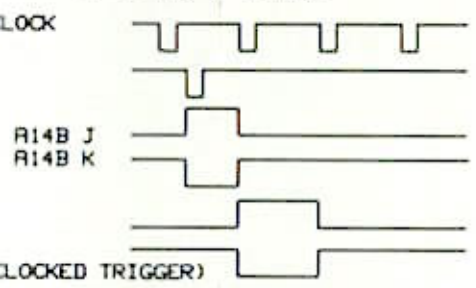
→ 48 [150mA]

→ 43

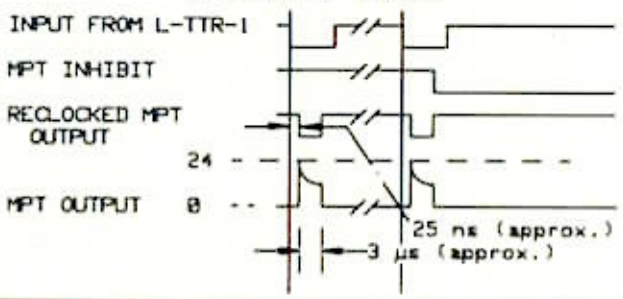
41 39

NOTES:

1. L-TTR-1 TIMING



2. C-TTG-1 TIMING



RFACE

waveforms with various external equipment, providing level shifting, waveshaping,
phase comparison functions.
coarse MPT to MPT RECLOCK waveform.
high-level transmitter triggers (MPT) for driving 50-ohm or 100-ohm loads.
e LOCAL INTERVAL waveform for external use such as blanking.
high-level EARLY TRIGGERS (at the start of the INTERVAL waveform in loran applications).
s, gates and filters 100 KHz square wave input to produce 100 KHz sine wave. Sine wave
ied to 15v p-p. Output has capability to drive 50-ohm or 100-ohm grounded loads.
-2 generate high-level phase code set and reset triggers, respectively, in Loran-C applications.
-2 are phase comparators with analog outputs for driving either current or voltage type meters, or
orders. Comparator is used to monitor local compensation loop activity in loran timer applications.
outputs of C-CSL-1, C-PCG-1, C-PCG-2, C-TTG-1, C-ETG-1 and L-IBA-1 and indicates loss
these outputs by operating a lamp driver and setting a logic level output FALSE.

1 40 42 1

C-REC-1: RECORDER CHANNEL 1 PHASE COMPARATOR

Generates DC output proportional to the phase lead between the FALSE going edge of the VARIABLE input and the selected edge of the majority of the REFERENCE inputs. Output corresponding to 0-360 degrees of phase lead is 0-1 mA through 4K or less floating load and 0-5v into 50K or greater grounded load. CHART POSITIONING switch selects FALSE going edge of REFERENCE as phase standard when in NORMAL position or TRUE going edge when in RECENTER position, allowing positioning of recorder trace near chart center. VARIABLE and REFERENCE signals may have different duty cycles but must be of same frequency between 200 Hz and 1 MHz.

VOLTAGE OUTPUT and feedback for filter is provided by voltage drop across 4.99K resistor. Drop is proportional (5v/mA) to 0-1 mA current flowing in external circuit between CURRENT OUTPUT and CURRENT RETURN. If CURRENT OUTPUT unused, or if external circuit voltage drop exceeds 5v, zener conducts and maintains current through 4.99K resistor.

OPERATION:

Majority gate forms inverted majority of REFERENCE inputs. EXCLUSIVE-OR gate output is in phase when the switch is in the NORMAL position, or inverted REFERENCE majority when the switch is in the RECENTER POSITION. The FALSE going edge of waveform clocks JK-FF to the SET position (Q is TRUE). Edge detector generates a FALSE pulse approximately 15 ns wide at each FALSE going transition of the VARIABLE input. This pulse asynchronously RESETS the JK-FF. JK-FF output is a FALSE pulse with width equal to the time difference between transitions of the VARIABLE input and REFERENCE majority. Q's duty cycle (FALSE time period) is proportional to the phase lead of the VARIABLE with respect to the REFERENCE. JK-FF outputs inverted and applied to the non-inverting input of an active 100 KHz 10 pass filter. Inverting input of the filter is held low by R23C to provide zero reference. Both inverter outputs are pulled up to Vcc by 1000-ohm resistors to provide full 0-to-Vcc voltage swing.

9
11
13
27

38 10

Channel 1 Outputs
Current Output
37 0-1mA

Voltage Output / Current Return
35 0-1mA

0-5V
50K Ω Min

Channel 2 Reference
2
20
22
18

Channel 2 Variable
1
25

C-REC-2: RECORDER C

Same as C-REC-1.

46 Disable PC Alarm

C-PCG-1: PHASE CODE TRIGGER GENERATOR

Generates phase code SET trigger on TRUE going transition of PHASE CODE INPUT waveform when PHASE CODE MODE input is TRUE. Outputis fast rising exponentially decaying trigger of nominally 24V amplitude and 3 us 50 % width into a balanced grounded or floating load.

Operation: Open-collector power driver grounds low end of 1:1.1 pulse transformer primary when driver input logic is satisfied. 0.1 uf capacitor discharges into trnasformer primary, generating fast rising, exponentially decaying trigger. When driver turns off, 0.1 uf

TP4, Brown
PC Set

80 +
82 -

100Ω BAL

Phase Code
Set Trigger

C-TDL-1: TRANSMITTER DRIVE LOSS ALARM

Senses loss of 100 KHz output. Interval, early triggers, transmitter triggers or phase 100 KHz is selected (PHASE CODE MODE held FALSE). Phase code trigger and waveform loss a provided for front-panel indicator. Logic level output goes FALSE to indicate signal los

OPERATION:

I Phase Code Loss

When PHASE CODE MODE is TRUE, PC SET and PC RESET TRIGGER MONITOR pulses from C-PCG-1

capacitor recharges to 24V in approximately 500 us. Diode across primary limits reverse transients. 100-ohm shunt resistor provides termination to absorb transmission line reflections. Transformer secondary is floating to provide isolation and flexibility in driving 100-ohm balanced or 50-ohm unbalanced loads. Transformer tertiary feeds voltage divider to provide TTL- compatible trigger for on-card fault monitoring.

53

PC Set Trigger Monitor

TP3, Green
PC Reset

76 + 100Ω BAL
Phase Code Reset Trigger
78 -

PC Reset Trigger Monitor

is reconstruction of PHASE CODE waveform and is applied to A10B. A10B output is
With PHASE CODE MODE input FALSE, PC SET and PC RESET triggers are no longer generated
now the inverted PHASE CODE waveform and A10B output is either inphase or inverted PHASE
FALSE going transitions of A10B output trigger A15, a retriggerable single-shot with
output makes transitions less than 3 seconds apart. A15's inverted Q output will transit
output will go FALSE indicating an ALARM condition by causing LOST TRANSMITTER DRIVE ALA
DISABLE PC ALARM input FALSE, A16B output is held TRUE, preventing ALARM indication to
II 100 KHz LOSS
100 KHz SINE WAVE OUTPUT is coupled by C41 to a peak detector and filter. Filter outpu
A12, retriggerable 3-second single-shot, inputs FALSE, partially satisfies the input log
If 100 KHz is gated, A12 inputs are only enabled during the time that 100 KHz is gated
III Interval Loss
BLANKING (buffered INTERVAL-FALSE during local interval) output is inverted by A16C ar
the local interval (BLANKING output FALSE).

C-PCG-2: PHASE CODE TRIGGER GENERATOR

Same as C-PCG-1 except PHASE CODE RESET trigger generated on FALSE going edge of PHASE CODE INPUT.

TP1, Red
100 KHz
Sinewave Output

47

C-CSL-1: 100 KHz PHASE CODER, SHAPER, LINE DRIVER

Uses RC filter to shape 100KHz square wave input into sine wave. Sine wave is amplified by operational amplifier, A2, and booster amplifier, A3, to level of nominally 15 volts peak-to-peak into 50 or 100 ohm unbalanced, grounded load. 100 KHz is gated on when 100 KHz GATING INTERVAL INPUT is FALSE. The 100 KHz is phase coded by the PHASE CODE INPUT when PHASE CODE MODE is FALSE. When PHASE CODE MODE is TRUE, 100 KHz continuously coded POSITIVE.

OPERATION:
With PHASE CODE MODE input TRUE, A6D output is FALSE and output of A10A is POSITIVE coded 100 KHz (non-inverted). With PHASE CODE MODE input FALSE, A6D output is inverted PHASE CODE waveform and A10A output is phase coded 100 KHz. 100 KHz square wave from A10A drives open-collector gates A1A through A1C. When to 100 KHz GATING INTERVAL input is FALSE, A1A, B, C output is a 15 V p-p 100 KHz square wave which is applied to an R-C filter network. Filter output is 100 KHz sine wave and is applied via the 100 KHz LEVEL trimpot to operational amplifier, A2 and booster A3 which form a power amplifier with 40 dB voltage gain and are capable of driving 15 V p-p into a 50 or 100-ohm load. Since C-CSL-1 is normally internal to a cycle compensation loop its absolute input to output time delay is uncritical and is not calibrated.

100 KHz
Sinewave Output
46 50Ω

51

TP5, Orange
+ MPT

TP6, Yellow
- MPT

L-IBA-1: INTERVAL BUFFER AMPLIFIER

Buffers the timer INTERVAL waveform for external use such as control of receiver blanking. Output is TTL logic level with 60 unit load driver capability. Output waveform is FALSE during interval.

65 58 60

L-TTR-1: TRANSMITTER TRIGGER RECLOCK

Circuit nine times MPT to MPT RECLOCK waveform.
OPERATION: FALSE going edge of MPT toggles A14A to the SET state. A14B J input is driven TRUE. K input is driven FALSE. The next FALSE transition of MPT RECLOCK toggles A14B to SET state (Q is TRUE, Q is FALSE) generating the FALSE going leading edge of the reclocked trigger and asynchronously RESETTING A14A. This puts A14B J input FALSE and k input TRUE. The next FALSE going transition of MPT RECLOCK TOGGLES A14B to RESET state, generating the TRUE going trailing edge of the reclocked trigger.

See NOTE: 1 for timing.

55 59 63

C-TTG-1: TRANSMITTER TRIGGER GENERATOR

Generates fast rising exponentially decaying trigger at leading edge of reclocked transmitter trigger. Output has nominal 24V peak amplitude and 3 us 50 % width into 100-ohm balanced or 50-ohm grounded load. Triggers are inhibited when MPT INHIBIT input is FALSE.

OPERATION:
FALSE going edge of input from L-TTR-1 triggers 3 us single shot A9 when MPT INHIBIT input is TRUE, generating a FALSE going, 3 us wide RECLOCKED MPT OUTPUT pulse. TRUE going reclocked MPT pulse from A9 drives trigger generator (see C-PCG-1 for details). Putting MPT INHIBIT FALSE will prevent A9 from triggering on subsequent inputs but will not affect the single shot delay cycle once triggered.

See NOTE: 2 for timing.

68 + 100Ω BAL
MPT Out
66 -

MPT MONITOR

61 10
RECLOCKED MPT OUTPUT

EARLY TRIGGER MONITOR

C-ETG-1: EARLY TRIGGER GENERATOR

Generates fast rising exponentially decaying trigger at start of INTERVAL (FALSE going edge). Output is nominally 24 V peak amplitude and 3 us 50 % width into 100 ohm unbalanced loads.

OPERATION:
See C-PCG-1 for further explanation of trigger generator.

64

72 + 100Ω BAL
Early Trigger Output
74 -

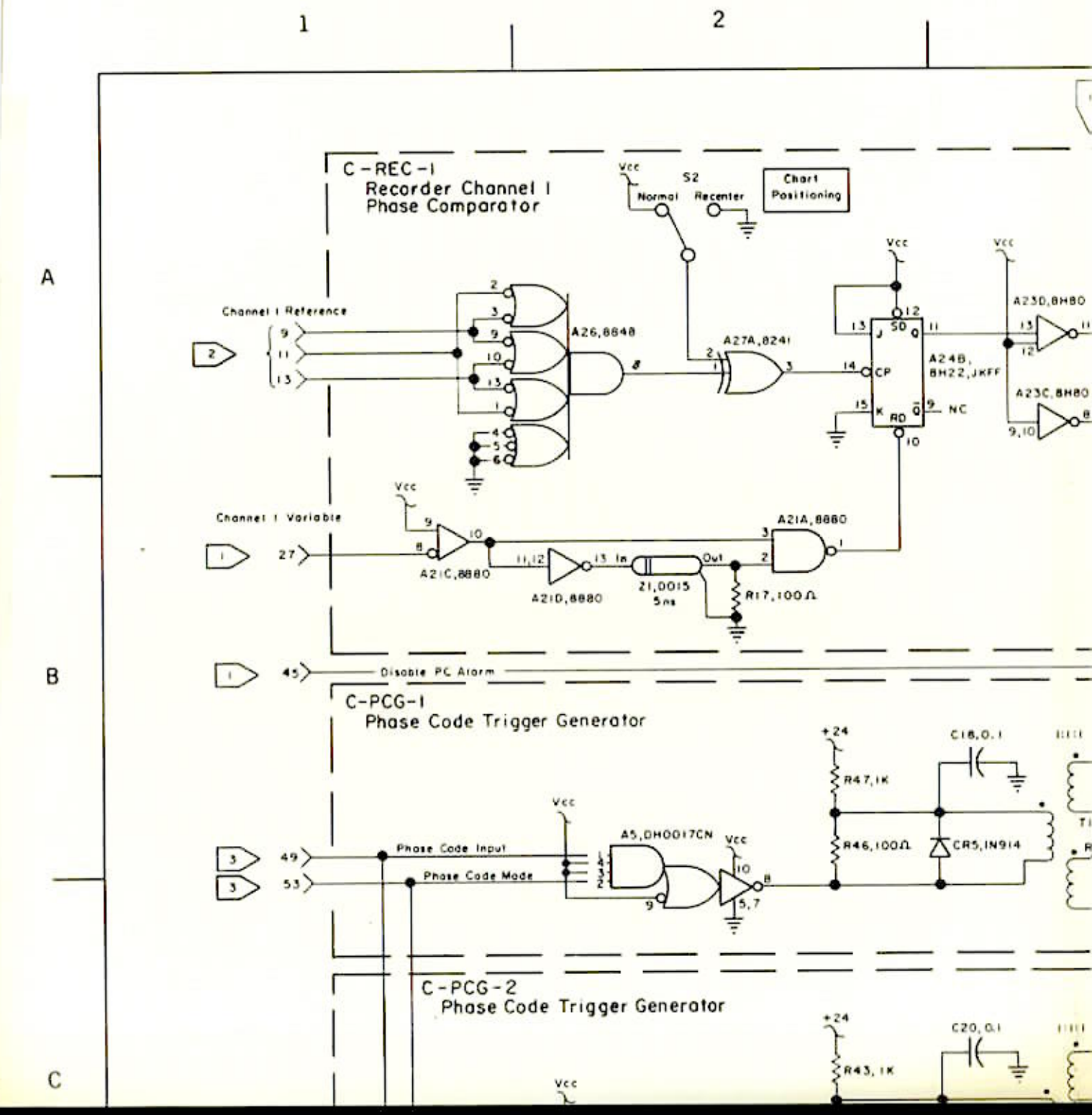
W0486-8A/INTE
Interfaces timer
phase coding and
L-TTR-1 reclocks
C-TTG-1 generates
L-IBA-1 buffers t
C-ETG-1 generates
C-CSL-1 Phase cod
is amplif
C-PCG-1 and C-OCG
C-REC-1 and C-REC
chart rec
C-TDL-1 monitors
of any of

re 7.15. W0486-8A/INTERFACE Block Diagram
/7.32


Channe
Refer
2
Channe
Vari
1
1

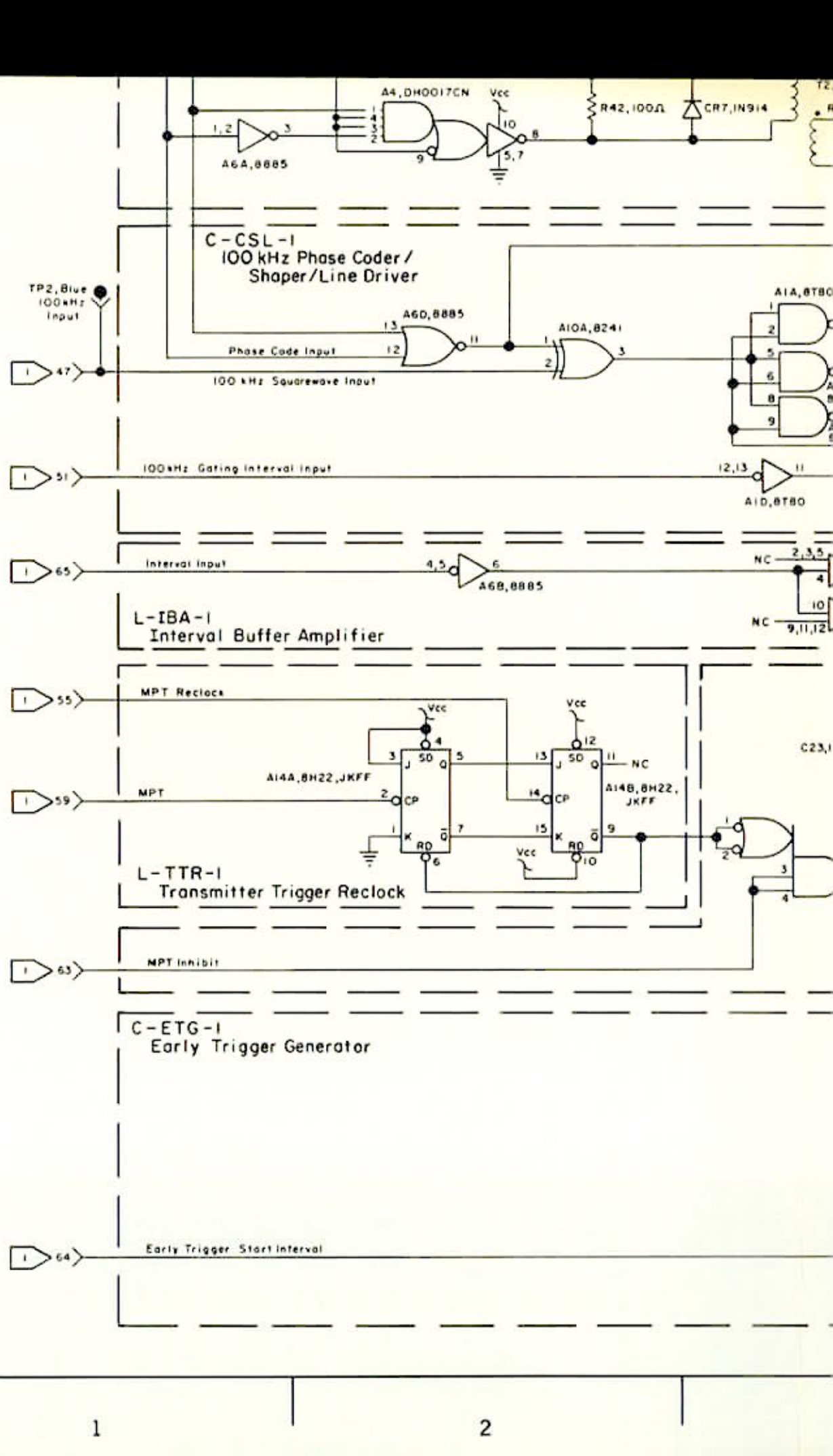

3
TP2, E
100KHz
100KHz
Square
100KHz
Interv
Interv
MPT Re
MPT1
MPT In
Early
Start

Figu
7.31

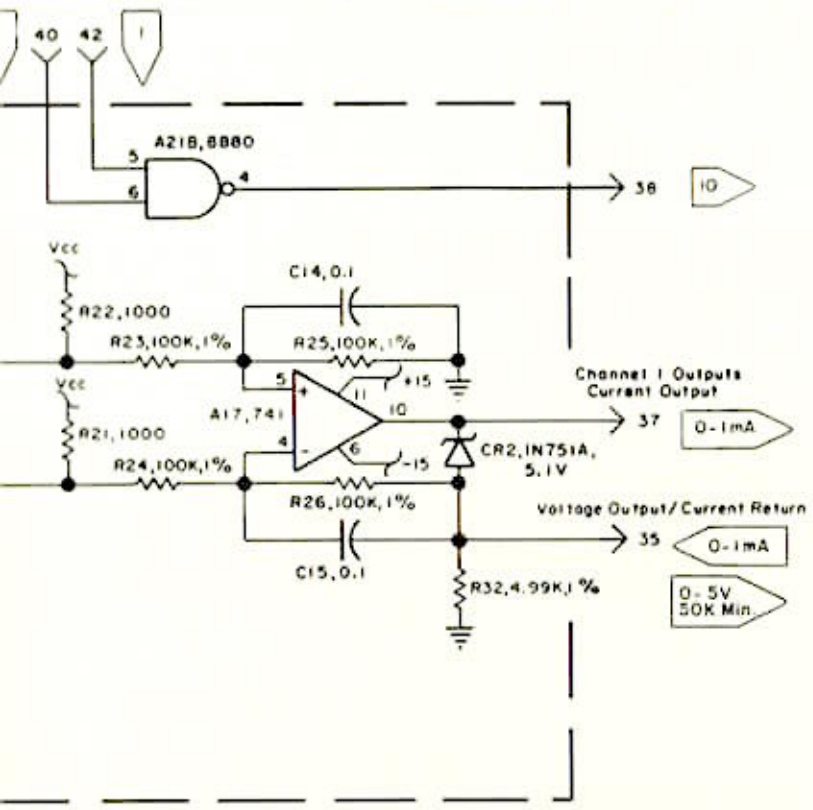

1
2
A
B
C
C-REC-1
Recorder Channel 1
Phase Comparator
Vcc
S2
Normal
Recenter
Chart
Positioning
Channel 1 Reference
A26,8648
A27A,8241
A24B,
8H22,JKFF
A23D,8H80
A23C,8H80
NC
Channel 1 Variable
A21C,8880
A21D,8880
A21A,8880
21,0015
5ns
R17,100Ω
Disable PC Alarm
C-PCG-1
Phase Code Trigger Generator
+24
C18,0.1
R47,1K
R46,100Ω
CR5,IN914
Phase Code Input
Phase Code Mode
A5,DH0017CN
C-PCG-2
Phase Code Trigger Generator
C20,0.1
R43,1K

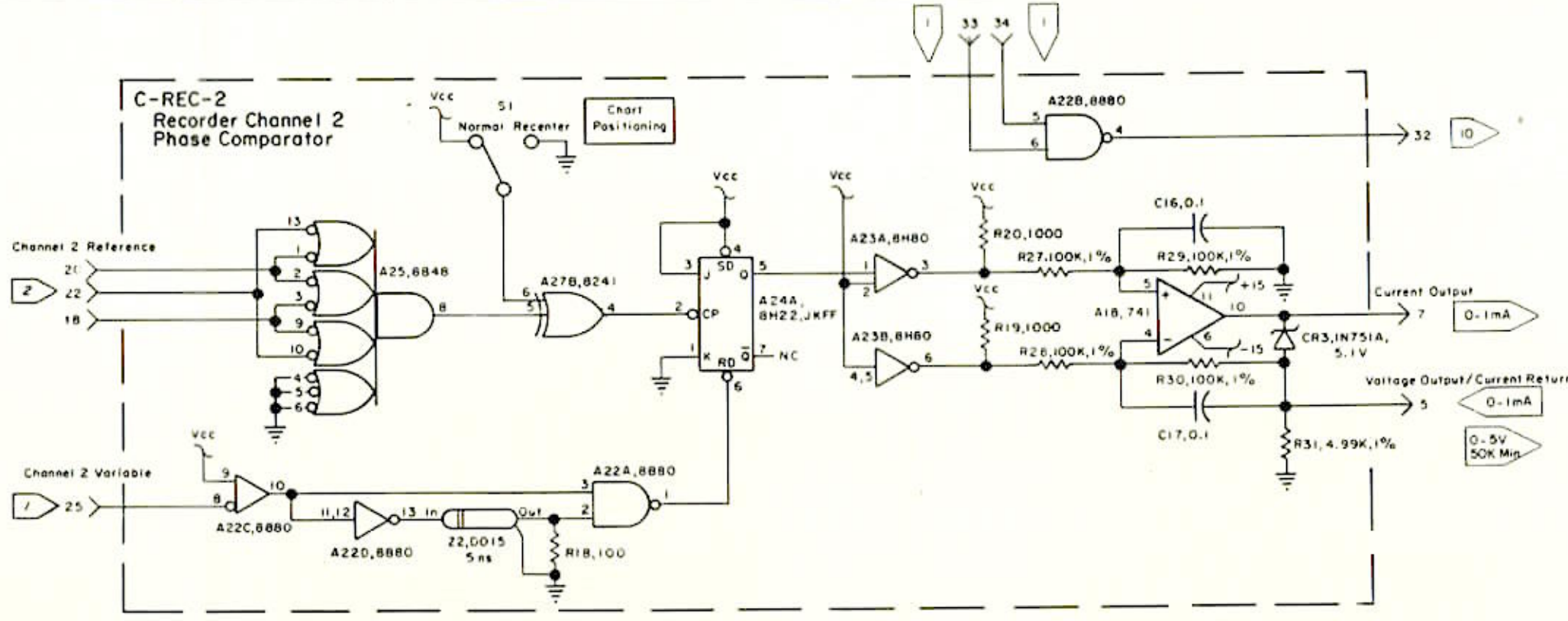
PART LOCATION INDEX

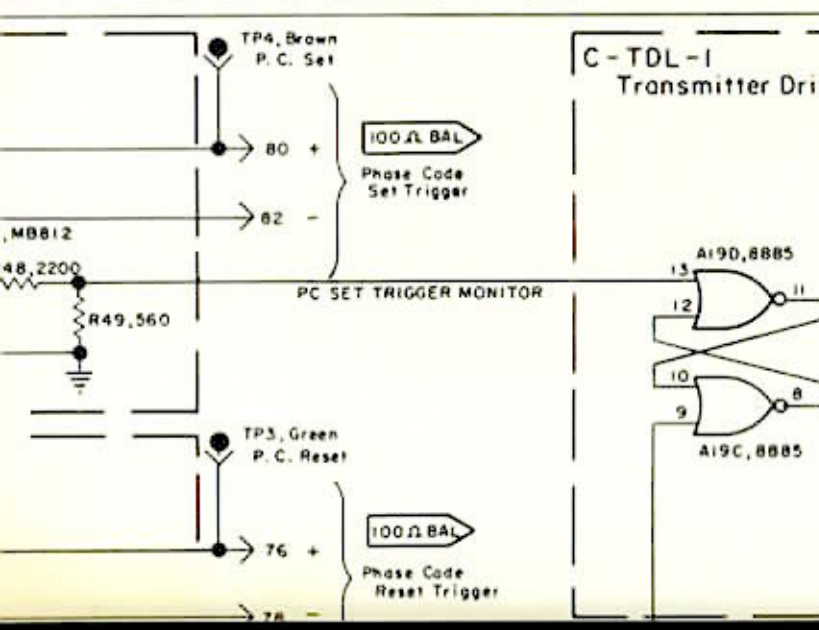
REF.DESIG.	LOCATION	REF.DESIG.	LOCATION	REF.DESIG.	LOCATION	REF.DESIG.	LOCATION
A1A	3D	A24A	6A	C41	6D	R25	3A
A1B	3D	A24B	2A			R26	3A
A1C	3D	A25	5A	CR1	6D	R27	7A
A1D	3D	A26	2A	CR2	4A	R28	7A
A2	5D	A27A	2A	CR3	8A	R29	7A
A3	5D	A27B	6A	CR4	4E	R30	7A
A4	2C			CR5	3B	R31	8B
A5	2B	C1	3D	CR6	4F	R32	4B
A6A	1C	C2	3D	CR7	3C	R33	6D
A6B	2D	C3	4D	CR8	5D	R34	4F
A6C	NOT USED	C4	4D	CR9	5D	R35	4F
A6D	2D	C5	4D			R36	5F
A7A	6C	C6	5D	E1	NOT SHOWN	R37	5F
A7B	7B	C7	5D	E2	NOT SHOWN	R38	4E
A8	7C	C8	NOT USED	E3	NOT SHOWN	R39	4E
A9	3E	C9	5D	E4	NOT SHOWN	R40	5E
A10A	2D	C10	7F	E5	NOT SHOWN	R41	5E
A10B	5C	C11	7F	E6	NOT SHOWN	R42	2C
A11A	3D	C12	6D			R43	2C
A11B	3E	C13	7D	Q1	6D	R44	3C
A12	7D	C14	3A	Q2	7D	R45	3C
A13	4E	C15	3A	Q3	6B	R46	2B
A14A	2E	C16	7A			R47	2B
A14B	2E	C17	7A	R1	3D	R48	3B
A15	5B	C18	3B	R2	3D	R49	3C
A16A	7E	C19	7F	R3	4D	R50	5D
A16B	6C	C20	3C	R4	4D	R51	7D
A16C	7D	C21	8F	R5	4D	R52	6B
A17	3A	C22	5B	R6	4D		
A18	7A	C23	3E	R7	5D	S1	6A
A19A	7E	C24	4E	R8	5C	S2	2A
A19B	7E	C25	5E	R9	NOT USED		
A19C	4C	C26	4F	R10	3D	T1	3B
A19D	4B	C27	5F	R11	6D	T2	3C
A20	4F	C28	7F	R12	6D	T3	5E
A21A	2B	C29	8F	R13	7D	T4	5F
A21B	3A	C30	8F	R14	3E		
A21C	1B	C31	8F	R15	5B	TP1	6C
A21D	2B	C32	8F	R16	7D	TP2	1D
A22A	6B	C33	7F	R17	2B	TP3	3C
A22B	7A	C34	7F	R18	6B	TP4	3B
A22C	5B	C35	7F	R19	7A	TP5	5D
A22D	5B	C36	5D	R20	7A	TP6	5D
A23A	7A	C37	5D	R21	3A	TP7	8C
A23B	7A	C38	7F	R22	3A		
A23C	3A	C39	6D	R23	3A	Z1	2B
A23D	3A	C40	7B	R24	3A	Z2	6B

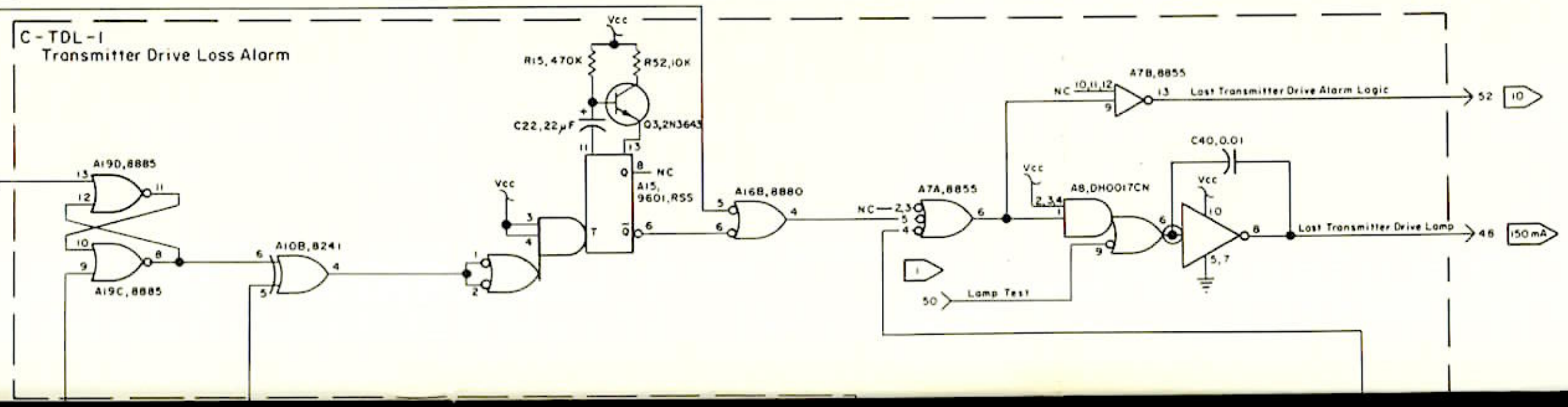


3 4 5 6 7 8


40 42 1
A21B,8880
38 10
Vcc
R22,1000
C14,0.1
R23,100K,1%
R25,100K,1%
+15
A17,741
Channel 1 Outputs
Current Output
37
0-1mA
CR2,IN751A,
5.1V
R21,1000
R24,100K,1%
-15
R26,100K,1%
Voltage Output/Current Return
35
0-1mA
C15,0.1
R32,4.99K,1%
0-5V
50K Min.


C-REC-2
Recorder Channel 2
Phase Comparator
Vcc
S1
Normal Recenter
Chart
Positioning
Channel 2 Reference
2
22
18
A25,6848
A27B,8241
A24A,
8H22,JKFF
SD
CP
RD
NC
A23A,8H80
A23B,8H80
A22B,8880
32 10
R20,1000
R27,100K,1%
R19,1000
R28,100K,1%
C16,0.1
R29,100K,1%
A18,741
Current Output
7
0-1mA
CR3,IN751A,
5.1V
R30,100K,1%
Voltage Output/Current Return
5
0-1mA
C17,0.1
R31,4.99K,1%
0-5V
50K Min.
Channel 2 Variable
25
A22C,8880
A22D,8880
22,0015
5ns
R18,100
A22A,8880


TP4, Brown
P.C. Set
80 +
82 -
100Ω BAL
Phase Code
Set Trigger
,MB812
48,2200
R49,560
PC SET TRIGGER MONITOR
TP3, Green
P.C. Reset
76 +
100Ω BAL
Phase Code
Reset Trigger


C-TDL-1
Transmitter Drive Loss Alarm
A19D,8885
A19C,8885
A10B,8241
R15,470K
R52,10K
C22,22μF
Q3,2N3643
A15,
9601,RSS
A16B,8880
A7A,8855
A7B,8855
Lost Transmitter Drive Alarm Logic
52 10
C40,0.01
A8,DH0017CN
Lost Transmitter Drive Lamp
48 150mA
Lamp Test
50

C-TTG-1
Transmitter Trigger Generator

PC RESET TRIGGER MONITOR

TP1, Red
100 kHz
Sinewave Output

100kHz Sinewave Output

TP7, Black

TP5, Orange
+MPT

TP6, Yellow
-MPT

Blanking

MPT Output

MPT Monitor

Reclocked MPT Output

Early Trig. Monitor

Early Trigger Output

NOTES:
1. ALL CAPACITOR VALUES IN MICROFARADS UNLESS OTHERWISE INDICATED.
2. NC = NO CONNECTION

Figure 7.16. W0486-8A/INTERFACE Schematic Diagra


A
B
C


D
E
F
m
4

	REF.DESIG.	LOCATION
	R19	6D
	R20	7D
	R21	6D
	R22	6D
	R23	6D
	R24	6D
	R25	6D
	R26	6D
	R27	7D
	R28	7D
	R29	7D
	R30	7D
	R31	7D
	R32	6D
	R33	5B
	R34	2D
	R35	2D
	R36	3D
	R37	3D
	R38	2C
	R39	2C
	R40	3C
	R41	3C
	R42	1D
	R43	1D
	R44	2D
	R45	2D
	R46	1C
	R47	1C
	R48	2C
	R49	2C
	R50	3B
	R51	5B
	R52	4D
	S1	6A
	S2	6A
	T1	1C
	T2	1E
	T3	2C
	T4	2E
	TP1	5A
	TP2	5A
	TP3	3A
	TP4	2A
	TP5	2A
	TP6	2A
	TP7	1A
	Z1	4E
	Z2	5E

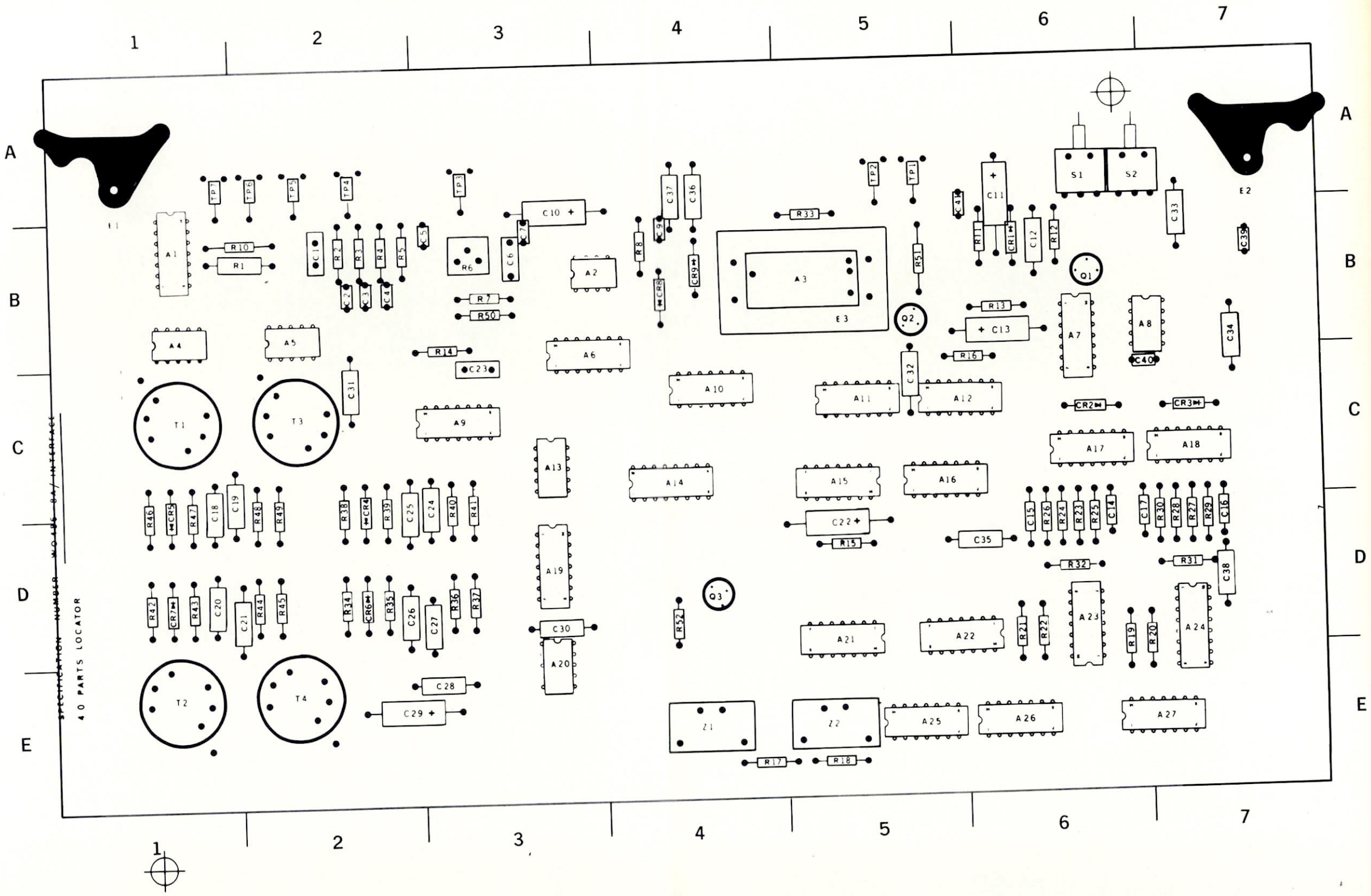


Figure 7.17. W0486-8A/INTERFACE Parts Locator

PART LOCATION INDEX

REF.DESIG.	LOCATION	REF.DESIG.	LOCATION
A1	1B	C26	2D
A2	3B	C27	3D
A3	5B	C28	3E
A4	1B	C29	2E
A5	2B	C30	3D
A6	3B	C31	2C
A7	6B	C32	5C
A8	7B	C33	7B
A9	3C	C34	7B
A10	4C	C35	6D
A11	5C	C36	4A
A12	5C	C37	4A
A13	3C	C38	7D
A14	4C	C39	7B
A15	5C	C40	7C
A16	5C	C41	6B
A17	6C		
A18	7C	CR1	6B
A19	3D	CR2	6C
A20	3E	CR3	7C
A21	5D	CR4	2C
A22	5D	CR5	1C
A23	6D	CR6	2D
A24	7D	CR7	1D
A25	5E	CR8	4B
A26	6E	CR9	4B
A27	7E		
		E1	1A
C1	2B	E2	7A
C2	2B	E3	5B
C3	2B	E4	NOT SHOWN
C4	2B	E5	NOT SHOWN
C5	3B	E6	NOT SHOWN
C6	3B	Q1	6B
C7	3B	Q2	5B
C8	NOT USED	Q3	4D
C9	4B	R1	2B
C10	3B	R2	2B
C11	6A	R3	2B
C12	6B	R4	2B
C13	6B	R5	2B
C14	6D	R6	3B
C15	6D	R7	3B
C16	7D	R8	4B
C17	7D	R9	NOT USED
C18	1C	R10	2B
C19	1C	R11	6B
C20	1D	R12	6B
C21	1D	R13	6B
C22	5D	R14	3B
C23	3C	R15	5D
C24	3C	R16	6C
C25	2C	R17	4E
		R18	5E

(C-INT-1) and issues a slew com-
ense is provided by the SLEW
d sense of the overflow/underflow
TRUE in MSB at overflow). Complete
le 20 ns jitter when less than
-RST-1 minimizes limit cycling in
ng 20 ns delay in reference strobe.
ical to radiated 20 ns jitter.
ay change commences when successive
hus transient performance of com-

60, LORTO (RESET) 1

62, SHIFT DIRECTION
TRUE-TIME ADVANCE 6

66, SHIFT PULSE 10

68, MAJORITY INTERVAL 1

6

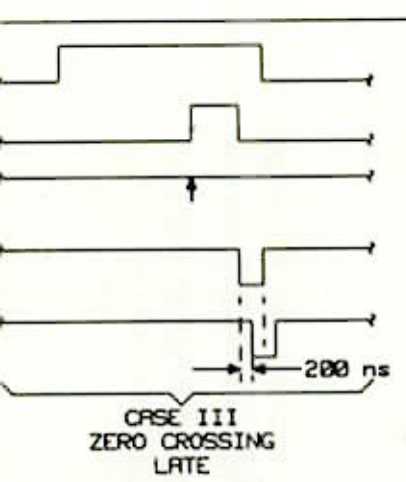
64
SHIFT DIRECTION
TRUE-TIME RETARD

TABLE I

APPROXIMATE BASIC TIME CONSTANT (960/X) - SECONDS	
BASIC RATE	LORAN C
4X00	6 sec
6X00	7 sec
7X00	9.5 sec
9X00	12 sec

TABLE II, LOOP SCALE FACTOR (N)

MULTIPLY BASIC TIME CONSTANT BY	C-RST-1 INPUTS				
	E9	E10	OR	E9	E10
1	E8	E8			
2	E8	E5		E5	E5
3	E8	E6		E6	E6
4	E5	E6			
5	E7	E8		E7	E7
6	E7	E5			
7	E7	E6			



detector
ctive
has
leading

TP1, WHITE
DERIVED
ENVELOPE

300 Ω

15
DERIVED
ENVELOPE
OUTPUT

LOOP TIME CONSTANT

Loop time constant is determined both by the sampling rate (average local RF pulses per second) and by the overflow/underflow count of C-INT-1.

time constant = $960 \frac{N}{X}$ seconds

where: X=sampling rate (see TABLE I)
N=C-INT-1 scale factor (TABLE II)

C-INT-1 scale factor (N) is determined by the wiring of jumpers between the four output turret terminals of C-INT-1 (E5, E6, E7, E8) and the two input turret terminals of C-RST-1 (E9, E10). These connections determine the overflow/underflow count of C-INT-1 and scale the loop again (K). When making these connections, both turret terminals E9 and E10 (A14 and A15 inputs) of C-RST-1 MUST be wired to one of the four available outputs of A13 in C-INT-1.

One or both input terminals of C-RST-1 may be wired to any given output of C-INT-1 (E5, E6, E7, E8), however, no two outputs of C-INT-1 may be connected together or to same C-RST-1 input. Table II gives all possible combinations of connections, which allow N to vary from 1 to 7.

W0486-10E/ERR SNS

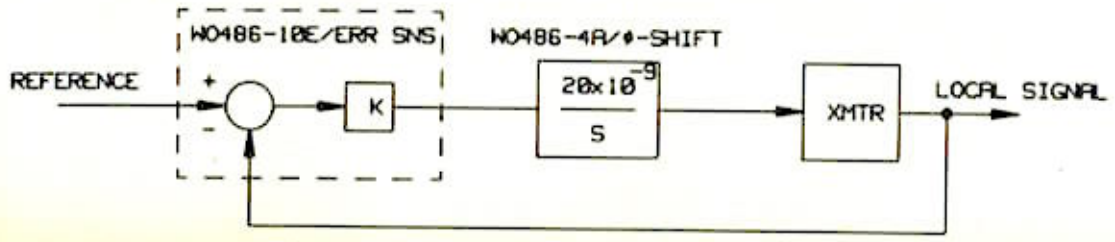
This module measures the error between an input reference waveform, derived from the DRRG majority and the local radiated ZERO CROSSING (either carrier ZERO CROSSING or envelope second derivative ZERO CROSSING). The output of the module is a slew command pulse and slew direction level to the digital phase shifter, W0486-4A/0 SHIFT. The module realizes the subtraction and gain function (K) of a TYPE 1 servo loop symbolically represented below.

C-GEN-1 develops precise REFERENCE STROBE whose leading and trailing edges are positioned in time by data from the DRRG's. C-ZC-1 generates a hard limited ZERO CROSSING of the local radiated carrier or envelope. C-SHP-1 generates two sequential count intervals whose width is equal to the time between REFERENCE STROBE leading edge and ZERO CROSSING, and ZERO CROSSING and REFERENCE STROBE trailing edge. C-INT-1 then digitally measures and scales the magnitude of the difference in these two intervals' width. When an unbalance persists in these two intervals, C-INT-1 develops a slew command to W0486-4/0 SHIFT in the direction to correct the unbalance. The complete servo loop thus maintains the radiated ZERO CROSSING positioned within 20 ns of the midpoint of the REFERENCE STROBE.

The principle feature of this module is that all measurements are made digitally; there are no analog functions (excluding the envelope deriver). This results in a system that is almost totally insensitive to temperature or line voltage fluctuations. This operation is achieved through the use of a 8 MHz clock (C-OSC-1) whose phase is random with respect to the differential intervals it is used to measure. C-INT-1 is a bipolar digital integrator (UP/DOWN counter) which performs the digital scaling function (gain K where K $<$ 1) and acts to average the differential width measured with C-OSC-1. Accurate control of the 20 ns phase shifter is provided with relative low frequency (8 MHz) digital elements by means of the noise bias introduced by the random clock phase.

P/DOWN counters.
tional sense to
SSING is to the
derflow indicates
controlled by the
nes loop time
stant is given

E8, E9, E10
NORMALLY CONNECTED



C-LSD-1: LOST SIGNAL DETECTOR

Detects loss of local signal input to C-ZC-1 and disables operation of W0486-10E/ERR SNS module. Lost signal threshold is nominally 6 dB below the normal input level.

The limited signal from C-ZC-1 R2 input (TP2) is applied to the gate of Q2 through a frequency compensated voltage divider. Q2 is connected as a source follower driving Q1's output in turn drives the input of A3 retriggerable single-shot which has approximately 100 ns runout. As long as the input signals to C-ZC-1 which exceed the threshold of C-LSD-1 occur every 100 ns or less, A3 remains in the triggered state with Pin B (LOST SIGNAL INHIBIT) TRUE.

LIMITED OPERATE RF

C-SSS RESET

TP2, ORANGE
LIMITED OPERATE RF

TP3, RED
HARD LIMITED
OPERATE RF

C-ZC-1: HARD LIMITING ZERO CROSSING DETECTOR

Hard limits LOCAL ZERO CROSSING INPUT signal to produce phase rise time, TTL level waveform. The LOCAL ZERO CROSSING INPUT may be either a direct RF local signal for phase lock operation of a demodulated and derived envelope (from C-ENV-1) for envelope lock operation. Phase code (PC and $\overline{PC}$) inputs are provided for phase-decoding phase-coded signals. Nominal input level is 15 Vp-p into 300 ohms. These signals are reclocked for SSX transmitter by 200 us by A18B.

Diodes CR2 through CR7 and R8 limit the comparator, A2 input to approximately 4 Vp-p. This signal is hard limited and converted to TTL levels by A2, a high-speed comparator. Approximately 10 mV positive feedback is supplied via R5 to ensure sharp transitions at the output of the comparator. A1A and A1B select either non-inverted or inverted comparator output according to the levels on PC and $\overline{PC}$ inputs. For positive coded signals, with PC TRUE and PC FALSE, lock will occur on the positive-going ZERO CROSSINGS of the input signal. For operation with C-ENV-1 output, putting PC FALSE and $\overline{PC}$ TRUE will cause lock to occur on the first (negative-going) ZERO CROSSING of C-ENV-1 output.

OPERATE RF

PHASE CODE

ure 7.18. W0486-10E/ERR SNS Block Diagram

?/7.38

occurs. This minimizes hunting of servo loop with errors less than 20 ns.

RETARD REF STROBE

ADVANCE REF STROBE

REFERENCE STROBE

REFERENCE STROBE (INVERTED)

C-SSS-1: SLEW SPEEDUP SERVO

Bypasses C-INT-1 and provides high speed slew (GRR μs/s) when ZERO CROSSING is entirely outside of REFERENCE STROBE (1.5 μs error to within 1.5 μs). C-SSS-1 is inoperative when ZERO CROSSING is within REFERENCE STROBE and has no effect on loop transient response for errors of less than ± 1.5 μs.

Two D-flip flops A10A and A10B are clocked at the leading and trailing edges of the REFERENCE strobe, respectively. The D-inputs of both flip flops are connected to the ZERO CROSSING signal. A10A output (Q) is TRUE or FALSE according to the level of ZERO CROSSING at the time of the REFERENCE STROBE leading edge. Similarly, A10B (Q) output is the level of ZERO CROSSING at the time of the REFERENCE STROBE trailing edge.

With the ZERO CROSSING (FALSE-going) with the REFERENCE STROBE, A10A (Q) output is FALSE and A10B (Q) output is TRUE.

If the ZERO CROSSING occurs earlier than REFERENCE STROBE, both A10A and A10B (Q) outputs are FALSE, A10A (Q) output is TRUE and A10A (Q) is FALSE. This forces A17A and A17B (in C-RST-1) to the RESET state indicating a SLEW DIRECTION to cause timing retardation. 200 ns after A10A (Q) goes TRUE, this state change SETS A10A and RESETS A10B through A11A, B, D and Z4. This pulse also sets A10A in (C-RST-1) and generates a SLEW COMMAND.

Operation is similar when ZERO CROSSING occurs later than REFERENCE strobe. C-SSS-RESET (Pin 10) input is provided for module testing purposes only.

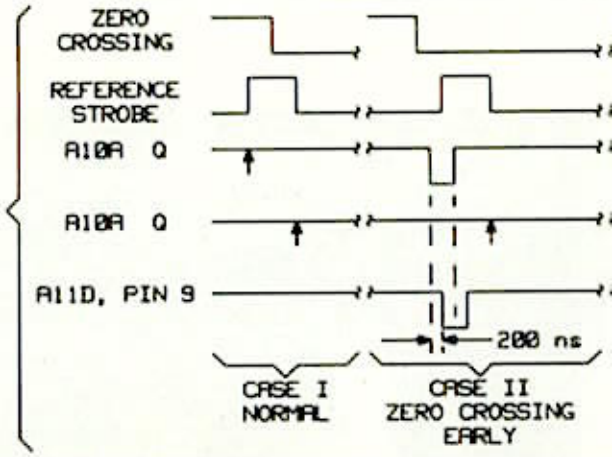
SLEW

ADVANCE

RETARD

C-RST-1 INTEGRATOR RESET

Reset logic detects overflow of mand pulse to phase shifter. Slew s DIRECTION output which is the store (e.g. Overflow is characterized by servo loop would normally limit cyc 20 ns error exists in loop. Limit C radiated signal by adding or remov This creates input to C-INT-1 ident Application of reference strobe de overflows are of different sense, t plete loop is unaffected.



C-ENV-1: ENVELOPE DETECTOR AND DRIVER

Demodulates and filters envelope of LOCAL SIGNAL input pulse using diode and L-C filter. Filtered envelope is applied to two identical broadband a derivers in cascade to generate second derivative of envelope (TP1) which negative-going ZERO CROSSING corresponding to the inflection point on the edge of the envelope.

Nominal input level is 11.5 V ZERO to peak into 50 ohm load.

50 Ω

LOCAL SIGNAL

TP4, BLUE
REFERENCE SELECT GATE

C-GEN-1: REFERENCE SELECT GATE GENERATOR

The PMPT8 signal from the PC/MPT module is retimed by the 100 kHz strobes from the DRRG majority to generate the Reference Select Gate. The Reference Select Gate is reclocked by the system 5 MHz clock to form the Reference Strobe. The final reclocking eliminates all temperature sensitive perturbations in the reference strobe's time position except those present in the 5 MHz clock.

MPT

TROBE INHIBIT

SYSTEM CLOCK

JORITY STROBE

SYSTEM CLOCK
RETURN

C-OSC-1: ASYNCHRONOUS OSCILLATOR

Delay line oscillator generates clock pulses at an approximately 8 MHz rate. Ideally, this oscillator output has random timing with respect to the loran time base.

TP5, YELLOW
REFERENCE STROBE

C-SHP-1: ZERO CROSSING SENSOR

Senses position of signal zero crossing, gates pulses from C-OSC-1 as either UP counts or DOWN counts during the time of the reference strobe. With the PC input line TRUE and PC input FALSE, DOWN counts are generated during coincidence of the reference strobe (TP5) with TRUE state of ZERO CROSSING (TP3). UP counts are generated when reference strobe coincides with FALSE ZERO CROSSING level. DOWN count waveform is delayed 100 ns with respect tp UP count waveform to ensure no overlap.
REFERENCE STROBE by C-RST-1, if C-INT-1

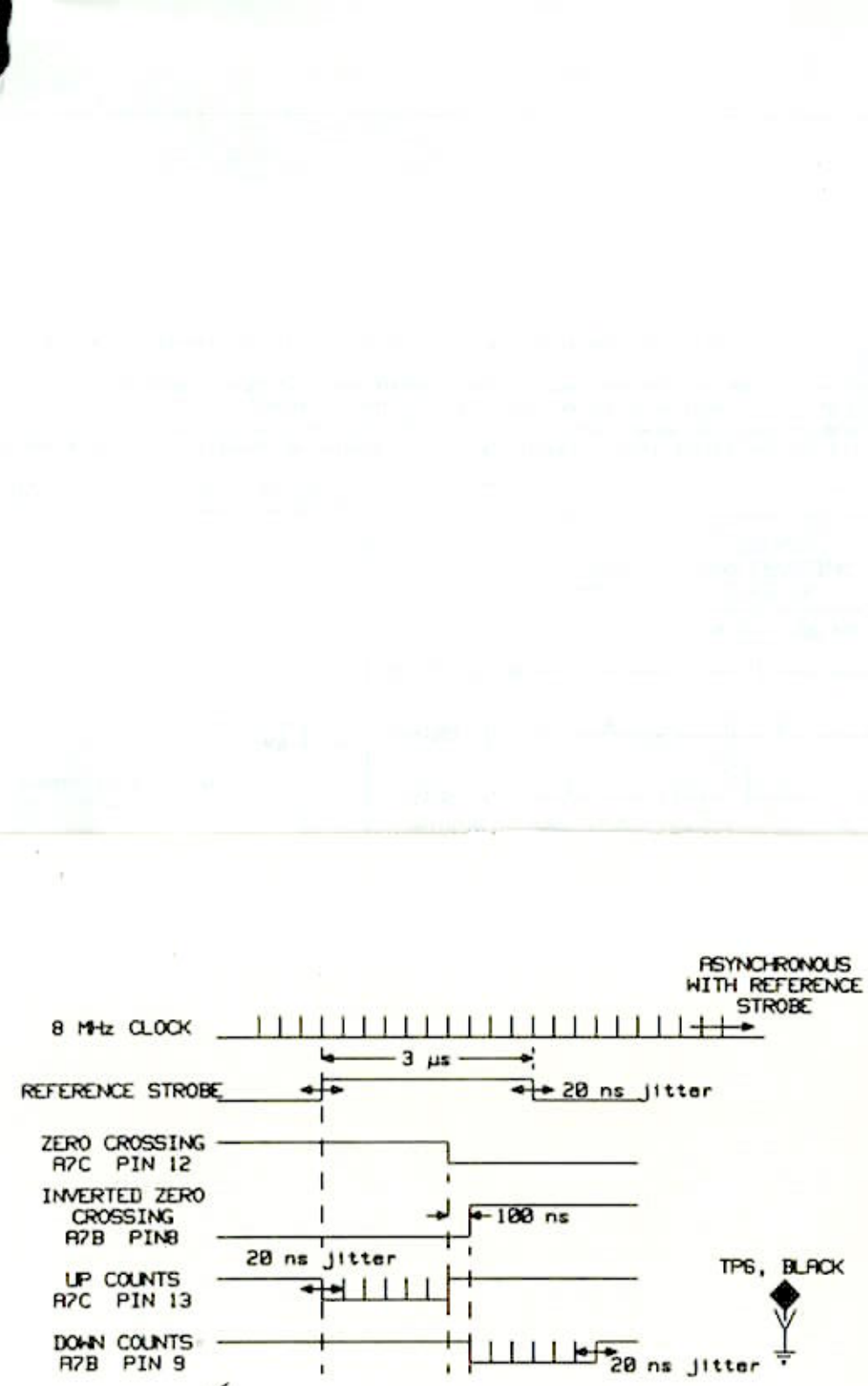
COUNT DOWN

COUNT UP

C-INT-1: DIGITAL INTEGRATOR

Bipolar digital integrator formed with three U
Counters are reset to 1/2 capacity, giving direc
error signal. Overflow indicates signal ZERO CRO
right (later in time) of strobe mid-position; un
left error. Total counter length is variable and
outputs wired to C-RST-1. Counter length determi
constant by changing the loop gain (k). Time con
in Tables I and II.

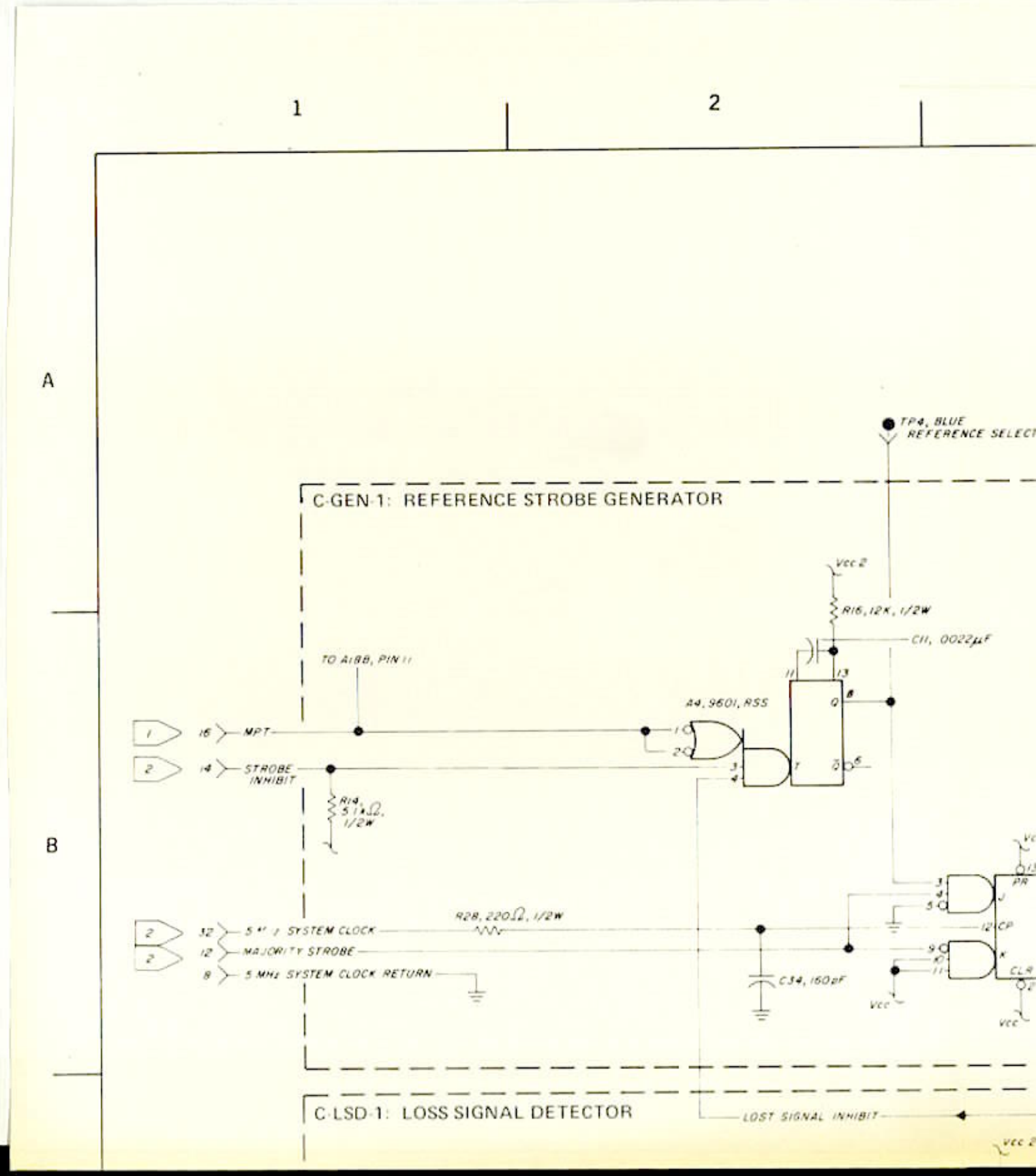
ASYNCHRONOUS
WITH REFERENCE
STROBE





Figu
7.37

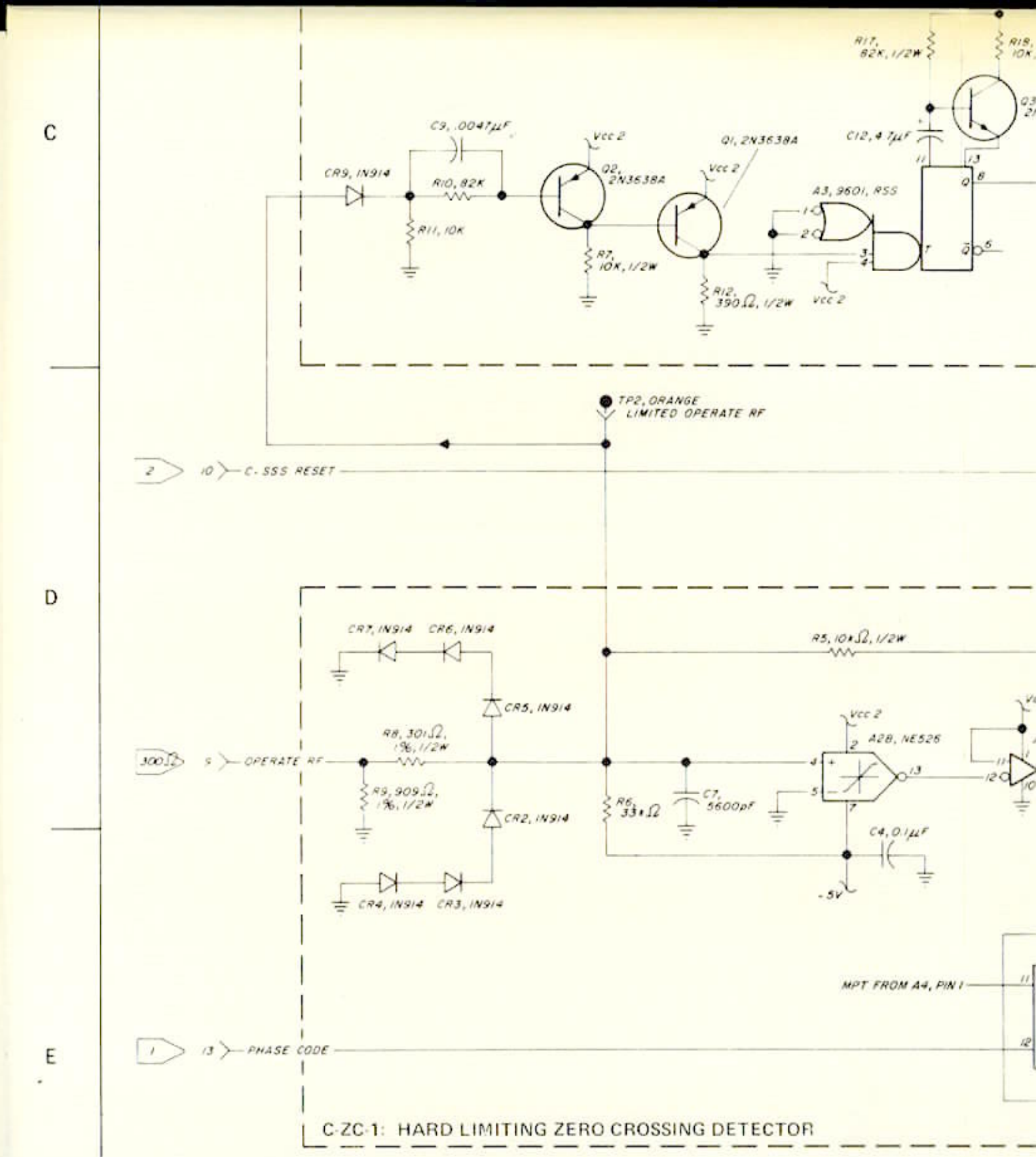

1
16
2
14
S
SMH
2
32
MF
2
12
8
SMH



1
2
A
B
TP4, BLUE
REFERENCE SELECT
C-GEN-1: REFERENCE STROBE GENERATOR
Vcc 2
R16, 12K, 1/2W
C11, .0022μF
TO A18B, PIN 11
A4, 9601, RSS
16 MPT
14 STROBE INHIBIT
R14, 5.1kΩ, 1/2W
32 5 MHz SYSTEM CLOCK
12 MAJORITY STROBE
8 5 MHz SYSTEM CLOCK RETURN
R28, 220Ω, 1/2W
C34, 160pF
Vcc
C-LSD-1: LOSS SIGNAL DETECTOR
LOST SIGNAL INHIBIT

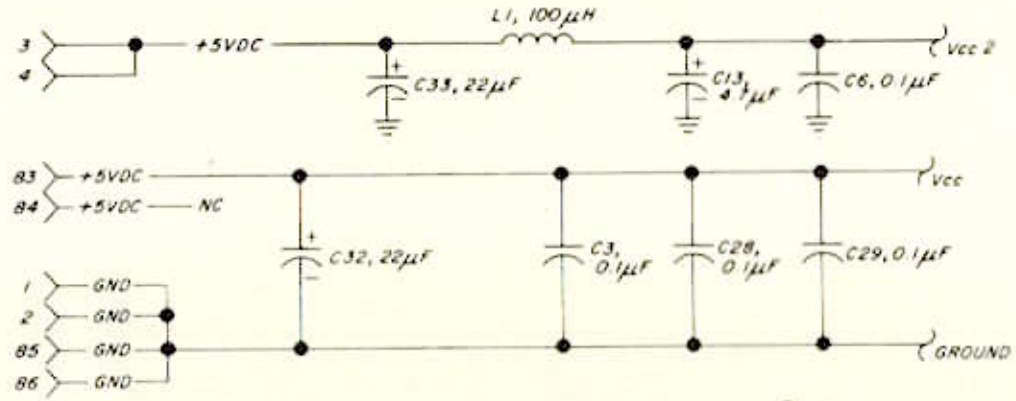
PART LOCATION INDEX

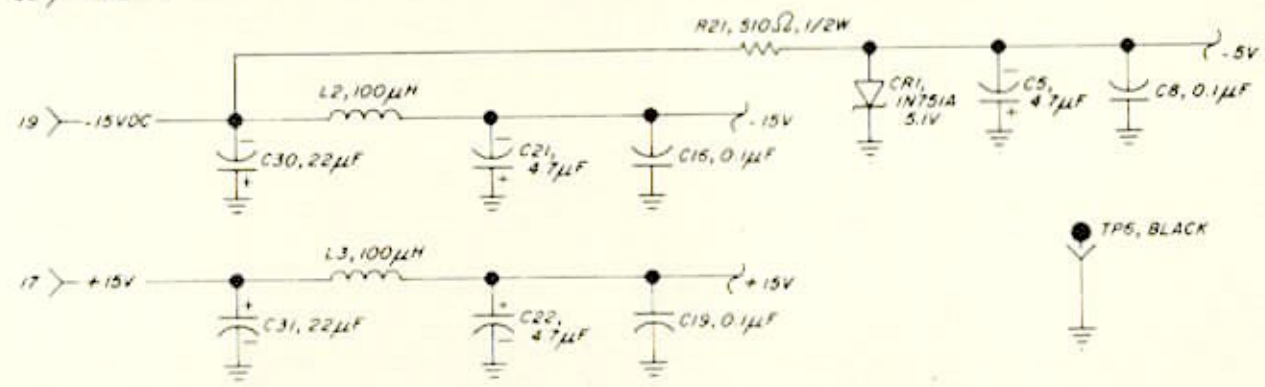
REF.DESIG.	LOCATION	REF.DESIG.	LOCATION	REF.DESIG.	LOCATION
A1A	3D	C12	2C	L1	6A
A1B	4D	C13	7A	L2	6A
A2A	3D	C14	NOT USED	L3	6B
A2B	2D	C15	NOT USED	L4	5E
A3	2C	C16	6A		
A4	2B	C17	7E	Q1	2C
A5	NOT USED	C18	7E	Q2	2C
A6	6B	C19	6B	Q3	3C
A7A	5B	C20	6E		
A7B	5B	C21	6A	R1	4C
A7C	5B	C22	6B	R2	5A
A8A	7D	C23	6E	R3	4B
A8B	4B	C24	6E	R4	5A
A9	3B	C25	6E	R5	2D
A10A	4D	C26	5E	R6	2D
A10B	4C	C27	5E	R7	2C
A11A	3C	C28	7A	R8	1D
A11B	4C	C29	7A	R9	1D
A11C	4D	C30	6A	R10	1C
A11D	4D	C31	6B	R11	1C
A12	7B	C32	6A	R12	2C
A13	7B	C33	6A	R13	NOT USED
A14A	6C	C34	2B	R14	1B
A14B	6C	C35	5B	R15	NOT USED
A15A	6C	C36	6B	R16	2B
A15B	8D			R17	2C
A16A	5C	CR1	7A	R18	3C
A16B	6C	CR2	1D	R19	3D
A16C	8D	CR3	1E	R20	4C
A16D	4C	CR4	1E	R21	7A
A17A	7D	CR5	1D	R22	7E
A17B	7D	CR6	1D	R23	7E
A18A	7C	CR7	1D	R24	6E
A18B	3E	CR8	5E	R25	6E
A19	7E	CR9	1C	R26	6E
A20	6E			R27	5E
A21	5B	E1	NOT SHOWN	R28	1B
A22	6B	E2	NOT SHOWN		
		E3	NOT USED	TP1	7E
C1	NOT USED	E4	NOT USED	TP2	2D
C2	4B	E5	7B	TP3	3D
C3	6A	E6	7B	TP4	2A
C4	2E	E7	8B	TP5	3B
C5	7A	E8	8B	TP6	7A
C6	7A	E9	7B		
C7	2D	E10	7B	Z1	4C
C8	7A	E11	NOT SHOWN	Z2	5A
C9	1C	E12	NOT SHOWN	Z3	3B
C10	NOT USED	E13	NOT SHOWN	Z4	3C
C11	2B				

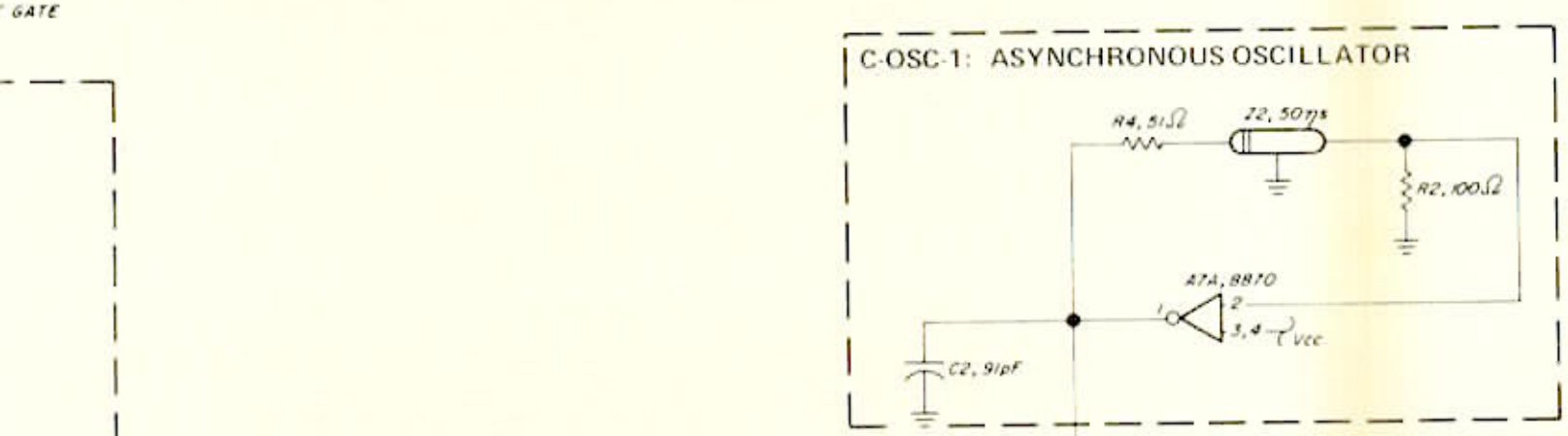


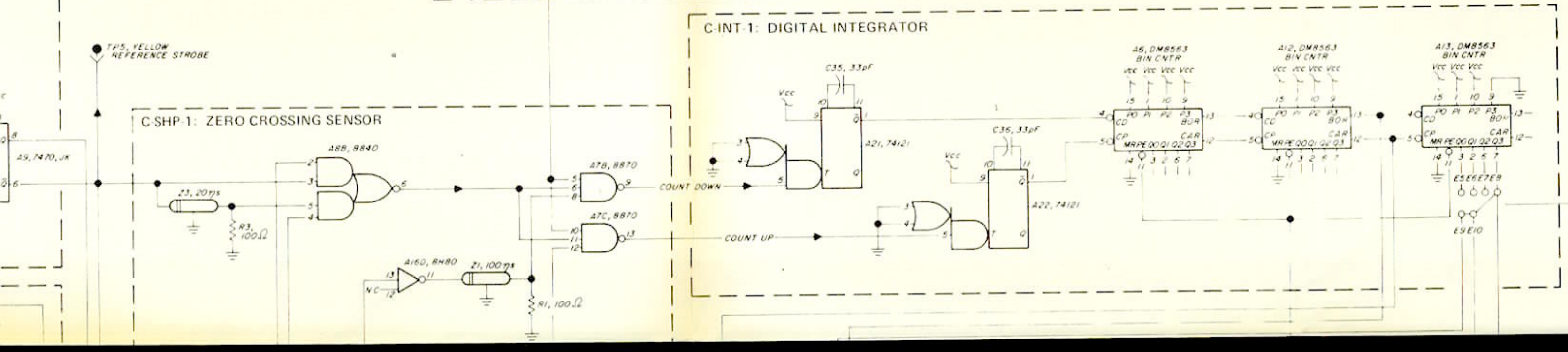
C-ZC-1: HARD LIMITING ZERO CROSSING DETECTOR

3 4 5 6 7


L1, 100µH
3
4
+5VDC
C33, 22µF
C13, 4.7µF
C6, 0.1µF
Vcc 2
83
84
+5VDC
+5VDC
NC
C32, 22µF
C3, 0.1µF
C28, 0.1µF
C29, 0.1µF
Vcc
1
2
85
86
GND
GND
GND
GND
GROUND


R21, 510Ω, 1/2W
-5V
19
-15VDC
L2, 100µH
C30, 22µF
C21, 4.7µF
C16, 0.1µF
-15V
CR1, IN751A 5.1V
C5, 4.7µF
C8, 0.1µF
17
+15V
L3, 100µH
C31, 22µF
C22, 4.7µF
C19, 0.1µF
+15V
TP6, BLACK


C-OSC-1: ASYNCHRONOUS OSCILLATOR
R4, 51Ω
Z2, 50ns
R2, 100Ω
A7A, 8870
1
2
3, 4
Vcc
C2, 91pF


C-INT-1: DIGITAL INTEGRATOR
C-SHP-1: ZERO CROSSING SENSOR
TP5, YELLOW REFERENCE STROBE
A9, 7470, JK
A8B, 8840
Z3, 20ns
R3, 100Ω
A7B, 8870
A7C, 8870
COUNT DOWN
COUNT UP
A16D, 8H80
Z1, 100ns
R1, 100Ω
C35, 33pF
A21, 74121
A22, 74121
A6, DM8563 BIN CNTR
A12, DM8563 BIN CNTR
A13, DM8563 BIN CNTR
Vcc Vcc Vcc Vcc
MR PE Q0 Q1 Q2 Q3
CD
CP
PE
CAR
BOR

RETARD REFERENCE STROBE
ADVANCE REFERENCE STROBE
REFERENCE STROBE
REFERENCE STROBE (INVERTED)

C-SSS-1: SLEW SPEEDUP SERVO

A11A, 8885
A11B, 8885
24, 200Ω
R20, 100Ω
Vcc
R19, 5.1kΩ
A11C, 8885
A11D, 8885
A10B, 7474
A10A, 7474

TP3, RED
HARD LIMITED OPERATE RF

A1A, 8840
A1B, 8840
A18B, 7474, OFF

C-RST-1: INTEGRATOR R

RESET
A14A, 7425
A14B, 7425
A15B, 8H80
A16A, 8H80
A15A, 8816
A18A, 7474, OFF
SLEW
ADVANCE
RETARD
A17B, 7474, OFF
A8A, 8840
A16C, 8H80
A17A, 7474, OFF

C-ENV-1: ENVELOPE DETECTOR AND DRIVER

50Ω
LOCAL SIGNAL
CR8, IN277
L4, 1000μH
C27, 220pF
C26, 0.01μF
R27, 51Ω, 1/2W
R26, 510Ω, 1/2W
C25, 1000pF
C24, 82pF
R25, 15kΩ, 1/2W
C23, 150pF
R24, 13kΩ, 1/2W
A20, LM301
C20, 1000pF
C18, 82pF
R23, 15kΩ, 1/2W
C17, 150pF
R22, 13kΩ, 1/2W
A19, LM301
+15V
-15V
TP1, WHITE
DERIVED ENVELOPE
15
300Ω
DERIVED ENVELOPE OU

Figure 7.19. W0486-10E

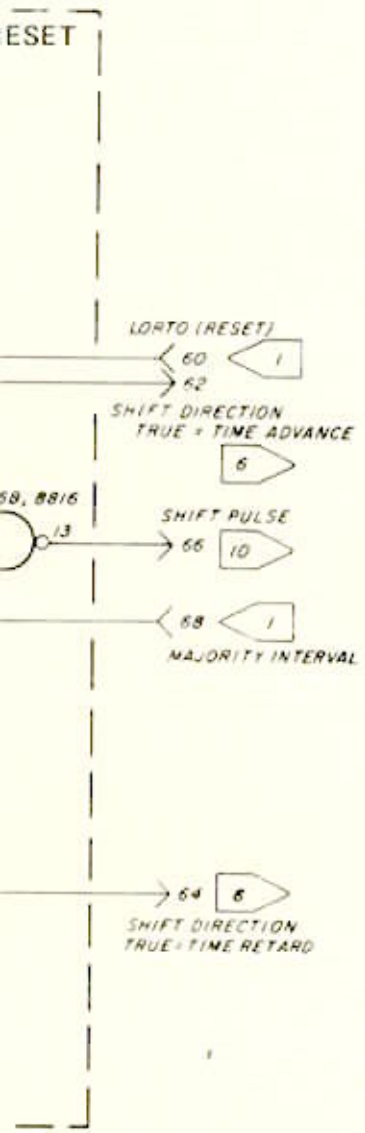
3 4 5 6 7

8

A

B

E8, E9, E10
NORMALLY CONNECTED



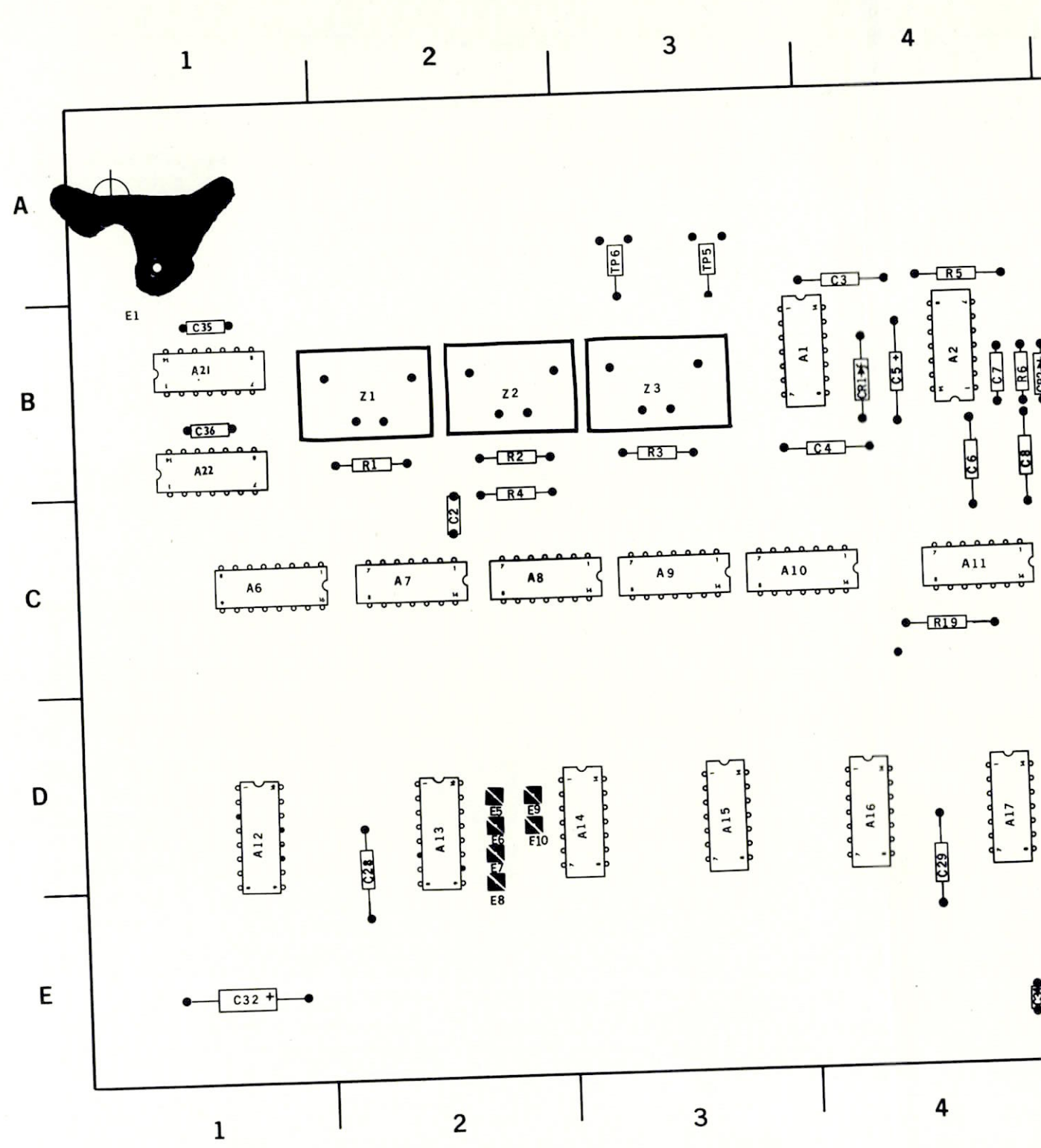
ITPUT

E/ERR SNS Schematic Diagram

7.39/7.40

PART LOCATION INDEX

REF.DESIG.	LOCATION	REF.DESIG.	LOCATION	REF.DESIG.	LOCATION
A1	4B	C22	7D	Q1	5B
A2	4B	C23	6D	Q2	5B
A3	6B	C24	6D	Q3	6C
A4	6B	C25	6D		
A5	NOT USED	C26	6D	R1	2B
A6	1C	C27	6E	R2	2B
A7	2C	C28	2D	R3	3B
A8	2C	C29	4D	R4	2C
A9	3C	C30	5E	R5	4A
A10	3C	C31	5E	R6	4B
A11	4C	C32	1E	R7	5A
A12	1D	C33	7E	R8	5B
A13	2D	C34	4E	R9	5B
A14	3D	C35	1B	R10	5B
A15	3D	C36	1B	R11	5B
A16	4D			R12	5A
A17	4D	CR1	4B	R13	NOT USED
A18	5D	CR2	4B	R14	6B
A19	6C	CR3	5B	R15	NOT USED
A20	6D	CR4	5B	R16	6B
A21	1B	CR5	5B	R17	6C
A22	1B	CR6	5B	R18	6C
		CR7	5B	R19	4C
C1	NOT USED	CR8	6E	R20	5C
C2	2C	CR9	5B	R21	5C
C3	4A			R22	6C
C4	4B	E1	1A	R23	6C
C5	4B	E2	7A	R24	6D
C6	4B	E3	7B	R25	6D
C7	4B	E4	7C	R26	6D
C8	4B	E5	2D	R27	6E
C9	5B	E6	2D	R28	5E
C10	NOT USED	E7	2D		
C11	6B	E8	2D	TP1	6A
C12	6B	E9	2D	TP2	6A
C13	7C	E10	2D	TP3	5A
C14	NOT USED	E11	NOT SHOWN	TP4	5A
C15	NOT USED	E12	NOT SHOWN	TP5	3A
C16	6C	E13	NOT SHOWN	TP6	3A
C17	6C				
C18	6C	L1	7B	Z1	2B
C19	7C	L2	6D	Z2	2B
C20	6C	L3	7D	Z3	3B
C21	6D	L4	6D	Z4	5C



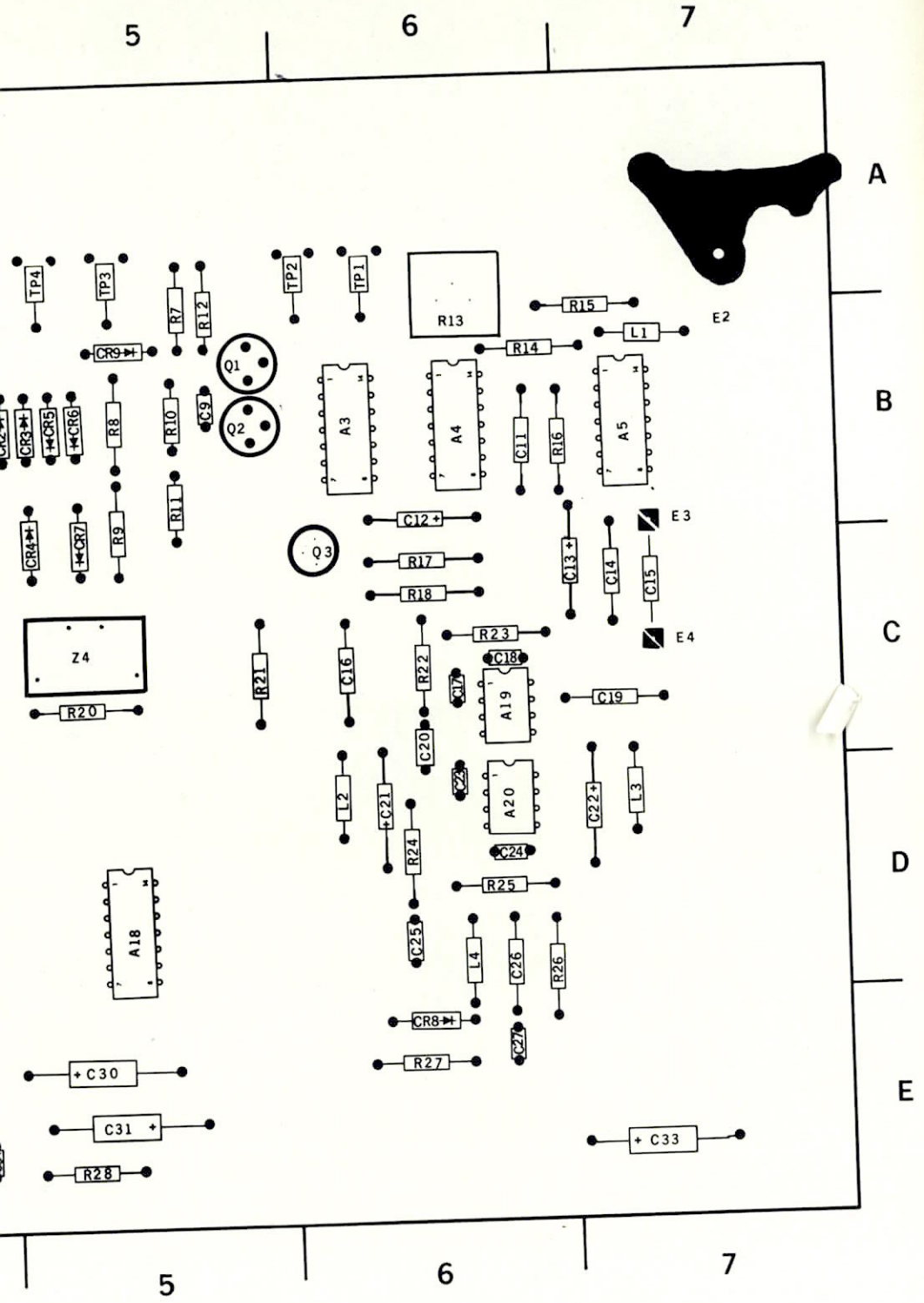


Figure 7.20. W0486-10E/ERR SNS Parts Locator

100 ns LATE STROBE → 48 [8]

TP-1, BROWN
100 ns STROBE

[10]

→ 6

DELAYED 100 ns
FALSE STROBE

DELAYED 100 ns
TRUE STROBE

→ 8

[9]

[10]

→ 16

DELAYED VARIABLE
WIDTH TRUE STROBE

DELAYED VARIABLE
WIDTH FALSE STROBE

→ 14

[10]

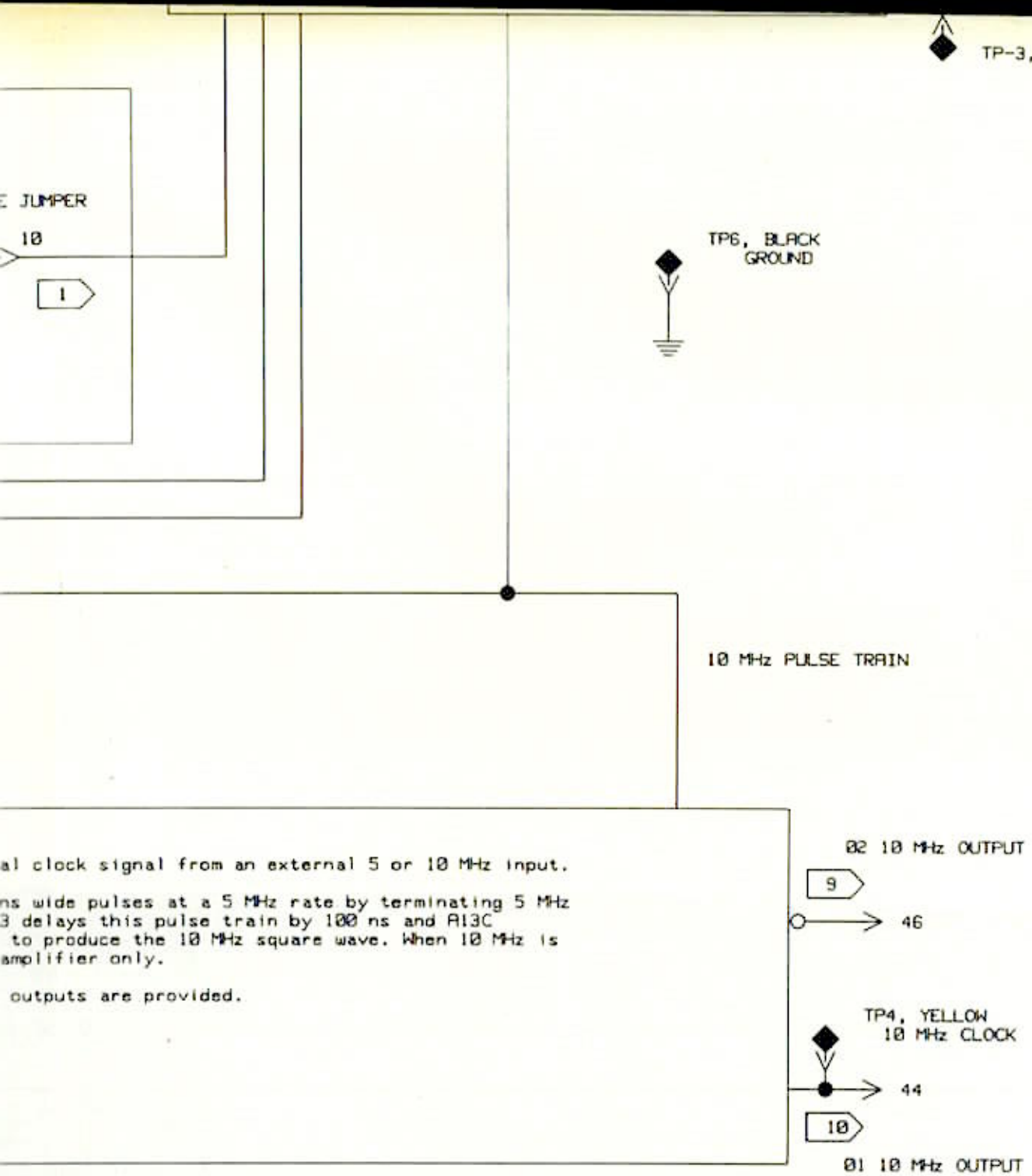
L-RSG-1: RECLOCK STROBE GENERATOR

Conventional JK flip-flop is enabled at L-CNTR-1 state 97 and toggled by the next internal clock pulse to produce the leading edge of the delayed strobe concurrently with L-CNTR-1 state 98. The trailing edge of the strobe is determined by the outputs of L-CNTR-1 selecting as K enabling inputs to the JK flip-flop, and may be set to provide any strobe width from 0.1 to 9.9 us by connecting FINE and COARSE STROBE WIDTH INPUTS to the appropriate outputs of L-CNTR-1. Both TRUE and FALSE delayed strobe outputs are available.

JUMPER

12

[1]



JSTMENT CONTROL

delayed from a majority 100 KHz reference input. Two sets of 9's complement BCD inputs designated
e delay through two decades in 0.1 us increments.

MHz internal clock signal from an external 5 or 10 MHz source to provide the 0.1 us resolution.

r preset pulse synchronous with the internal clock and occurring immediately after the leading edge
ry 10 us, L-CNTR-1 is preset to the 9's complement of the delay setting selected from either LOCAL
L-CNTR-1 counts up at the 10 MHz internal clock rate. Selected outputs of L-CNTR-1 arm L-RSG-1 J
trailing edge of the delayed strobe synchronous with the internal clock.

LOCAL/REMOTE INPUT 50

LOC MSD 8 54

REM MSD 8 52

LOC MSD 4 56

REM MSD 4 58

LOC MSD 2 62

REM MSD 2 60

LOC MSD 1 64

REM MSD 1 66

L-GAT-1: LOCAL/REMOTE SELECT GATE

Eight AND-OR-INVERT gates act as an eight-pulse, double-throw switch. The 9's complement of the strobe delay in BCD format is selected from the LOC inputs when the LOCAL/REMOTE input is HIGH or from the REM inputs when LOW in Loran-C Timer application, the LOC inputs are connected to a front panel ETA switch.

L-CNTR-1: PRESET COUNTER

Two conventional BCD counters are preset to the 9's complement of the desired delay in micro-seconds and tenths immediately following the falling edge of the majority 100 KHz reference, and count up at the internal 10 MHz rate. Decimal counter state 98 defines the termination of the delay, and the leading edge of the delayed strobe.

COARSE STROBE WIDTH CONTROL

10

USEC

9 23

8 21

7 15

6 17

5 19

4 33

3 31

2 29

1 27

0 25

10

9

BACKPLANE

COARSE STROBE START

LOC LSD 8
70
REM LSD 8
68
LOC LSD 4
72
REM LSD 4
74
LOC LSD 2
78
REM LSD 2
76
LOC LSD 1
80
REM LSD 1
82

FINE STROBE
WIDTH CONTROL
10
USEC
700 43
600 41
500 35
400 37
300 39
200 53
100 51
000 49
900 47
800 45
9
10
BACKPLANE
FINE STROBE START

TP-5, GREEN
PRESET PULSE
COUNTER PRESET PULSE

L-GEN-1: 10 MHz GENERATOR/BUFFER

Generates or buffers the 10 MHz intern

A13A, B and Z2 generate a train of 50
square wave 50 ns after the falling edge. Z
NOR's the original and delayed pulse trains
available, L-GEN-1 may be used as a buffer

In-phase (01) and inverted (02) 10 MHz

L-MAJ-1: MAJORITY GATE AND PRESET PULSE GENERATOR

100 KHz majority pulse generated by A8 is inverted and terminated 150 ns from the leading edge by Z, A10B and A10C. JK flip-flop A11B reclocks both leading and trailing edges of this pulse to the internal 10 MHz clock. The resulting counter preset pulse (available at TP 5) is a 100 ns wide LO pulse synchronous with the 10 MHz internal clock and occurring immediately after the leading edge of the majority 100 KHz.

7
73
69

C-ETA-1: ENVELOPE TIMING ADJU

Generates a variable width strobe
LOCAL and REMOTE, externally adjust th

L-GEN-1 generates or buffers a 10

L-MAJ-1 generates a 0.1 us counte
of the majority 100 KHz reference. Eve
or REMOTE external sources by L-GAT-1.
or K inputs to generate the leading or

10 MHz INPUT (USED IF 10 MHz AVAILABLE; OTHERWISE, TIED HIGH)
16
5 MHz INPUT (IF 10 MHz INPUT USED, TIE HIGH)
20

TP-2, RED
5 MHz INPUT

re 7.21. W0486-11/ETA Block Diagram
/7.44

[2]

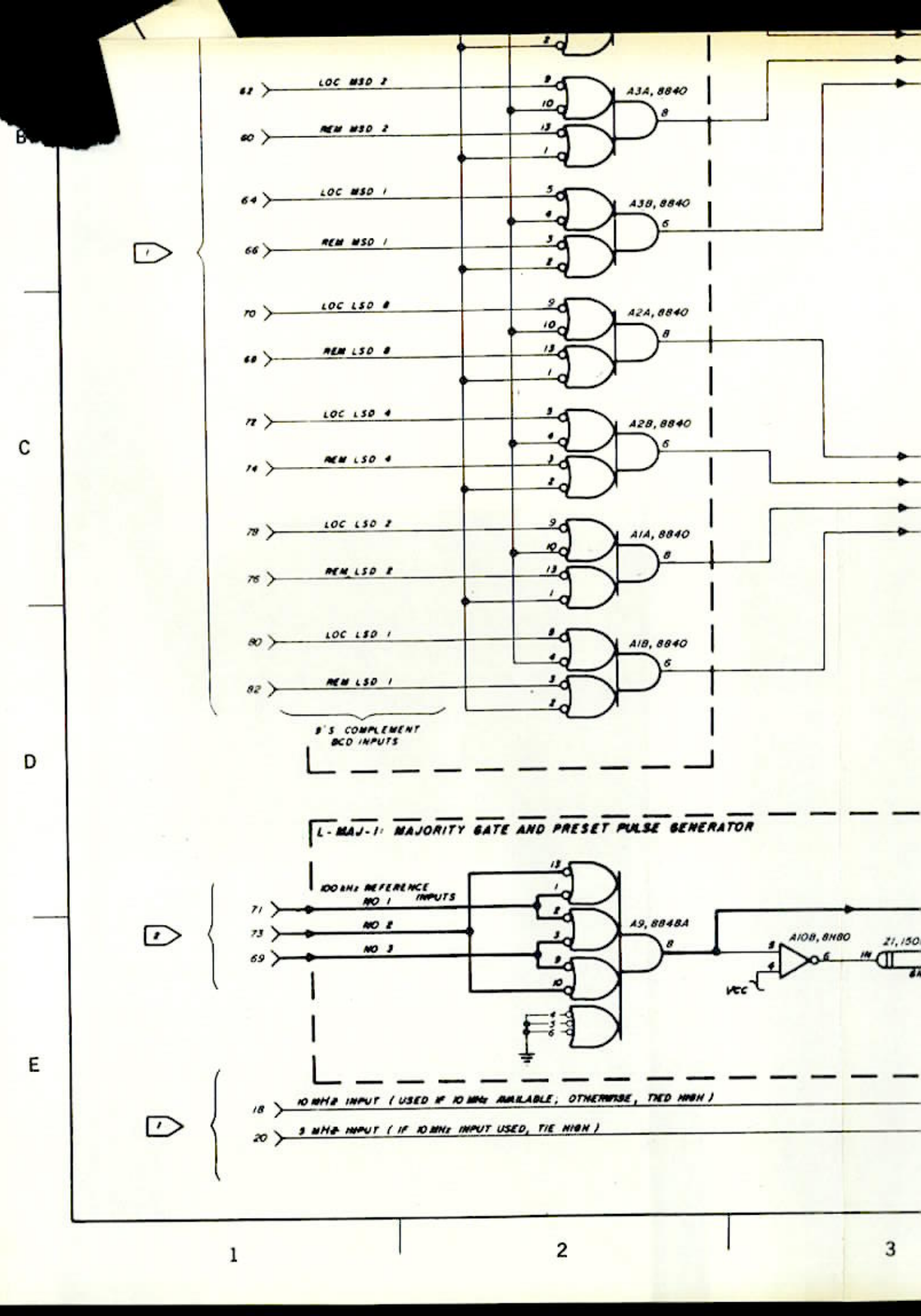
[1]

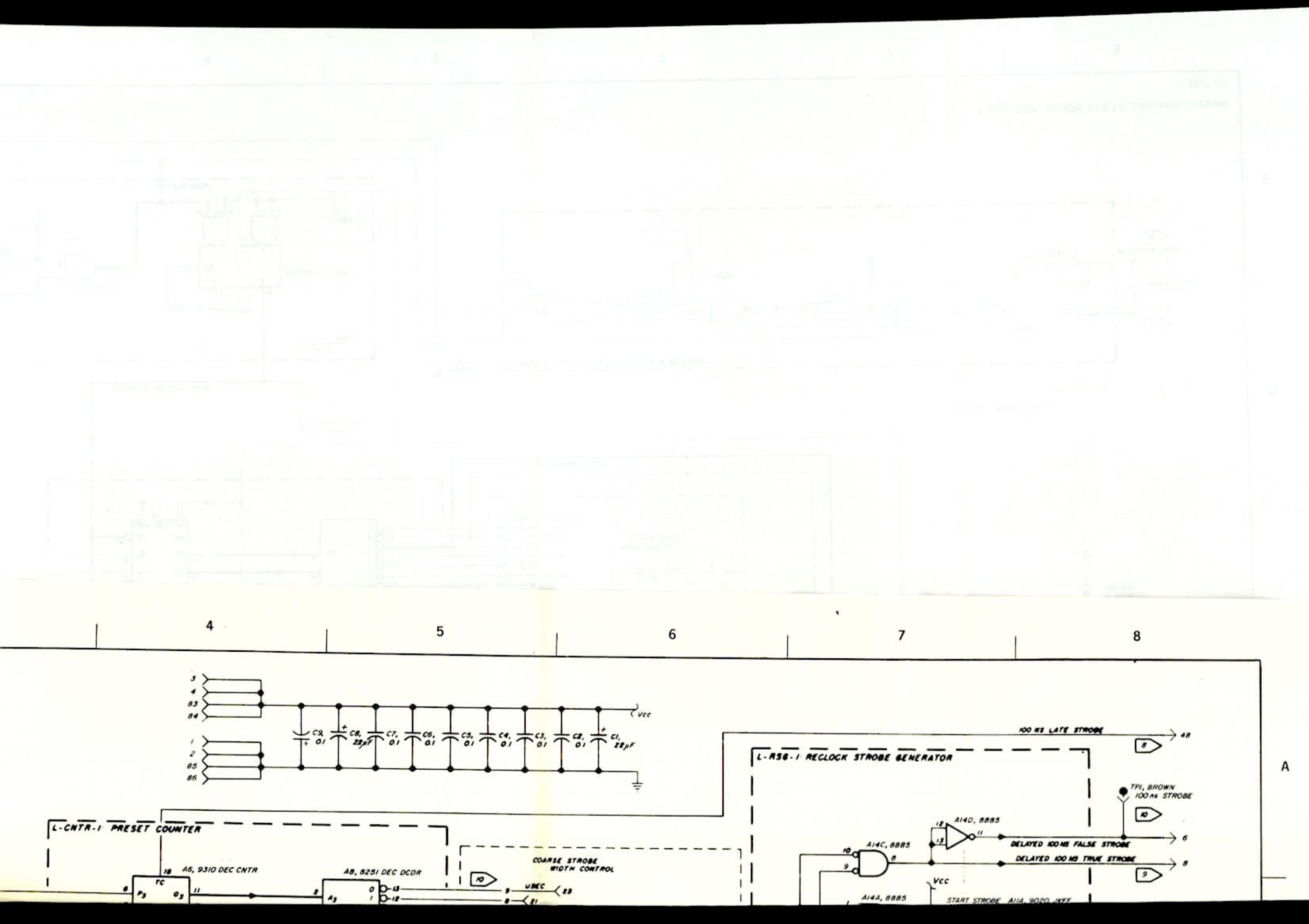
Figu
7.43


2
3
AL/REMOTE SELECT GATE
A12B, 8880
A4A, 8840
A4B, 8840
LOC MSD 4

PART LOCATION INDEX

REF. DESIG.	LOCATION	REF. DESIG.	LOCATION
A1A	2C	C1	6A
A1B	2D	C2	6A
A2A	2C	C3	5A
A2B	2C	C4	5A
A3A	2B	C5	5A
A3B	2B	C6	5A
A4A	2A	C7	5A
A4B	2B	C8	5A
A5	4C	C9	4A
A6	4B	C10	4E
A7	5C		
A8	5B	E1	NOT SHOWN
A9	2E	E2	NOT SHOWN
A10A	7D		
A10B	3E	R1	3E
A10C	4E	R2	6E
A10D	8E	R3	7E
A11A	7B		
A11B	4E	TP1	8A
A12A	1A	TP2	5D
A12B	2A	TP3	8B
A13A	6D	TP4	8D
A13B	5D	TP5	4D
A13C	7D	TP6	8C
A14A	7B		
A14B	7B	Z1	3E
A14C	7A	Z2	6D
A14D	7A	Z3	7D




4
5
6
7
8
A
3
4
83
84
1
2
85
86
C9, 0.1
C8, 22µF
C7, 0.1
C6, 0.1
C5, 0.1
C4, 0.1
C3, 0.1
C2, 0.1
C1, 22µF
Vcc
100 NS LATE STROBE
48
L-RSG-1 RECLOCK STROBE GENERATOR
TP1, BROWN
100 ns STROBE
A14D, 8885
A14C, 8885
A14A, 8885
DELAYED 100 NS FALSE STROBE
DELAYED 100 NS TRUE STROBE
START STROBE A11A, 9ORD, IKEE
L-CNTR-1 PRESET COUNTER
A6, 9310 DEC CNTR
A8, 8251 DEC DCDR
COARSE STROBE
WIDTH CONTROL
USEC

BACKPLANE JUMPER
COARSE STROBE WIDTH INPUT
COARSE STROBE START
A148, 8885
STOP STROBE
DELAYED VARIABLE WIDTH TRUE STROBE
DELAYED VARIABLE WIDTH FALSE STROBE
TP3, ORANGE
TP6, BLACK GROUND
A5, 9310 DEC CNTR
A7, 8251 DEC DCDR
FINE STROBE WIDTH CONTROL
BACKPLANE JUMPER
FINE STROBE WIDTH INPUT
FINE STROBE START
TP5, GREEN PRESET PULSE
COUNTER PRESET PULSE
10 MHz PULSE TRAIN
TP2, RED 5 MHz INPUT
L-GEN-1 10 MHz GENERATOR / BUFFER
A13B, 8H70
A13A, 8H70
A13C, 8H70
A10A, 8H80
A10D, 8H80
A10C, 8H80
A11B, 9020, JKFF
Z2, 50ns
Z3, 100ns
R1, 100Ω
R2, 100Ω
R3, 100Ω
C10, 22pF
100 ns
NO CONNECTION
Vcc
GND
TP4, YELLOW 10 MHz CLOCK

Figure 7.22. W0486-11/ETA Schematic Diagram

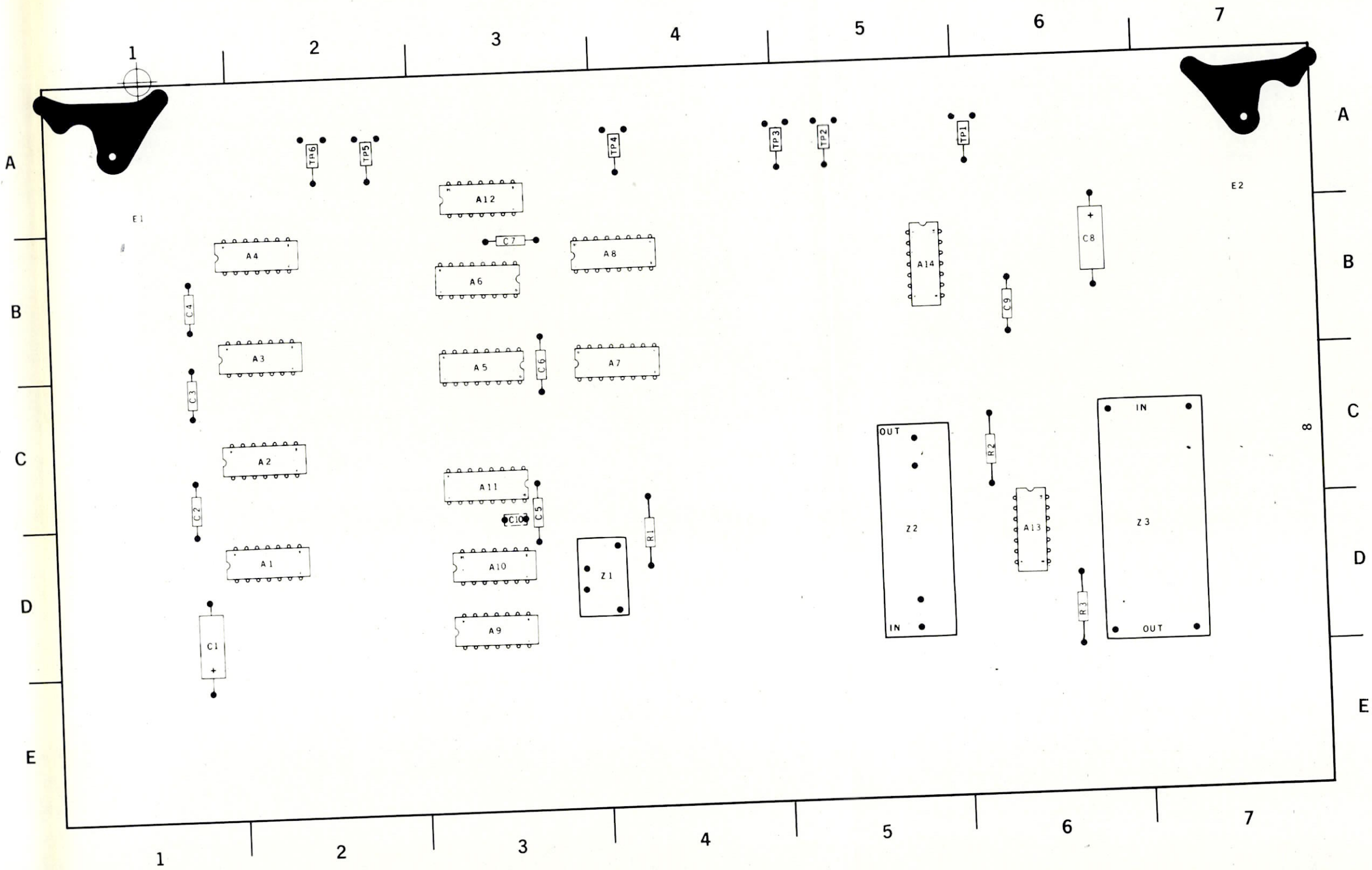
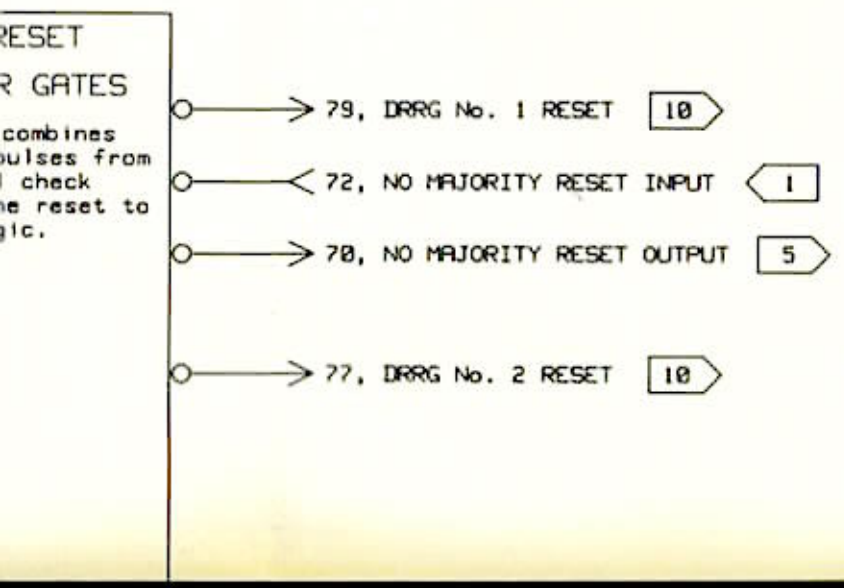


Figure 7.23. W0486-11/ETA Parts Locator

PART LOCATION INDEX	
REF. DESIG.	LOCATION
A1	2D
A2	2C
A3	2B
A4	2B
A5	3B
A6	3B
A7	4B
A8	4B
A9	3D
A10	3D
A11	3C
A12	3A
A13	6D
A14	5B
C1	1D
C2	1C
C3	1C
C4	1B
C5	3C
C6	3B
C7	3B
C8	6B
C9	6B
C10	3D
E1	1A
E2	7A
R1	4D
R2	6C
R3	6D
TP1	6A
TP2	5A
TP3	5A
TP4	4A
TP5	2A
TP6	2A
Z1	3D
Z2	5D
Z3	7D

W0486-12A/CONTROL

Control module designed specifically for majority type control of three DRRG's or three phase shifters. All of the logic necessary for this control and status display is included on this module. The basic concept of the module is the comparison of d.c. signals representing the agreement of one pair of the three controlled units. In addition, external reset logic is provided to synchronize the controlled units to either an external pulse signal, an external phase shifter, or both.



75, DRRG No. 3 RESET 10

C-ALM-2: MALFUNCTION ALARM

Actuates the output lamp driver if any abnormal (i.e., malfunction) condition exists among the on-card or external check logic elements.

A1-6
A6-6
A8-6
A9-6
ALARM INPUT, 8
ALARM INPUT, 10

150mA
12 ALARM DRIVER
7 ALARM LOGIC
10

C-MAJ-2: MAJORITY GATE

Generates logical majority of three inputs.

TIMING INDICATOR 10
TIMING DRIVER 150 mA
1
TIMING RESET 1

SOURCE 1 21
SOURCE 2 19
SOURCE 3 17

10
16 MAJORITY

ITY INTERVAL LORTO 20

AGREEMENT ALARM

nal agreement signals from either) or the phase shifter detector.

39, NO EXTERNAL AGREEMENT DRIVER 150 mA
11, NO EXTERNAL AGREEMENT INDICATOR 10

TP-1, RED
INTERNAL CLOCK

C-CLK-1: ASYNCHRONOUS CLOCK

Provides a source of independent 2 MHz clock signals to slew or reset WO486-4A/PHASE SHIFT - type phase shifters.

1 CLOCK ENABLE, 28

8
18, CP
10
18, $\overline{CP}$

C-AND-1: DRRG ERROR LOGIC

Combines lost signal levels from the DRRG's to determine which DRRG has malfunctioned or that no two of the DRRG's agree (NO MAJORITY condition). For example, if DRRG -1 malfunctions, the two input lines marked 1, 2 and 1, 3 will both be TRUE, thus passing through the A22C gate and lighting the "DRRG 1" lamp. If A22B, C, D gate outputs are FALSE, the NO MAJORITY gate, A14C will activate to generate an arbitrary reset to all three DRRG's.

2 54 1,2

2 58 2,3

2 56 1,3

A3-13

78, DRRG No. 1 JUMP

A3-1

76, DRRG No. 2 JUMP

150mA

A3-2

150mA

74, DRRG No. 3 JUMP

C-RST-1: RESET AND GATES

Enables the MAJORITY INTERVAL LORTO pulse to reset the DRRG determined by C-AND-1 to have malfunctioned. The MAJORITY INTERVAL LORTO pulse is phase coded, hence this reset operation will correct any phase code jumps as well as time jumps among the DRRG's.

TP-4, GREEN
NO MAJORITY RESET

C-RST-2: NO MAJORITY RESET LOGIC

Selects individual DRRG reset pulses or a NO MAJORITY reset pulse. This pulse is selected as the first DRRG LORTO to arrive at C-OR-2. The single shot locks out the NO MAJORITY reset circuit for a period greater than two Loran periods to allow the DRRG pulse loss indicators to determine if a majority agreement has been achieved. At the end of this time period

C-OR-1: R NOR

Digitally DRRG reset the internal logic and th external log

another reset attempt will be made if the NO MAJORITY CONDITION persists.

5 → 48, LOST MAJORITY OUTPUT

C-OR-2: OR GATE
Develops NO MAJORITY RESET PULSE from DRRG 1, 2 or 3 LORTO.

3 — 73 No. 1
3 — 71 No. 2
3 — 68 No. 3

C-MAJ-1: LORTO MAJORITY GATE

Provides a MAJORITY LORTO (not the INTERVAL MAJORITY LORTO) to all system cards such as Loran waveform generators etc.

TP-3, BLUE MAJORITY LORTO
20
MAJORITY LORTO → 45
MAJORITY LORTO → 43
20

C-ALM-3: CHECK TIMING ALARM

Flip-flop AMA is set by a NO MAJORITY condition and displays this to the operator as a CHECK TIMING indication. The operator must acknowledge this by actuating the CHECK TIMING RESET to clear the flip-flop.

1 EXT.
1 EXT.
9, CHECK
41, CHECK
50, CHECK
C11, 0.1μF

1
RVAL LORTO 1,2 — 65
RVAL LORTO 1,3 — 64
RVAL LORTO 2,3 — 62

C-OR-3: OR GATE/LINE DRIVER

Generates INTERVAL MAJORITY LORTO and provides a balanced line driver output for external use of this signal.

TP-5, WHITE
MAJORITY INTERVAL LORTO
52 — 20

47, MAJOR

C-AND-2: EXTERNAL AGREEMENT LOGIC

Determines if the local LORTO agrees with the EXTERNAL LORTO by setting a flip-flop on the leading edge of the EXTERNAL pulse and resetting with the AND agreement of the two pulses. A23 NOR gate provides lockout of all EXTERNAL RESET logic in the event that no local MAJORITY exists. This feature prevents cold-start lockup between two timing systems.

C-ALM-1: NO EXTERNAL

Logically OR's no extern the pulse detector (C-AND-2

1
1
44 — EXTERNAL MAJORITY INTERVAL LORTO
33 — EXTERNAL 0-SHIFTER AGREEMENT
2

C-RST-3 EXTERNAL RESET LOGIC

Provides RESET TO EXTERNAL logic. This logic will slew an internal phase shifter to agree with an external phase shifter and reset the dynamic DRRG elements. Actuation of the front panel RESET TO EXTERNAL pushbutton set A19B whose output enables the phase shifter reset mechanism. When the phase shifter agrees A18C changes state and sets the flip-flop composed of A24 gates. This output stops the DRRG dividers (actuates Parallel Enable) until this flip-flop is reset by the AND of the 5 MHz clock and the EXTERNAL INTERVAL MAJORITY LORTO. The divider is thus restarted precisely in time with the local 5 MHz and coarsely timed (within 200 ns) to the external MAJORITY pulse.

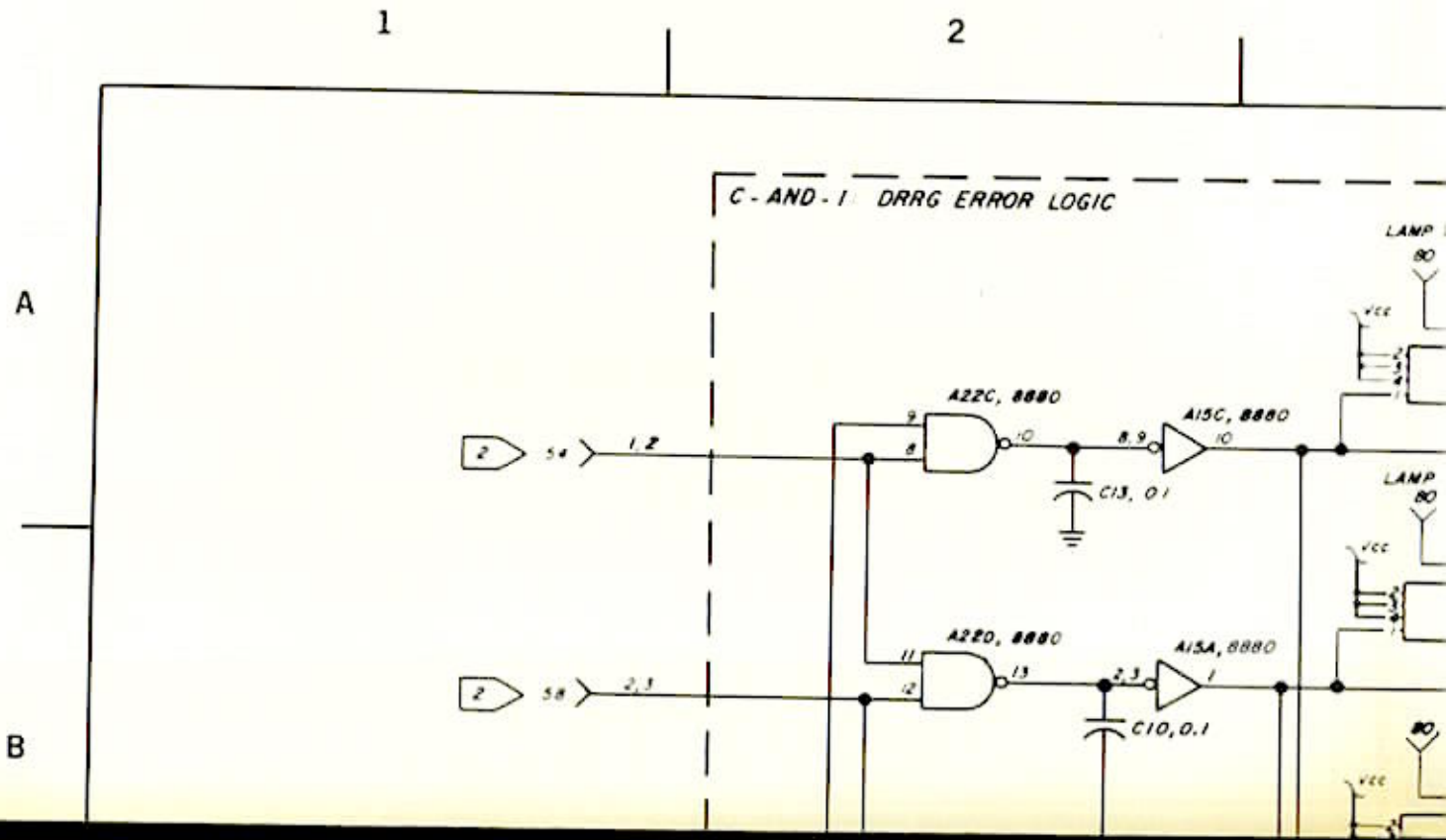
TEM 5MHz
1
AL RESET EXTERNAL
2
TE RESET EXTERNAL
2

27, Φ-SHIFT RESET TO EXTERNAL — 10
5, RESET TO EXTERNAL LOGIC — 6
37, RESET TO EXTERNAL DRIVER — 150 mA
30, Φ-SHIFT CLOCK SET OUTPUT — 5

ure 7.24. W0486-12A/CONTROL Block Diagram
3/7.50

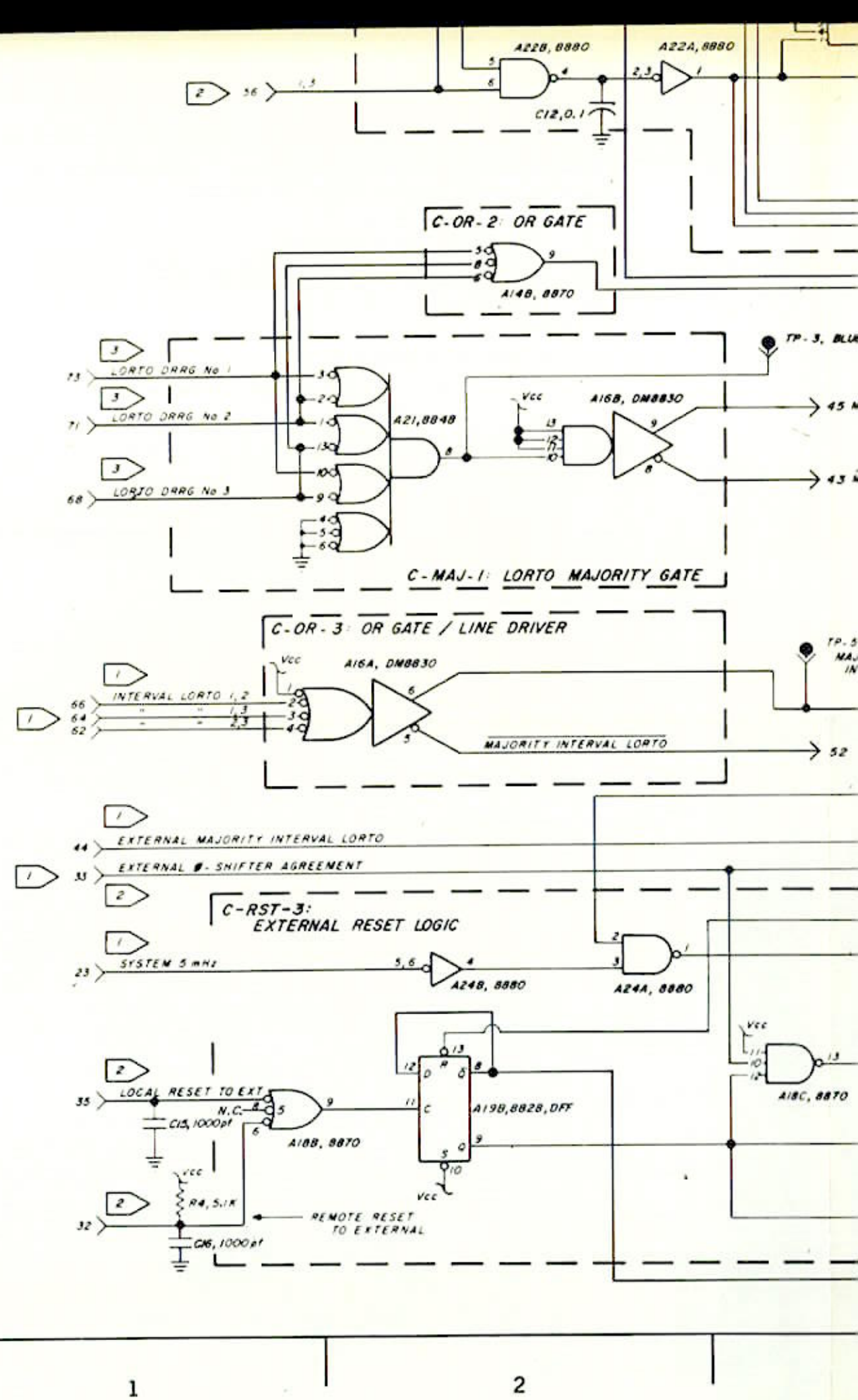

LORTC
DRRG
LORTC
DRRG
LORTC
DRRG
INTE
INTE
1
INTE
SYS
23
LOC
TO
35
REMO
TO
32

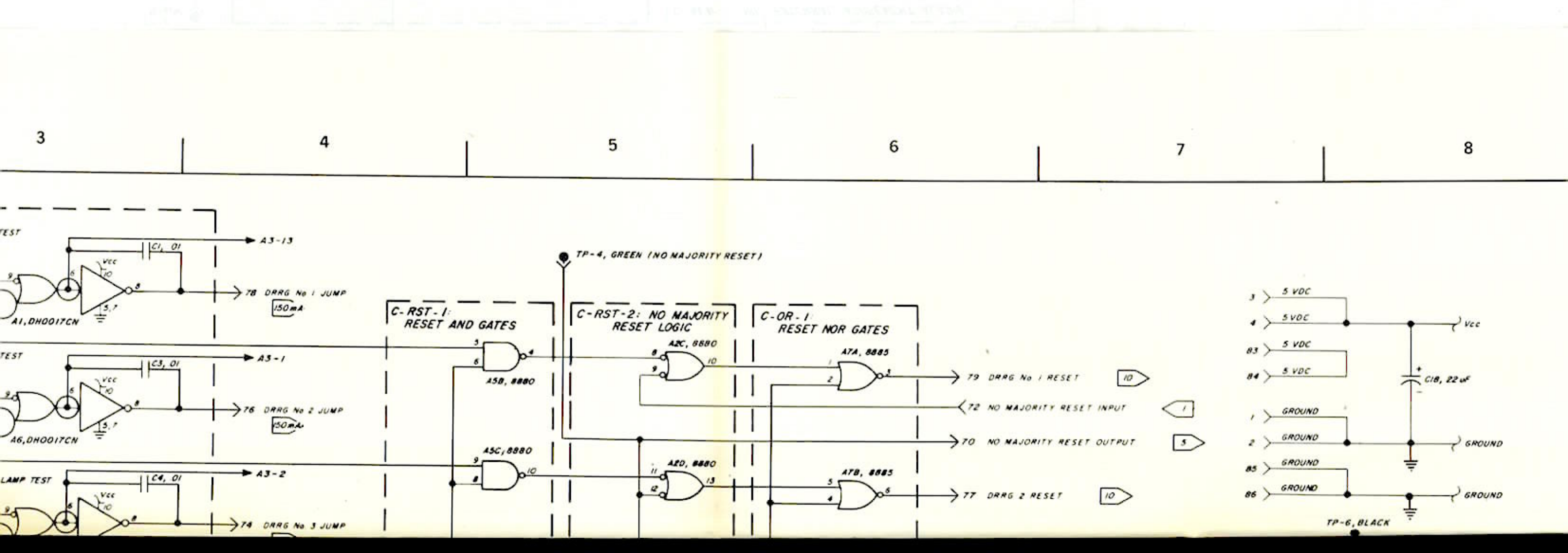
Figu
7.45


1
2
A
B
C - AND - 1 DRRG ERROR LOGIC
A22C, 8880
A15C, 8880
C13, 0.1
A22D, 8880
A15A, 8880
C10, 0.1
LAMP
80
VCC

PART LOCATION INDEX

REF. DESIG.	LOCATION	REF. DESIG.	LOCATION
A1	3A	A22D	2B
A2A	NOT USED	A23	4C
A2B	NOT USED	A24A	2E
A2C	5A	A24B	2E
A2D	5B	A24C	NOT USED
A3A	7C	A24D	4E
A3B	6C	A25A	4F
A3C	7C	A25B	5E
A4A	4F	A25C	3E
A4B	8C	A25D	3F
A4C	6E	A26	7D
A4D	5C		
A5A	4E	C1	3A
A5B	5A	C2	5E
A5C	5B	C3	3A
A5D	5B	C4	3B
A6	3B	C5	5D
A7A	6A	C6	6E
A7B	6B	C7	4F
A7C	NOT USED	C8	8C
A7D	6B	C9	7E
A8	3B	C10	2B
A9	4D	C11	5D
A10	6E	C12	2B
A11	4F	C13	2A
A12	7C	C14	4C
A13	7F	C15	1F
A14A	4C	C16	1F
A14B	2C	C17	3F
A14C	3C	C18	8A
A15A	2B	C19	6E
A15B	5B	CR1	4C
A15C	2A		
A15D	4C	E1	NOT SHOWN
A16A	1D	E2	NOT SHOWN
A16B	2D	E3	NOT SHOWN
A17A	4D		
A17B	NOT USED	R1	7E
A18A	NOT USED	R2	7F
A18B	1F	R3	4B
A18C	3F	R4	1F
A19A	5E	R5	3F
A19B	2F	R6	3E
A20A	7C		
A20B	NOT USED	TP1	8E
A20C	8D	TP2	4E
A20D	8F	TP3	3C
A21	2D	TP4	5A
A22A	2B	TP5	3D
A22B	2B	TP6	8B
A22C	2A		
		Z1	7F




3
4
5
6
7
8
TEST
A3-13
C1, 01
Vcc
78 DRAG No 1 JUMP
150mA
A1, DH0017CN
TEST
A3-1
C3, 01
76 DRAG No 2 JUMP
150mA
A6, DH0017CN
LAMP TEST
A3-2
C4, 01
74 DRAG No 3 JUMP
TP-4, GREEN (NO MAJORITY RESET)
C-RST-1: RESET AND GATES
A5B, 8880
A5C, 8880
C-RST-2: NO MAJORITY RESET LOGIC
A2C, 8880
A2D, 8880
C-OR-1: RESET NOR GATES
A7A, 8885
A7B, 8885
79 DRAG No 1 RESET
10
72 NO MAJORITY RESET INPUT
1
70 NO MAJORITY RESET OUTPUT
5
77 DRAG 2 RESET
10
3 5 VDC
4 5 VDC
83 5 VDC
84 5 VDC
Vcc
C18, 22 uF
1 GROUND
2 GROUND
85 GROUND
86 GROUND
GROUND
GROUND
TP-6, BLACK

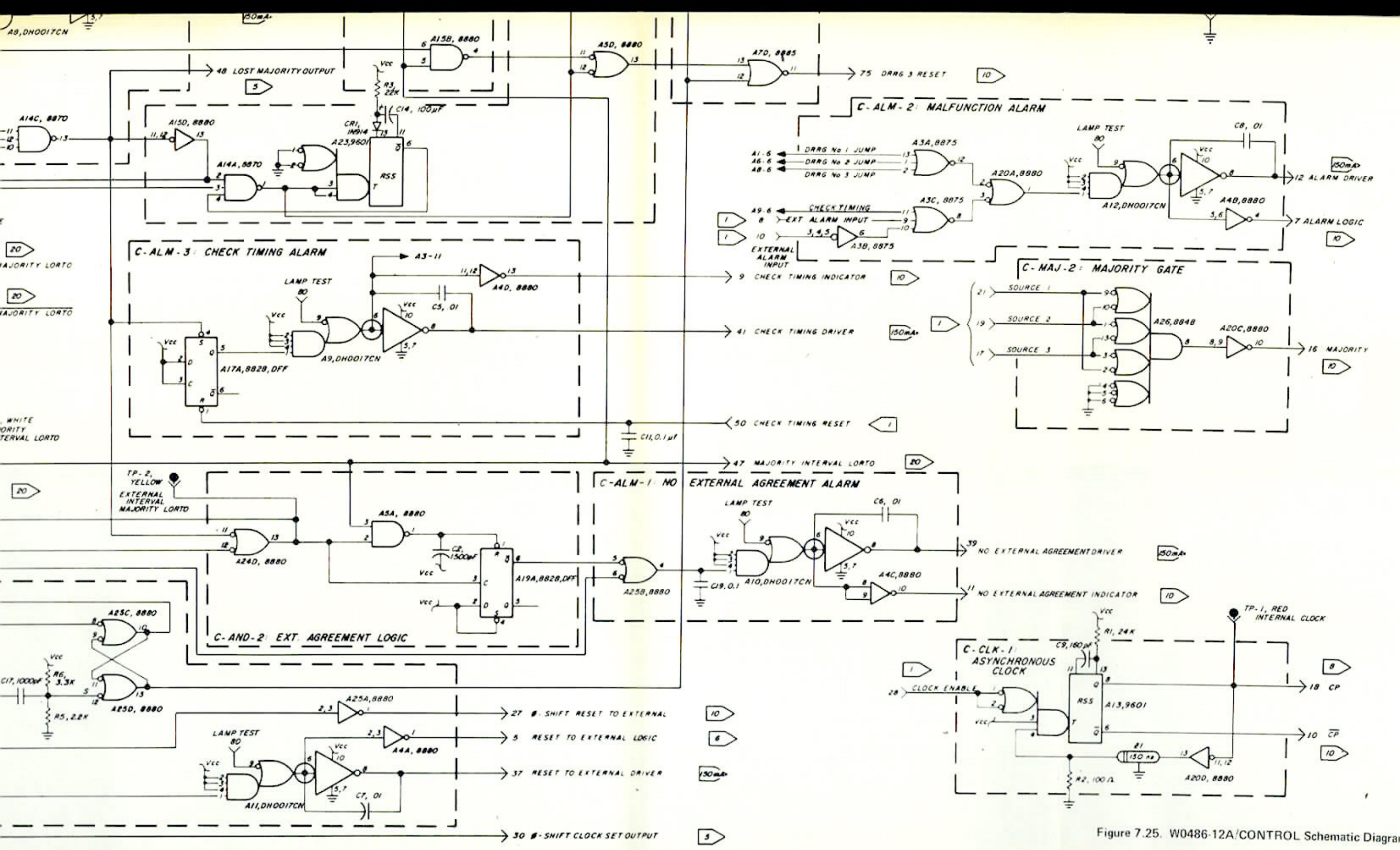
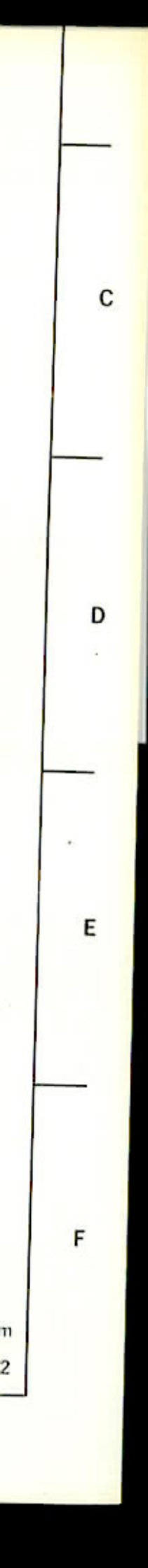


Figure 7.25. W0486-12A/CONTROL Schematic Diagra

3 4 5 6 7 8


A
B


C
D
E
F
m
2

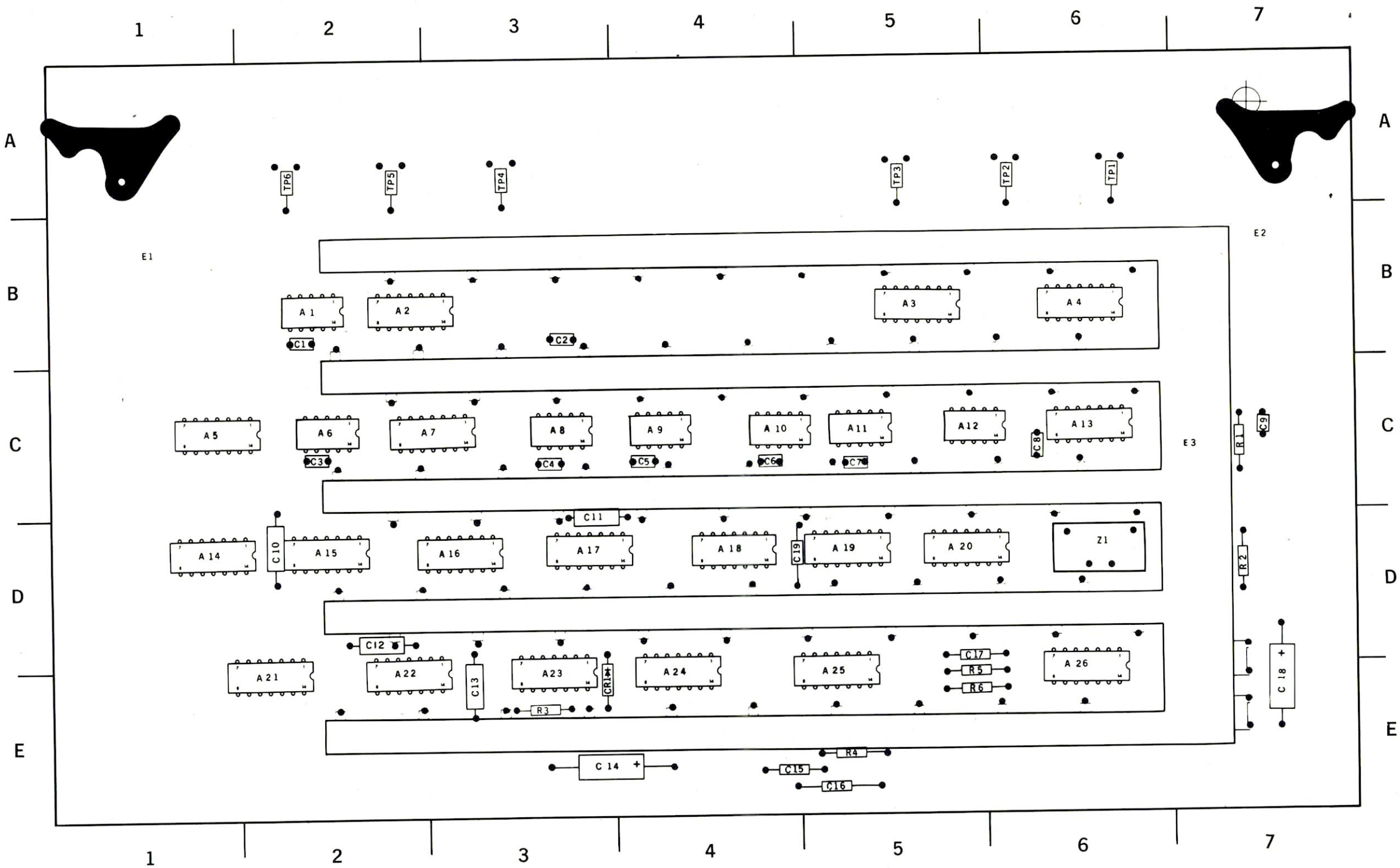


Figure 7.26. W0486-12A/CONTROL Parts Locator

PART LOCATION INDEX			
REF. DESIG.	LOCATION	REF. DESIG.	LOCAT
A1	2B	C9	7C
A2	2B	C10	2D
A3	5B	C11	3D
A4	6B	C12	2D
A5	1C	C13	3E
A6	2C	C14	3E
A7	2C	C15	4E
A8	3C	C16	5E
A9	4C	C17	5D
A10	4C	C18	7E
A11	5C	C19	4D
A12	5C		
A13	6C	CR1	3E
A14	1D		
A15	2D	E1	1A
A16	3D	E2	7A
A17	3D	E3	7C
A18	4D		
A19	5D	R1	7C
A20	5D	R2	7D
A21	2E	R3	3E
A22	2E	R4	5E
A23	3E	R5	5E
A24	4E	R6	5E
A25	5E		
A26	6E	TP1	6A
		TP2	6A
C1	2B	TP3	5A
C2	3B	TP4	3A
C3	2C	TP5	2A
C4	3C	TP6	2A
C5	4C		
C6	4C	Z1	6D
C7	5C		
C8	6C		

TP3, BLUE
PULSE TRIGGERS

TP4, GRAY

+ comm ♦ + ETR ♦.

TP7, GREEN
EMPT

R26,
100 Ω

10

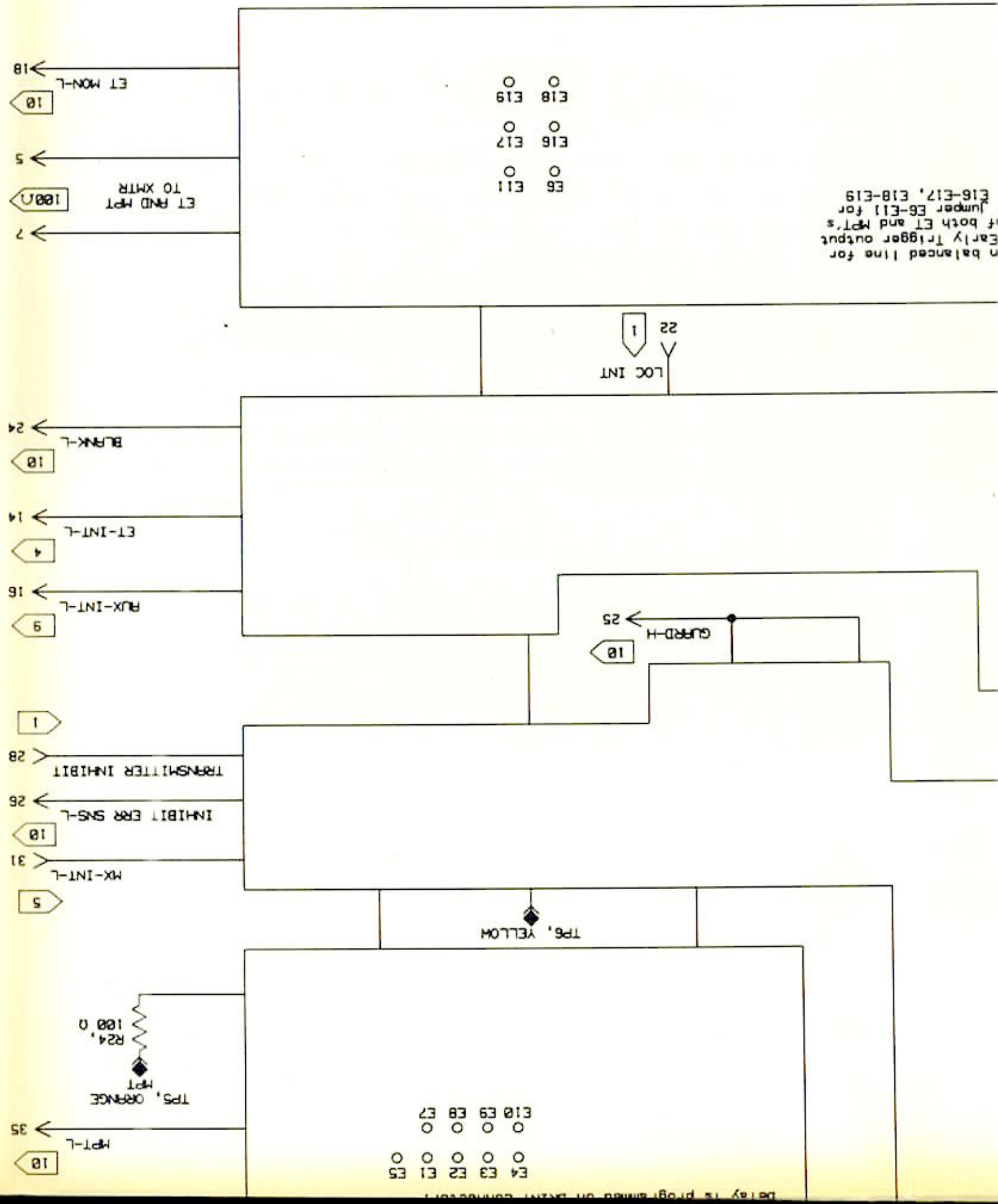
29

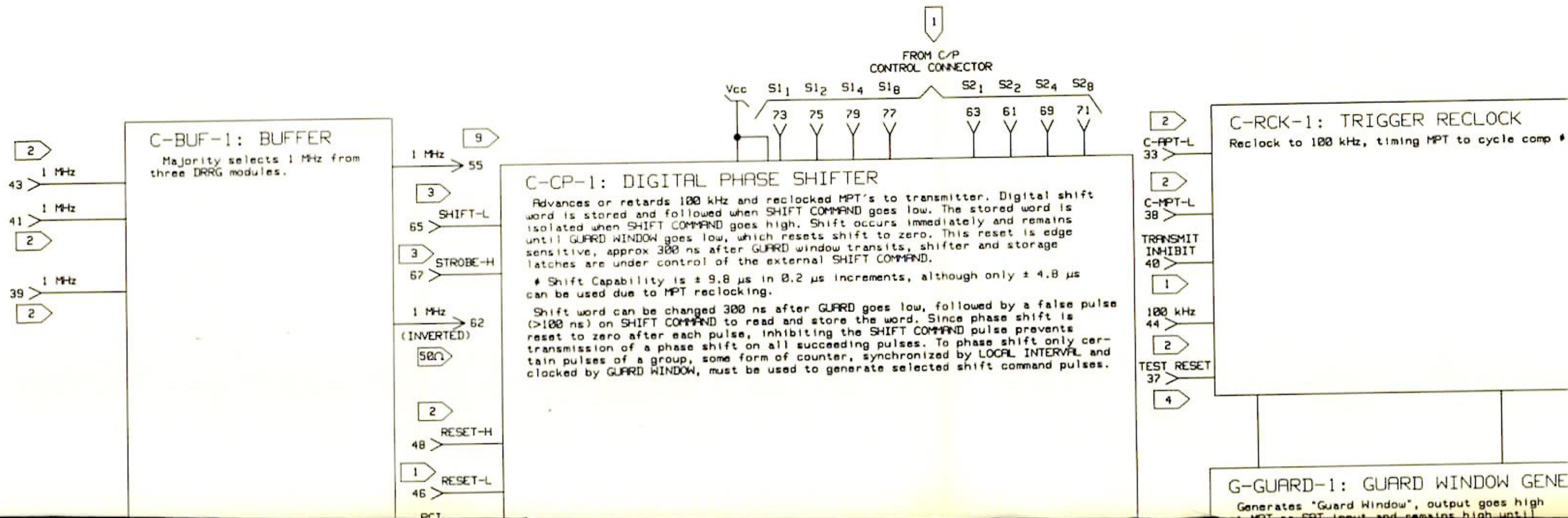
EMPT-L

RATOR

C-TD-1: DIGITAL DELAY

Delays EMPT to form LMPT in increments of 10 µs.
Total delay is n x 10µs; 1≤ n ≤ 16.


E18 E19
E16 E17
E6 E11
n balanced line for
Early Trigger output
f both ET and MPT's
Jumper E6-E11 for
E16-E17, E18-E19
LOC INT
22
1
ET MON-L
18
10
ET RND MPT
TO XMTR
100Ω
5
7
BLANK-L
24
10
ET-INT-L
14
4
RUX-INT-L
16
9
GUARD-H
25
10
1
TRANSMITTER INHIBIT
28
INHIBIT ERR SNS-L
26
10
MX-INT-L
31
5
TP6, YELLOW
TP5, ORANGE
MPT
R24,
100 Ω
MPT-L
35
10
E10 E9 E8 E7
E4 E3 E2 E1 E5



FROM C/P CONTROL CONNECTOR
Vcc
S1₁ S1₂ S1₄ S1₈ S2₁ S2₂ S2₄ S2₈
73 75 79 77 63 61 69 71
C-BUF-1: BUFFER
Majority selects 1 MHz from three DRRG modules.
1 MHz 43
1 MHz 41
1 MHz 39
1 MHz 55
SHIFT-L 65
STROBE-H 67
1 MHz (INVERTED) 62
50Ω
RESET-H 48
RESET-L 46
C-CP-1: DIGITAL PHASE SHIFTER
Advances or retards 100 kHz and reclocked MPT's to transmitter. Digital shift word is stored and followed when SHIFT COMMAND goes low. The stored word is isolated when SHIFT COMMAND goes high. Shift occurs immediately and remains until GUARD WINDOW goes low, which resets shift to zero. This reset is edge sensitive, approx 300 ns after GUARD window transits, shifter and storage latches are under control of the external SHIFT COMMAND.
* Shift Capability is ± 9.8 µs in 0.2 µs increments, although only ± 4.8 µs can be used due to MPT reclocking.
Shift word can be changed 300 ns after GUARD goes low, followed by a false pulse (>100 ns) on SHIFT COMMAND to read and store the word. Since phase shift is reset to zero after each pulse, inhibiting the SHIFT COMMAND pulse prevents transmission of a phase shift on all succeeding pulses. To phase shift only certain pulses of a group, some form of counter, synchronized by LOCAL INTERVAL and clocked by GUARD WINDOW, must be used to generate selected shift command pulses.
C-APT-L 33
C-MPT-L 38
TRANSMIT INHIBIT 40
100 kHz 44
TEST RESET 37
C-RCK-1: TRIGGER RECLOCK
Reclock to 100 kHz, timing MPT to cycle comp *
G-GUARD-1: GUARD WINDOW GENE
Generates "Guard Window", output goes high

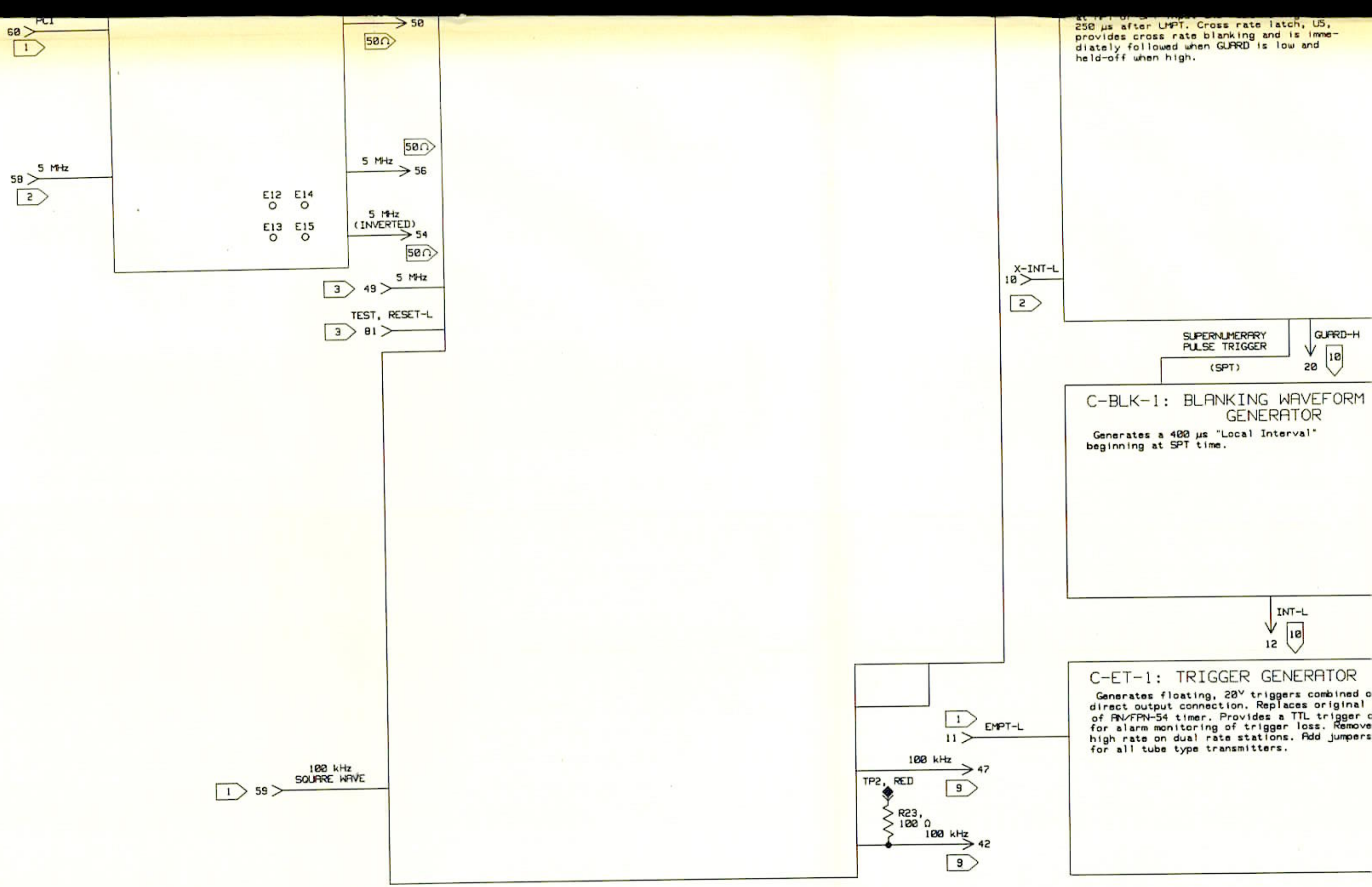
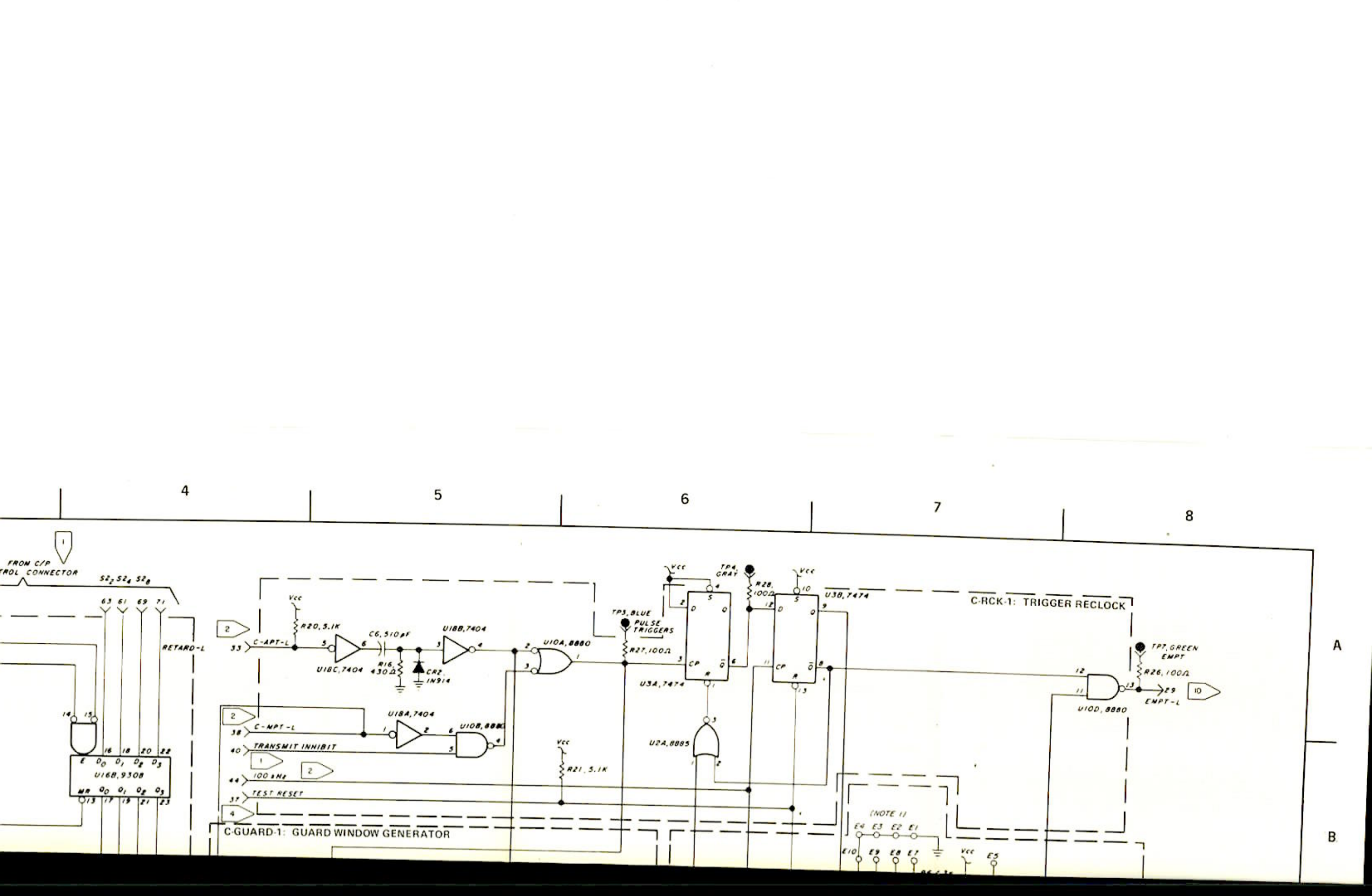


Figure 7.27. W0486-28B/DRINT/CP Block Diagram

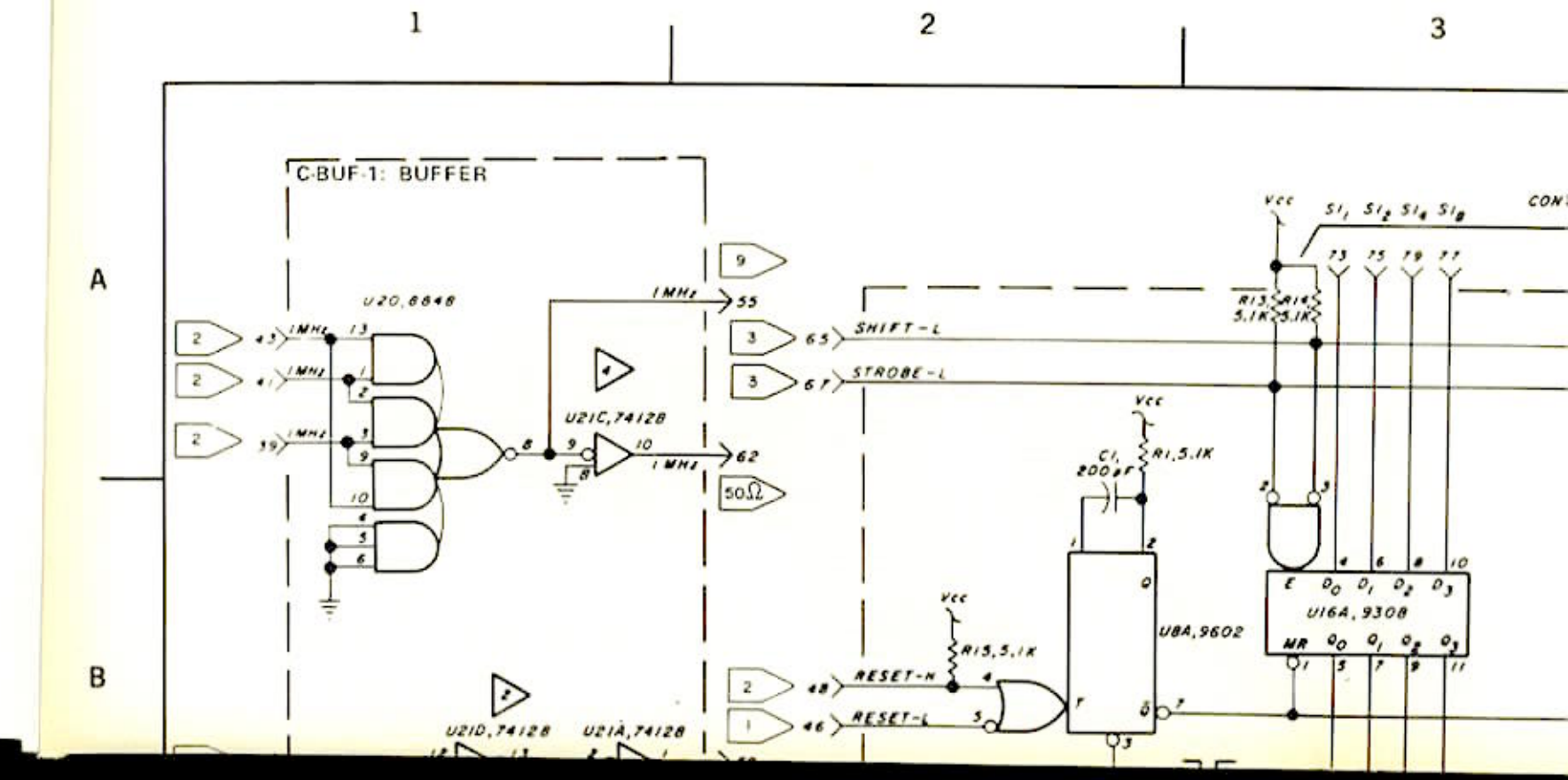

4
5
6
7
8
A
B
FROM C/P TROL CONNECTOR
$S2_2$ $S2_4$ $S2_8$
63 61 69 71
RETARD-L
U16B, 9308
C-APT-L
R20, 5.1K
C6, 510 pF
U18B, 7404
U18C, 7404
R16, 430Ω
CR2, IN914
U10A, 8880
C-MPT-L
U18A, 7404
U10B, 8880
TRANSMIT INHIBIT
100 kHz
TEST RESET
C-GUARD-1: GUARD WINDOW GENERATOR
TP3, BLUE PULSE TRIGGERS
R27, 100Ω
U3A, 7474
TP4, GRAY
R28, 100Ω
U3B, 7474
U2A, 8885
R21, 5.1K
C-RCK-1: TRIGGER RECLOCK
U10D, 8880
TP7, GREEN EMPT
R26, 100Ω
EMPT-L
(NOTE 1)
E4 E3 E2 E1
E10 E9 E8 E7
E5

C-TD-1: DIGITAL DELAY

C-BLK-1: BLANKING WAVEFORM GENERATOR

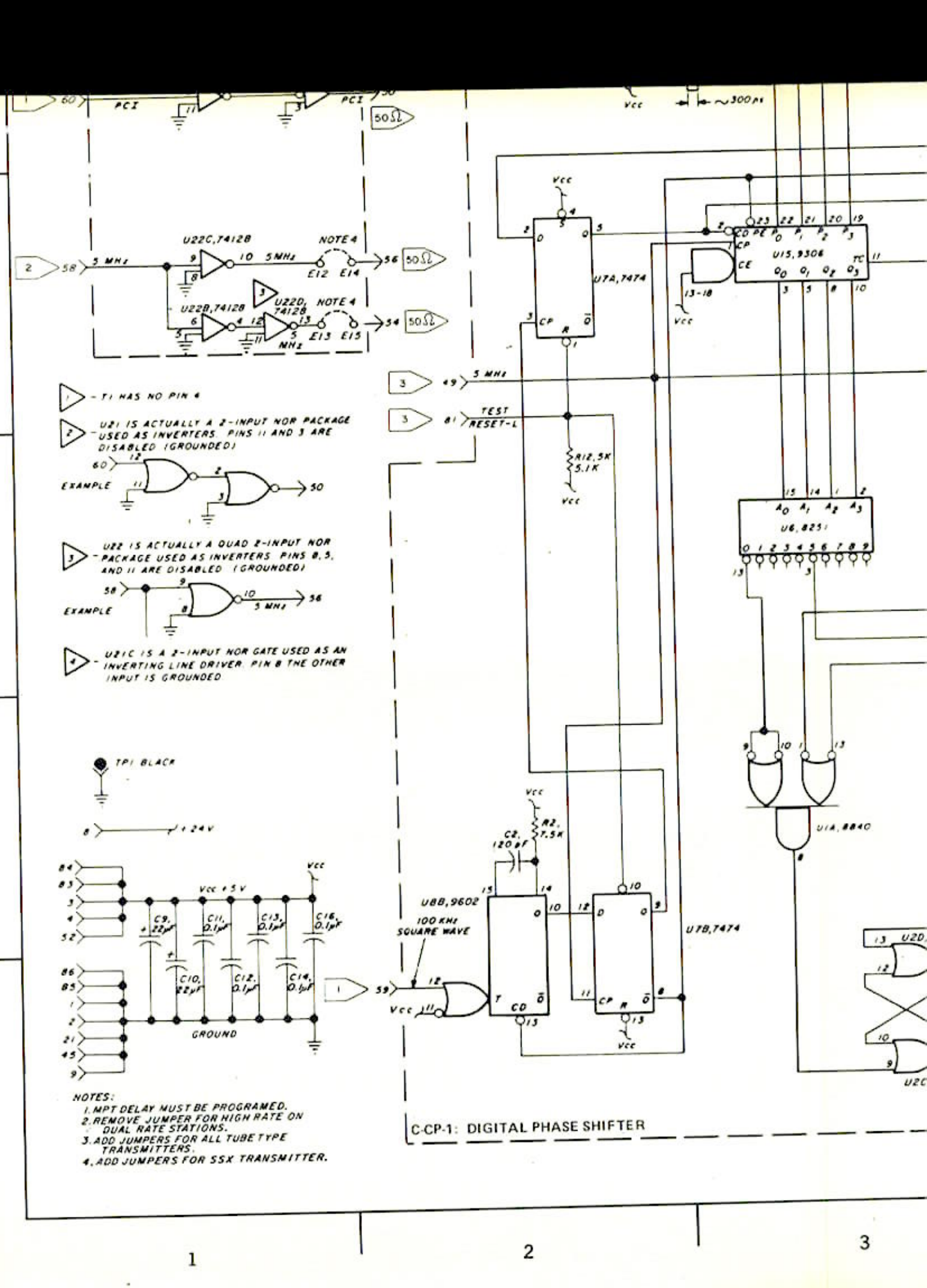
C-ET-1: TRIGGER GENERATOR

Figure 7.28. W0486-28B/DRINT/CP Schematic Diagram


1
2
3
A
B
C-BUF-1: BUFFER
U20, 6848
U21C, 74128
U21D, 74128
U21A, 74128
1MHz
50Ω
SHIFT-L
STROBE-L
RESET-H
RESET-L
Vcc
R1, 5.1K
R13, 5.1K
R14, 5.1K
R15, 5.1K
C1, 200pF
U8A, 9602
U16A, 9308

PART LOCATION INDEX

REF.DESIG.	LOCATION	REF.DESIG.	LOCATION	REF.DESIG.	LOCATION
C1	2A	R1	2A	U3A	6A
C2	2E	R2	2E	U3B	6A
C3	5C	R3	7C	U4	7C
C4	5D	R4	7B	U5	6D
C5	5F	R5	7B	U6	3D
C6	5A	R6	7B	U7A	2C
C7	6F	R7	5C	U7B	2F
C8	6F	R8	7C	U8A	2B
C9	1E	R9	5D	U8B	2F
C10	1F	R10	5F	U9	4D
C11	1E	R11	5F	U10A	5A
C12	1F	R12	2D	U10B	5B
C13	1E	R13	3A	U10C	8C
C14	1F	R14	3A	U10D	8A
C15	7C	R15	2B	U11A	5C
C16	1E	R16	5A	U11B	5D
		R17	7F	U12A	7D
CR1	8C	R18	6F	U12B	7D
CR2	5A	R19	5F	U12C	7E
CR3	5F	R20	4A	U12D	7E
CR4	5F	R21	6B	U13	5F
CR5	6F	R22	6D	U14	5E
CR6	6F	R23	4F	U15	3C
CR7	5F	R24	8C	U16A	3B
		R25	7C	U16B	4B
E1	7B	R26	8A	U17	4C
E2	7B	R27	6A	U19D	7F
E3	7B	R28	6A	U18A	5B
E4	7B	R29	8C	U18B	5A
E5	7B			U18C	5A
E6	5F	T1	6F	U19A	8D
E7	7B			U19B	8E
E8	7B	TP1	1E	U19C	7E
E9	7B	TP2	4F	U19E	7F
E10	7B	TP3	6A	U19F	5C
E11	5F	TP4	6A	U20	1A
E12	1C	TP5	8C	U21A	1B
E13	1C	TP6	7C	U21B	NOT USED
E14	2C	TP7	8A	U21C	1A
E15	2C			U21D	1B
E16	7F	U1A	3E	U22A	NOT USED
E17	7F	U1B	4E	U22B	1C
E18	7F	U2A	6B	U22C	1C
E19	7F	U2B	7C	U22D	1C
E20	NOT SHOWN	U2C	3F		
E21	NOT SHOWN	U2D	3F		



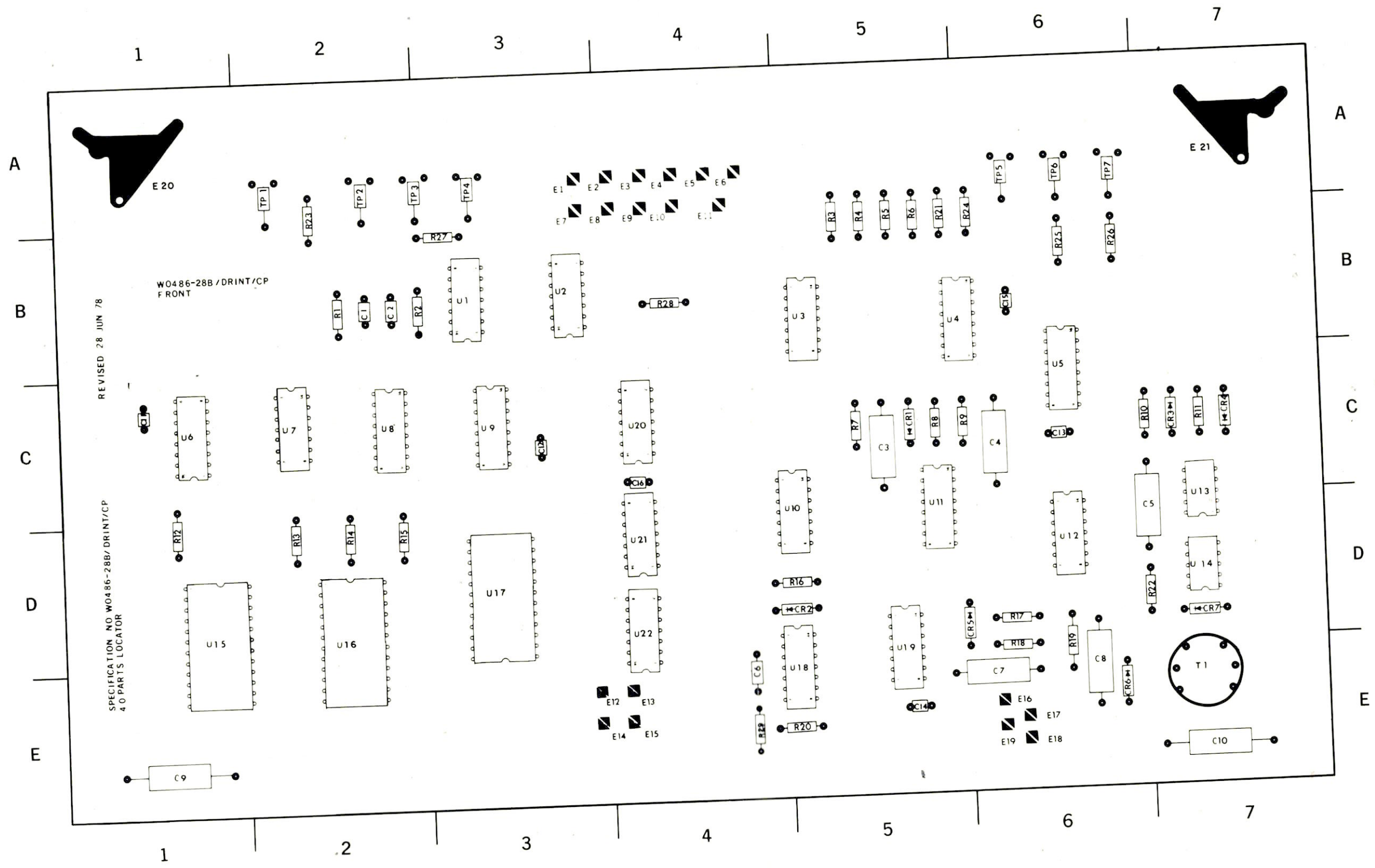


Figure 7.29. W0486-28B/DRINT/CP Parts Locator

PART LOCATION INDEX

REF. DESIG.	LOCATION	REF. DESIG.	LOCATION
C1	2B	R9	5C
C2	2B	R10	7C
C3	5C	R11	7C
C4	6C	R12	1D
C5	7D	R13	2D
C6	4E	R14	2D
C7	6E	R15	2D
C8	6E	R16	5D
C9	1E	R17	6D
C10	7E	R18	6D
C11	1C	R19	6D
C12	3C	R20	5E
C13	6C	R21	5B
C14	5E	R22	7D
C15	6B	R23	2A
C16	4C	R24	5B
		R25	6B
CR1	5C	R26	6B
CR2	5D	R27	3B
CR3	7C	R28	4B
CR4	7C	R29	4E
CR5	6D		
CR6	6E	T1	7E
CR7	7D		
		TP1	2A
E1	3A	TP2	2A
E2	4A	TP3	2A
E3	4A	TP4	3A
E4	4A	TP5	6A
E5	4A	TP6	6A
E6	4A	TP7	6A
E7	3A		
E8	4A	U1	3B
E9	4A	U2	3B
E10	4A	U3	5B
E11	4A	U4	5B
E12	3E	U5	6C
E13	4E	U6	1C
E14	3E	U7	2C
E15	4E	U8	2C
E16	6E	U9	3C
E17	6E	U10	5D
E18	6E	U11	5D
E19	6E	U12	6D
E20	1A	U13	7C
E21	7A	U14	7D
		U15	1D
R1	2B	U16	2D
R2	2B	U17	3D
R3	5B	U18	5E
R4	5B	U19	5E
R5	5B	U20	4C
R6	5B	U21	4D
R7	5C	U22	4D
R8	5C		

.75 41 LORTO-L

Vcc

R15, 4.7K

TP6, BLUE LOCAL INT.-L

TP5, GREEN MAJ. MPT #-H

R13, 4.7K

44 TUBE-H/SSX-L

C-MSG-1: 1 kHz MAJORITY SELECTOR GATE

AND-OR-INVERT gates (U19, U20) form the logical majority of 1 kHz #5 and 1 kHz #9 signals from three WE486-3/DRRG modules. The six inputs of each gate must be externally connected in three pairs (#5-L1, -L2, -L3 and #9L1, -L2, -L3).

With S4 (SSX/TUBE) in the SSX position or with TUBE-H/SSX-L input held low, two-input multiplexer, U18, selects #9 1-kHz for MAJ MPT#-H which generates coarse MPT (PMPT9) 900 µs after the start of LOCAL INTERVAL and selects #5 for MAJ INT/H which terminates LOCAL INTERVAL 1600 µs after the last (8th or 9th) PMPT. With the TUBE-H/SSX-L input high and S4 (SSX/TUBE) in the TUBE position, U18 selects #5 1-kHz to time the end of LOCAL INTERVAL 1200 µs after the last PMPT.

21
17
19
.25 27
25
23

6
12
8
25

L-PCG-1: PHASE CODE GENER

Majority PCI, Master/Secondary input from
switch S-4, and MPT Counter outputs Q_D, Q_C
512 X 8 PROM to develop Phase Code wavefor
Also developed are PMPT8 Gate Control, PM
Control to the Local Interval Generator.
creates a set of MPT's which occur at a s
by C-RSG-1) after each of the first eight
PMPT-9 is input to the 28B/DRINT/CP and P
28B/DRINT/CP and the 8A/INTERFACE. LORTO
of Local Interval is determined by the s
the MASTER/SECONDARY input to the 30/PC/

S4	M
TUBE	10,900 µs
SSX	11,500 µs

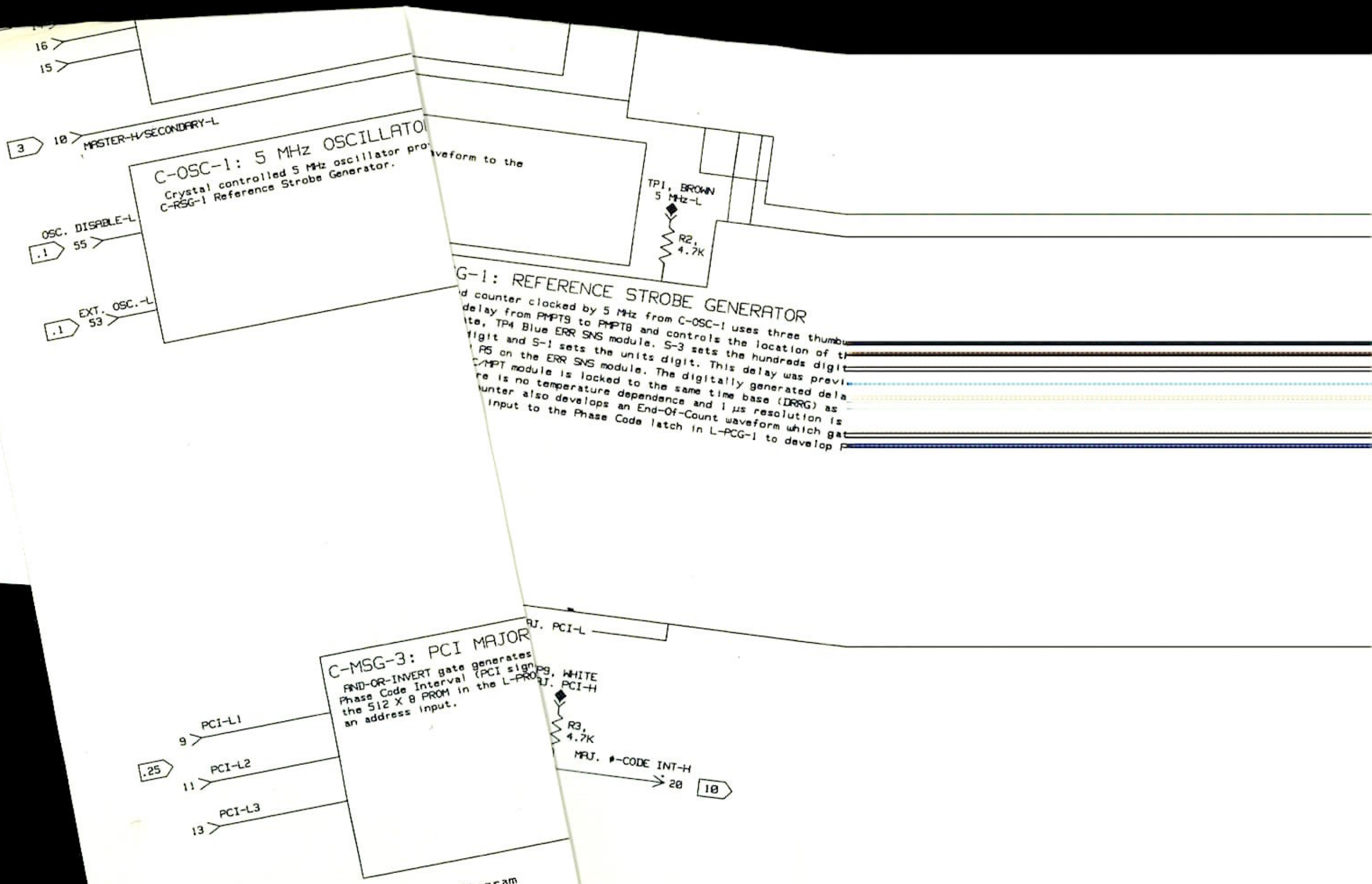
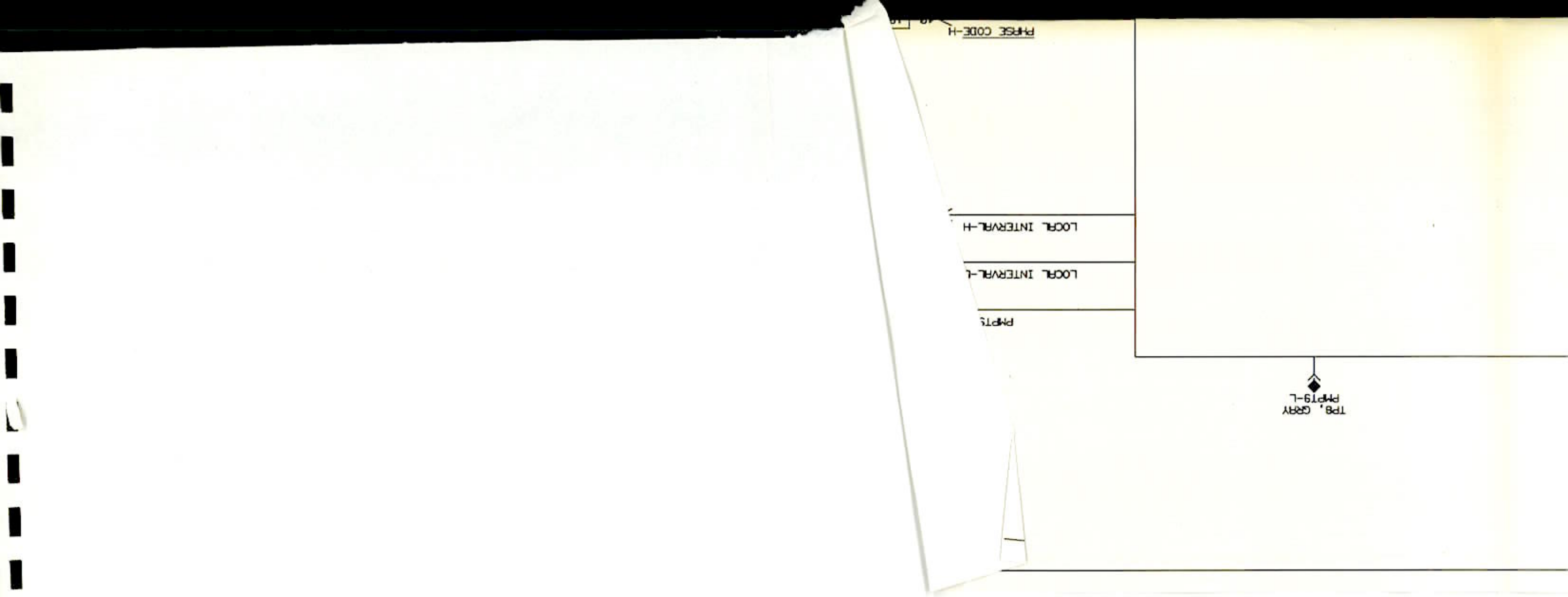
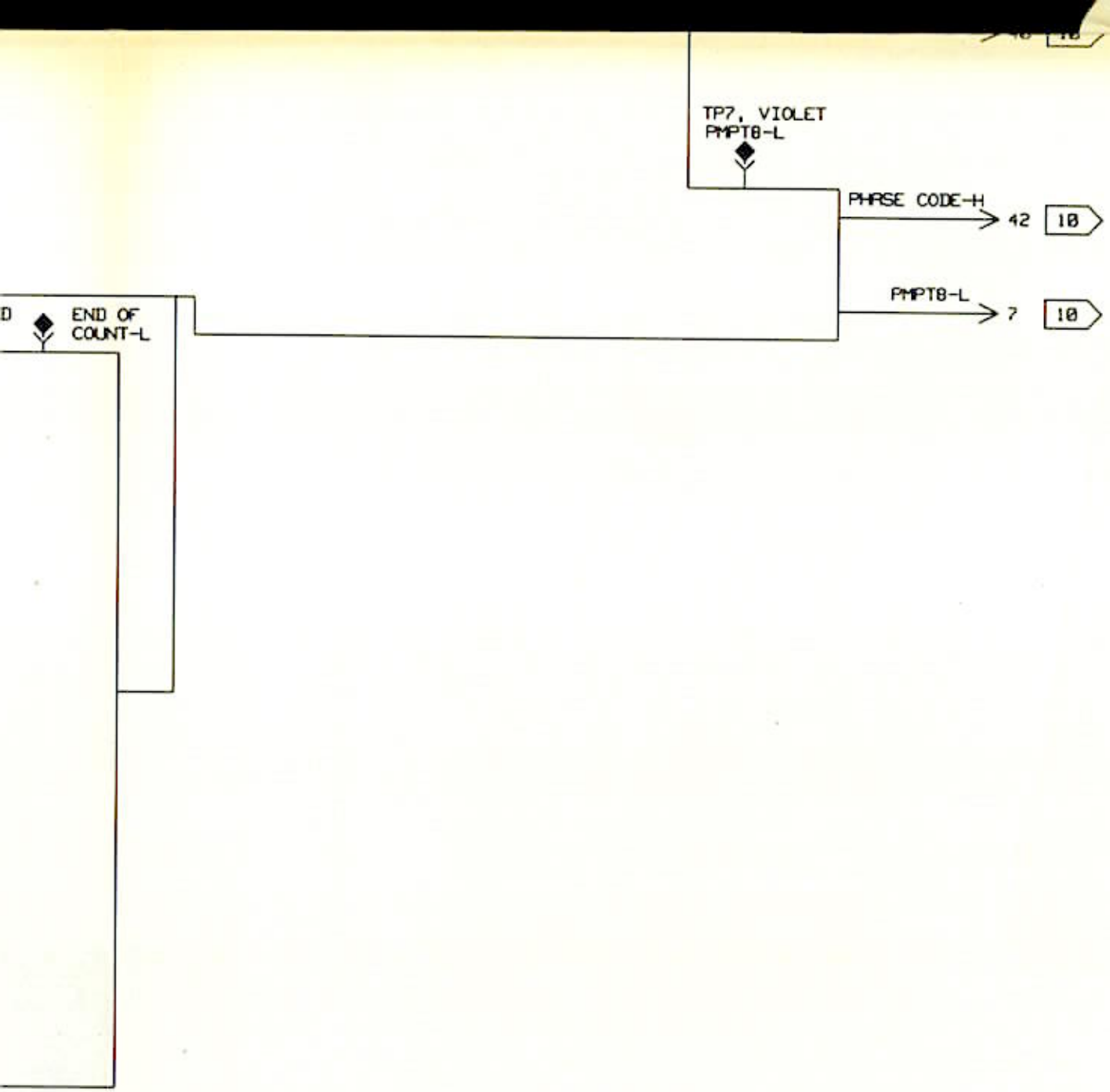


Figure 7.30. W0486-30/PC/MPT Block Diagram


PHRSE CODE-H
LOCAL INTERVAL-H
LOCAL INTERVAL-L
PHPT9
TPB, GRAY
PHPT9-L



ger module generates timing waveforms
dary Loran-C pulse group with delays
ther vacuum-tube or solid-state trans-

41 LORTO-L

Vcc

R15, 4.7K

TP6, BLUE LOCAL INT.-L

44 TUBE-H/SSX-L

TP5, GREEN MAJ. MPT #-H

R13, 4.7K

C-MSG-1: 1 kHz MAJORITY SELECTOR GATE

AND-OR-INVERT gates (U19, U20) form the logical majority of 1 kHz #5 and 1 kHz #9 signals from three H0486-3/DRRG modules. The six inputs of each gate must be externally connected in three pairs (#5-L1, -L2, -L3 and #9L1, -L2, -L3).

With S4 (SSX/TUBE) in the SSX position or with TUBE-H/SSX-L input held low, two-input multiplexer, U18, selects #9 1-kHz for MAJ MPT#-H which generates coarse MPT (PMPT9) 900 µs after the start of LOCAL INTERVAL and selects #5 for MAJ INT/H which terminates LOCAL INTERVAL 1600 µs after the last (8th or 9th) PMPT. With the TUBE-H/SSX-L input high and S4 (SSX/TUBE) in the TUBE position, U18 selects #5 1-kHz to time the end of LOCAL INTERVAL 1200 µs after the last PMPT.

21
17
19
27
25
23
6
12
8

L-PCG-1: PHASE CODE GENERATOR

Majority PCI, Master/Secondary input from the Program Card, Tube/SSX switch S-4, and MPT Counter outputs Q_D, Q_C, Q_B and Q_A are gated in a 512 X 8 PROM to develop Phase Code waveform to the Phase Code Latch. Also developed are PMPT8 Gate Control, PMPT9 Gate Control and Local Control to the Local Interval Generator. A Pseudo-MPT (PMPT8) generator creates a set of MPT's which occur at a selectable delay (controlled by C-RSG-1) after each of the first eight MPT's of the MPT9 signal. PMPT-9 is input to the 28B/DRINT/CP and PMPT-8 is input to both the 28B/DRINT/CP and the 8A/INTERFACE. LORTO starts Local Interval. The length of Local Interval is determined by the setting of S4 (TUBE or SSX) and the MASTER/SECONDARY input to the 30/PC/MPT.

S4	M	S
TUBE	10,900 µs	8,900 µs
SSX	11,500 µs	9,500 µs

14
16
15
10 MASTER-H/SECONDARY-L

C. DISABLE-L
55
EXT. OSC.-L
53

C-OSC-1: 5 MHz OSCILLATOR

Crystal controlled 5 MHz oscillator provides waveform to the C-RSG-1 Reference Strobe Generator.

TP1, BROWN
5 MHz-L

R2,
4.7K

TP2, RE

C-RSG-1: REFERENCE STROBE GENERATOR

A gated counter clocked by 5 MHz from C-OSC-1 uses three thumbwheel switches. Set the delay from PMPT9 to PMPT8 and controls the location of the Reference Select Gate, TP4 Blue ERR SNS module. S-3 sets the hundreds digit, S-2 sets the tens digit and S-1 sets the units digit. This delay was previously controlled by R13 and R5 on the ERR SNS module. The digitally generated delay of the W0486-30/PC/MPT module is locked to the same time base (DRRG) as the 3 μs Reference Strobe. There is no temperature dependence and 1 μs resolution is provided. The gated counter also develops an End-Of-Count waveform which gates the 5 MHz clock and is input to the Phase Code latch in L-PCG-1 to develop Phase Code.

MAJ. PCI-L

C-MSG-3: PCI MAJORITY SELECTOR GATE

AND-OR-INVERT gate generates a majority DRRG Majority Phase Code Interval (PCI signal. This is in turn sent to the 512 X 8 PROM in the L-PROM-J Phase Code Generator as an address input.

PCI-L1
9
5
PCI-L2
11
PCI-L3
13

TP9, WHITE
MAJ. PCI-H

R3,
4.7K

MAJ. ϕ-CODE INT-H
20
10

100 kHz DELAYED → 49 9
100 kHz → 76 1

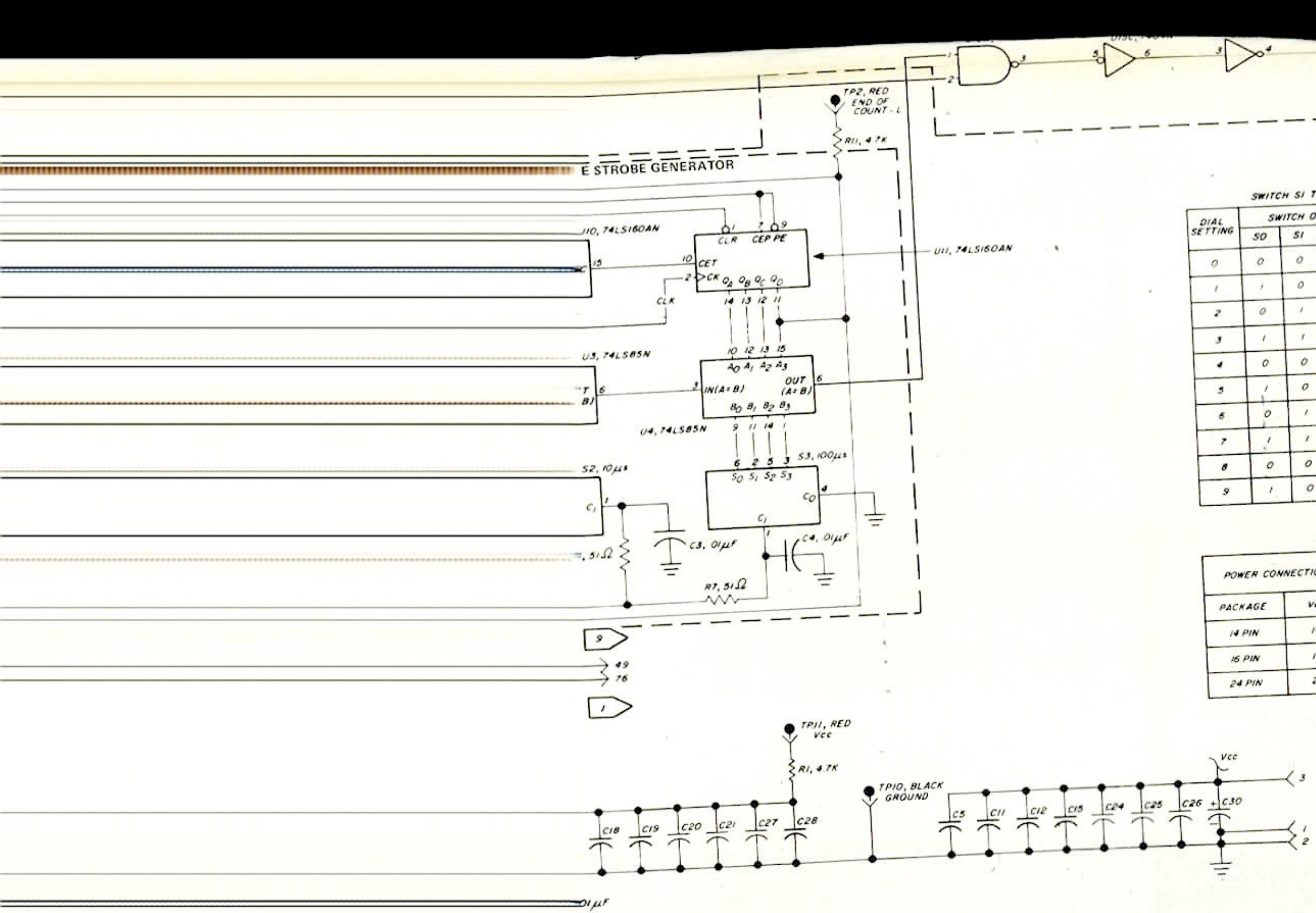
W0486-30/PC/MPT
Phase Code/Multiplier Trigg
to format a Master or Second
selectable to accomodate ei
mitter types.

ure 7.30. W0486-30/PC/MPT Block Diagram
1/7.62


.75
.25
.25



Fig
7.6



SWITCH S1 THRU S3

DIAL SETTING	SWITCH OUTPUTS			
	S0	S1	S2	S3
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

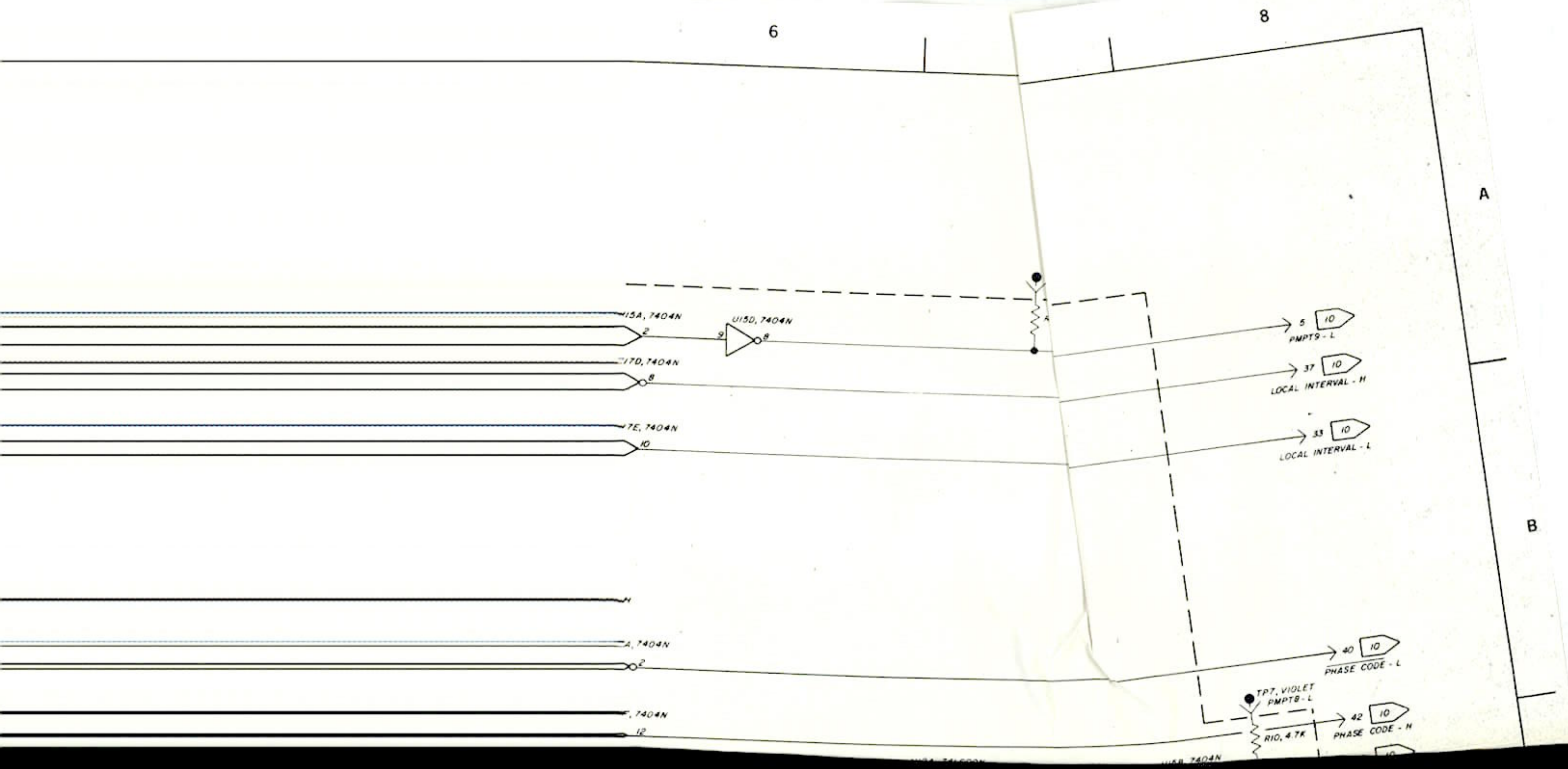
0 = CONNECTED TO COMMON C0 (GROUND)

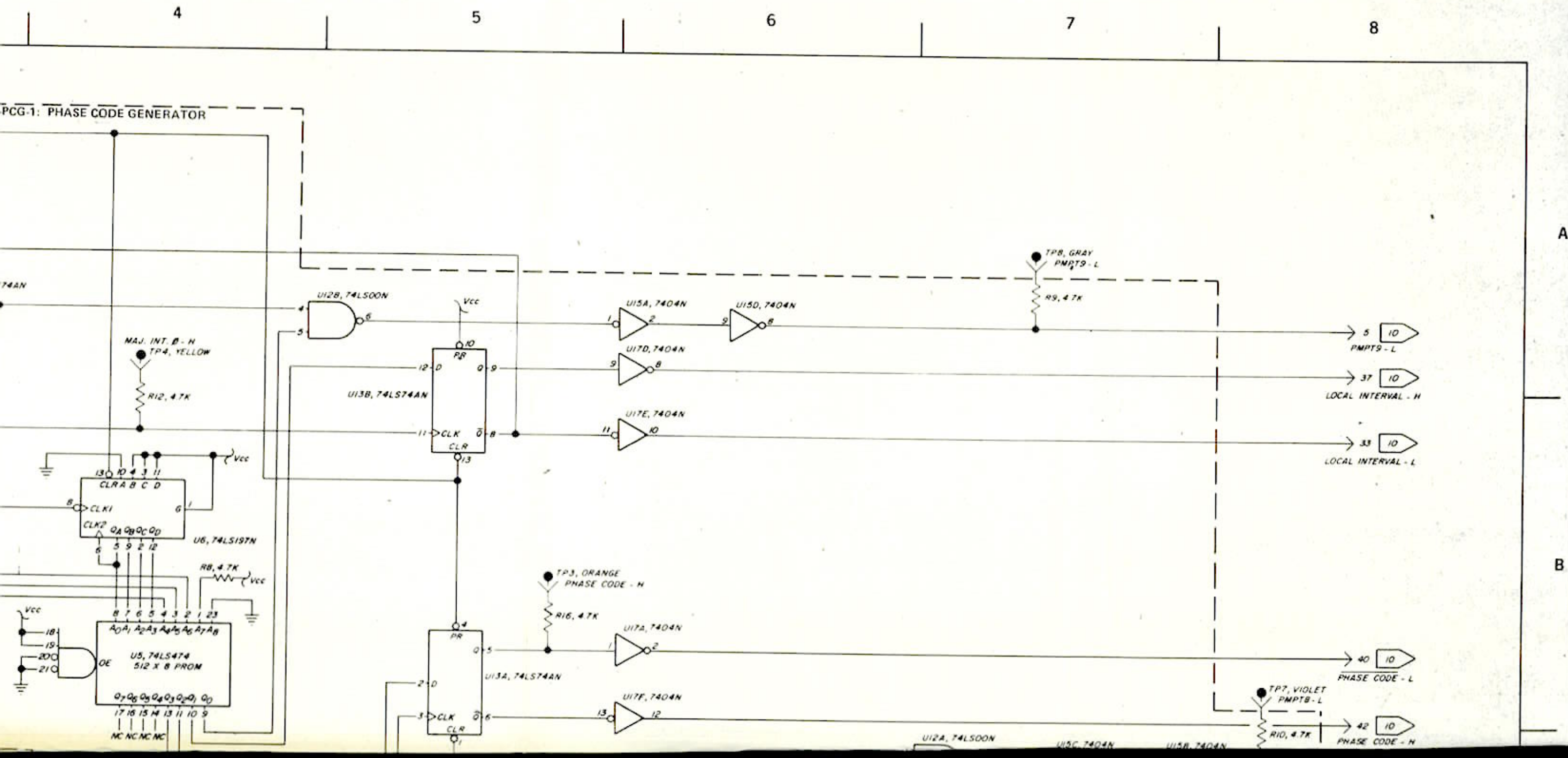
1 = CONNECTED TO COMMON C1 (+5V)

POWER CONNECTIONS (ALL IC's)

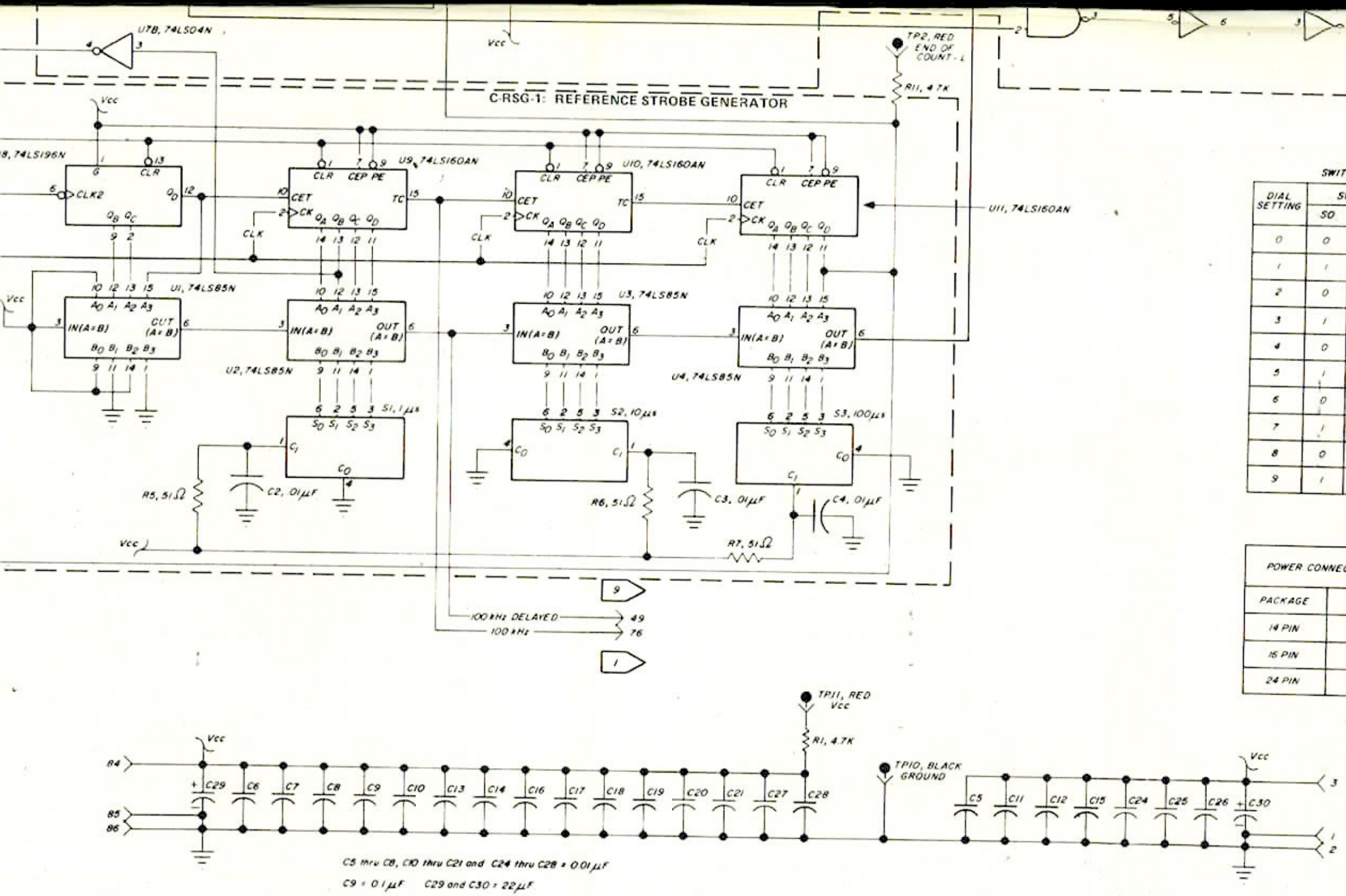
PACKAGE	Vcc	GROUND
14 PIN	14	7
16 PIN	16	8
24 PIN	24	12

Figure 7.31. W0486-30/PC/MPT Schematic Diagram


6
8
A
B
15A, 7404N
U15D, 7404N
17D, 7404N
7E, 7404N
H
A, 7404N
F, 7404N
5
10
PMPT9 - L
37
10
LOCAL INTERVAL - H
33
10
LOCAL INTERVAL - L
40
10
PHASE CODE - L
TP7, VIOLET
PMPT8 - L
R10, 4.7K
42
10
PHASE CODE - H



4
5
6
7
8
A
B
PCG-1: PHASE CODE GENERATOR
74AN
MAJ. INT. Ø - H
TP4, YELLOW
R12, 4.7K
U12B, 74LS00N
Vcc
U13B, 74LS74AN
U15A, 7404N
U15D, 7404N
U17D, 7404N
U17E, 7404N
TP8, GRAY
PMPT9 - L
R9, 4.7K
5
PMPT9 - L
37
LOCAL INTERVAL - H
33
LOCAL INTERVAL - L
CLR A B C D
CLK1
CLK2
U6, 74LS197N
R8, 4.7K
U5, 74LS474
512 X 8 PROM
OE
NC NC NC NC
TP3, ORANGE
PHASE CODE - H
R16, 4.7K
U13A, 74LS74AN
U17A, 7404N
U17F, 7404N
40
PHASE CODE - L
TP7, VIOLET
PMPT8 - L
R10, 4.7K
42
PHASE CODE - H
U12A, 74LS00N
U15C, 7404N
U15B, 7404N



SWITCH S1 THRU S3

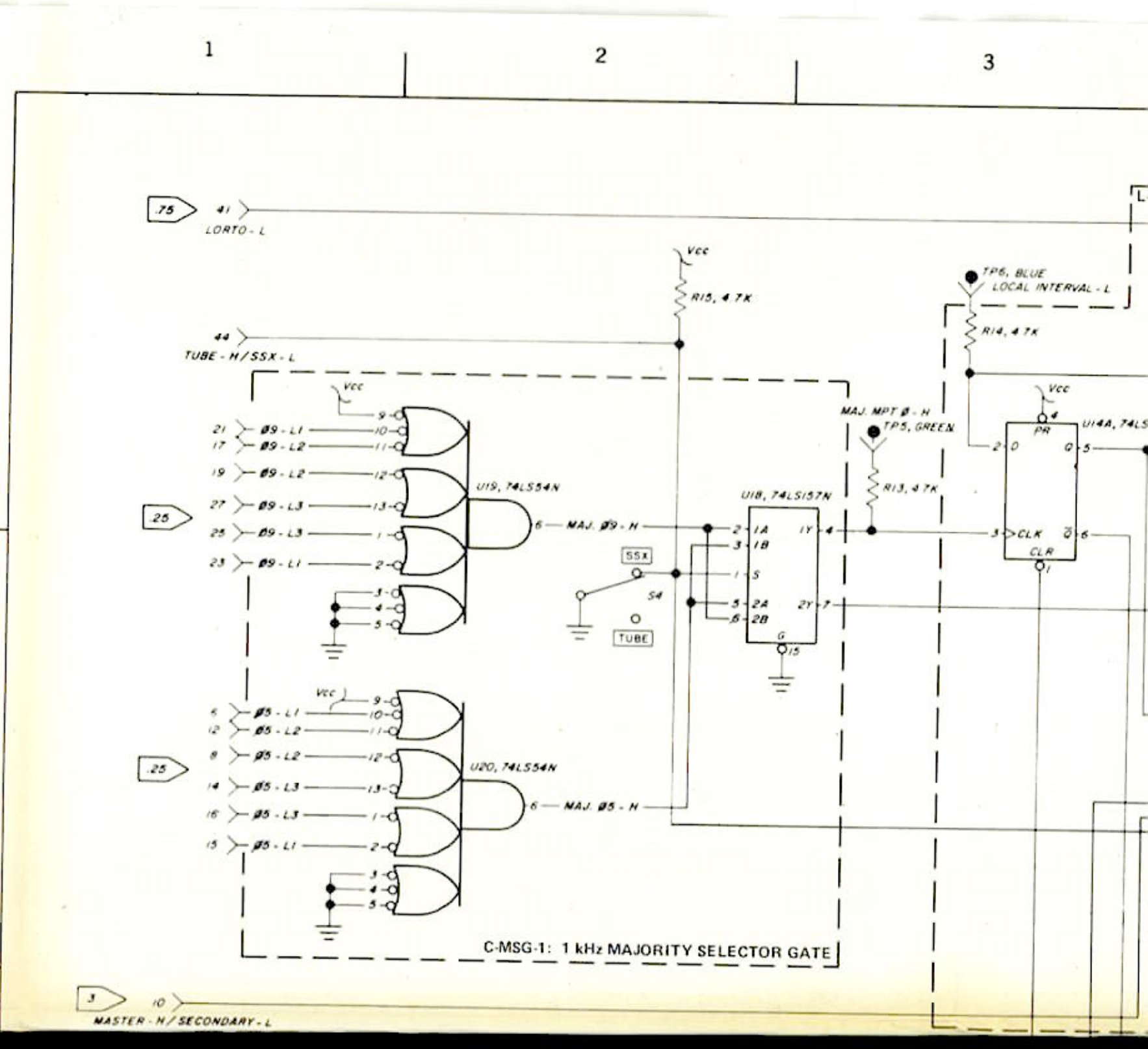
DIAL SETTING	SWITCH OUTPUTS			
	S0	S1	S2	S3
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

0 = CONNECTED TO COMMON C0 (GROUND)

1 = CONNECTED TO COMMON C1 (+5V)

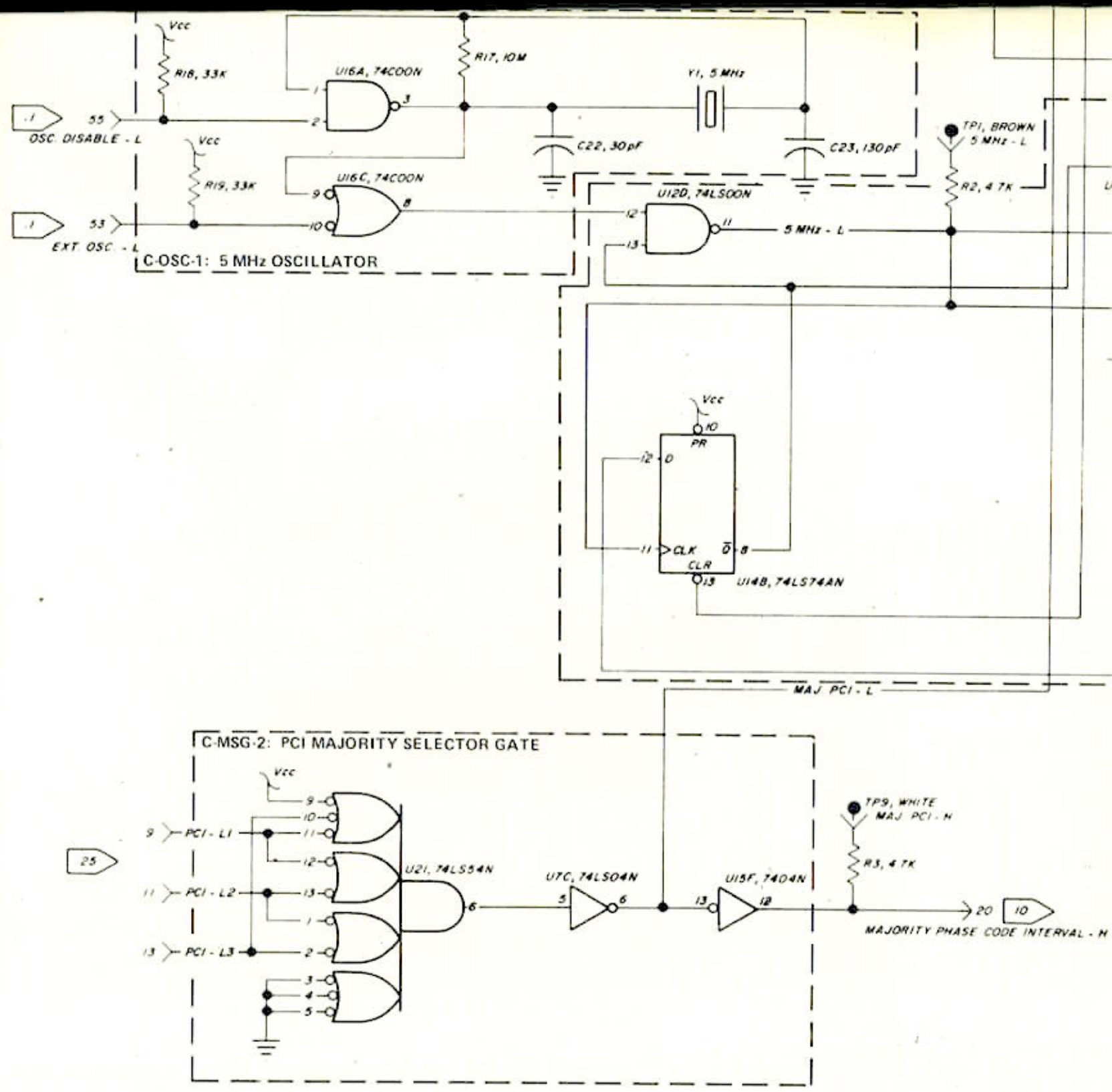
POWER CONNECTIONS (ALL IC's)		
PACKAGE	Vcc	GROUND
14 PIN	14	7
16 PIN	16	8
24 PIN	24	12

Figure 7.31. W0486-30/PC/MPT Schematic Diagram


1
2
3
A
B
.75
41
LORTO - L
Vcc
R15, 4.7K
TP6, BLUE
LOCAL INTERVAL - L
R14, 4.7K
44
TUBE - H/SSX - L
MAJ. MPT Ø - H
TP5, GREEN
R13, 4.7K
U14A, 74LS
U19, 74LS54N
U18, 74LS157N
MAJ. Ø9 - H
SSX
S4
TUBE
.25
U20, 74LS54N
MAJ. Ø5 - H
C-MSG-1: 1 kHz MAJORITY SELECTOR GATE
3
10
MASTER - H/SECONDARY - L

PART LOCATION INDEX

DESIG.	LOCATION	REF. DESIG.	LOCATION	REF. DESIG.	LOCATION
	NOT USED	R6	5D	U7B	4C
	4D	R7	6D	U7C	2E
	6D	R8	4B	U7D	NOT USED
	6D	R9	7A	U7E	NOT USED
	6E	R10	8C	U7F	NOT USED
	4E	R11	6C	U8	4C
	4E	R12	4B	U9	4C
	4E	R13	3A	U10	5C
	5E	R14	3A	U11	6C
0	5E	R15	2A	U12A	7C
1	6E	R16	5B	U12B	5A
2	7E	R17	2C	U12C	NOT USED
3	5E	R18	1C	U12D	2C
4	5E	R19	1C	U13A	5B
5	7E			U13B	5B
6	5E	S1	4D	U14A	3A
7	5E	S2	5D	U14B	2D
8	5E	S3	6D	U15A	6A
9	5E	S4	2B	U15B	7C
0	6E			U15C	7C
1	6E	TP1	3C	U15D	6A
2	2C	TP2	6C	U15E	NOT USED
3	3C	TP3	5B	U15F	3E
4	7E	TP4	4A	U16A	2C
5	7E	TP5	3A	U16B	NOT USED
6	7E	TP6	3A	U16C	2C
7	6E	TP7	8B	U16D	NOT USED
8	6E	TP8	7A	U17A	6B
9	4E	TP9	3D	U17B	NOT USED
0	7E	TP10	7E	U17C	NOT USED
		TP11	7D	U17D	6A
	NOT SHOWN			U17E	6B
	NOT SHOWN	U1	4C	U17F	6B
		U2	4C	U18A	2B
	6E	U3	5C	U18B	NOT USED
	3C	U4	6C	U19	2A
	3E	U5	4B	U20	2B
	NOT USED	U6	4B	U21	2E
	4D	U7A	NOT USED		
				Y1	2C



C D E

1 2 3

REF.
C1
C2
C3
C4
C5
C6
C7
C8
C9
C1
C1
C1
C1
C1
C1
C1
C1
C1
C2
C2
C2
C2
C2
C2
C2
C2
C2
C2
C3
E1
E2
R1
R2
R3
R4
R5

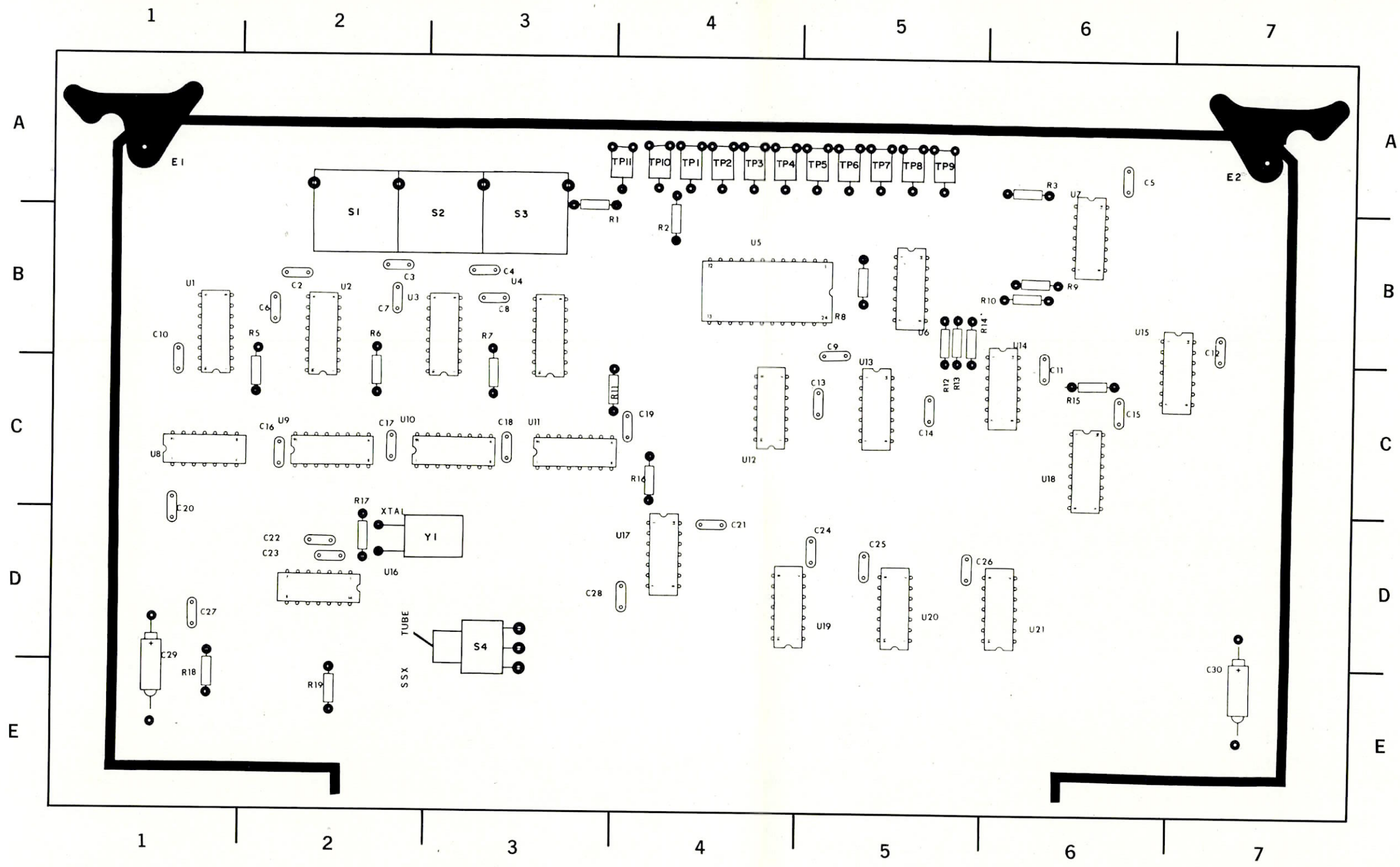


Figure 7.32. W0486-30/PC/MPT Parts Locator

PART LOCATION INDEX			
REF. DESIG.	LOCATION	REF. DESIG.	LOCATION
C1	NOT USED	R13	5B
C2	2B	R14	5B
C3	2B	R15	6C
C4	3B	R16	4C
C5	6A	R17	2D
C6	2B	R18	1E
C7	2B	R19	2E
C8	3B		
C9	5B	S1	2B
C10	1C	S2	3B
C11	6C	S3	3B
C12	7B	S4	3D
C13	5C		
C14	5C	TP1	4A
C15	6C	TP2	4A
C16	2C	TP3	4A
C17	2C	TP4	4A
C18	3C	TP5	5A
C19	4C	TP6	5A
C20	1C	TP7	5A
C21	4D	TP8	5A
C22	2D	TP9	5A
C23	2D	TP10	4A
C24	5D	TP11	4A
C25	5D		
C26	6D	U1	1B
C27	1D	U2	2B
C28	4D	U3	3B
C29	1E	U4	3B
C30	7E	U5	4B
		U6	5B
E1	1A	U7	6B
E2	7A	U8	1C
		U9	2C
R1	3A	U10	3C
R2	4B	U11	3C
R3	6A	U12	4C
R4	NOT USED	U13	5C
R5	2C	U14	6C
R6	2C	U15	7C
R7	3C	U16	2D
R8	5B	U17	4D
R9	6B	U18	6C
R10	6B	U19	4D
R11	4C	U20	5D
R12	5B	U21	6D
		Y1	3D

18, TRANS TRIGGER

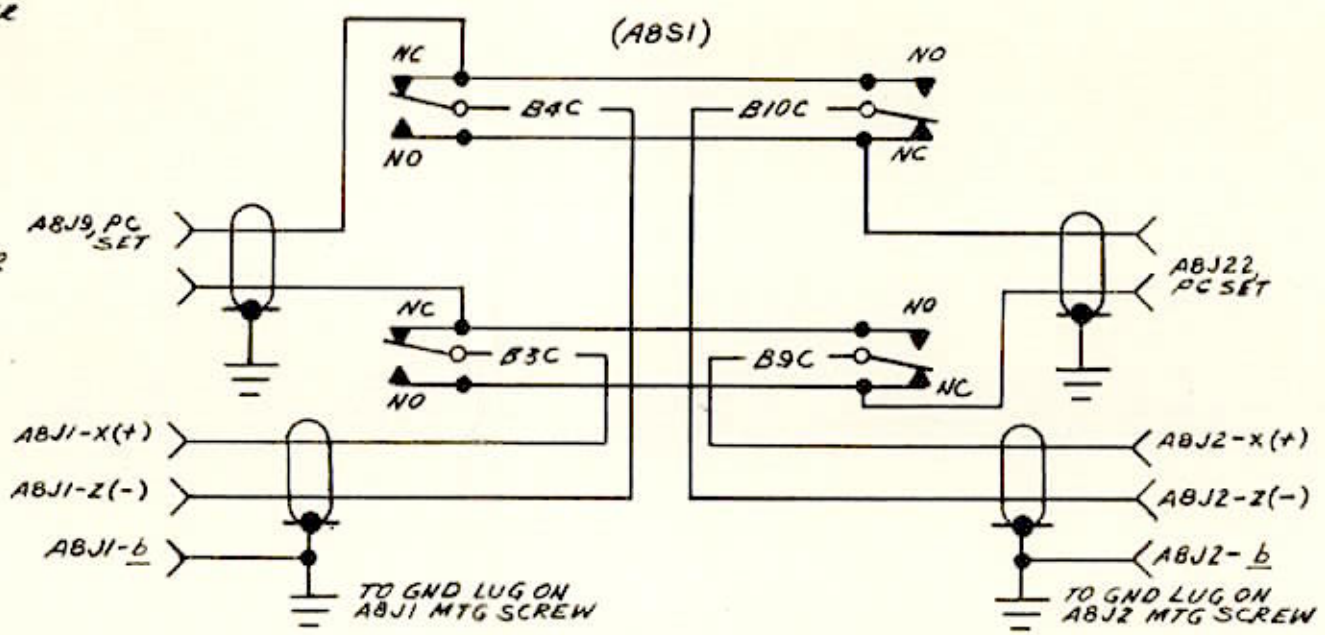
121, TRANS TRIGGER

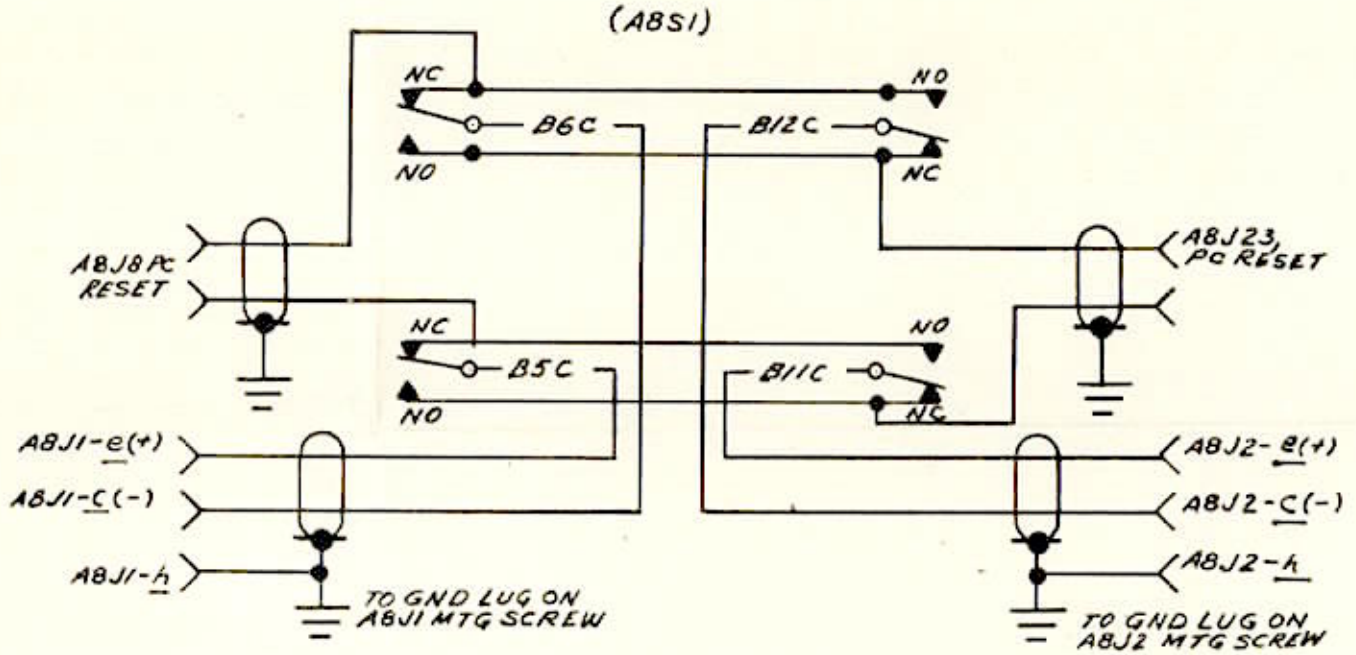
2-S(+)

-P(-)

-U

UG ON
SCREW





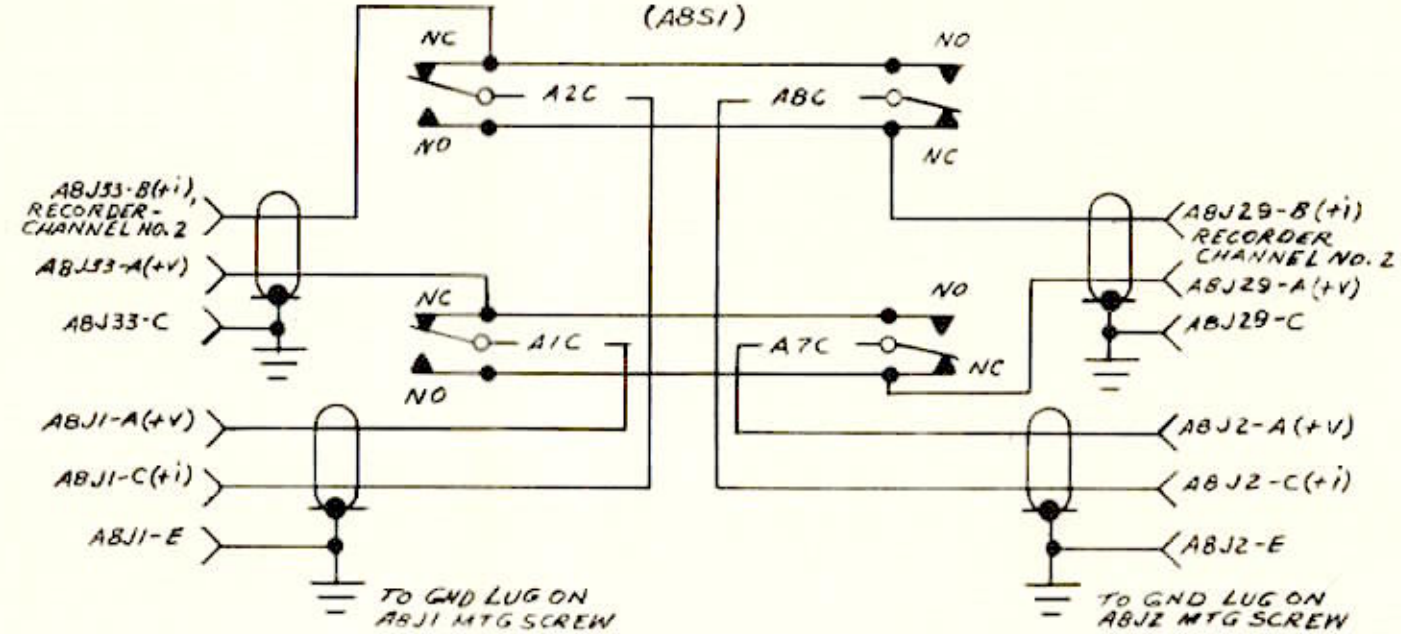
ABJ28
STANDBY
1 MHZ

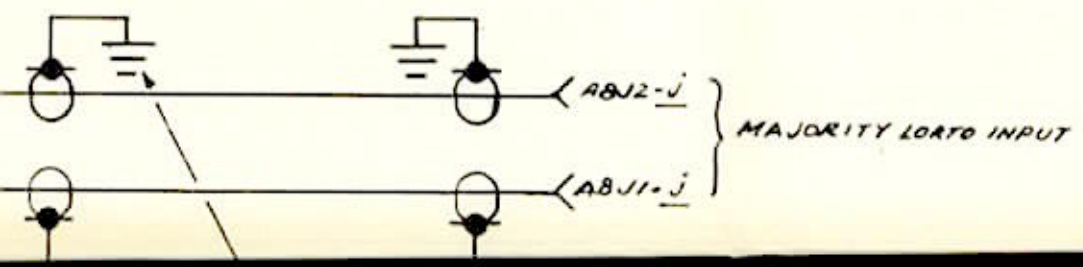
ABJ2-DD 1 MHZ

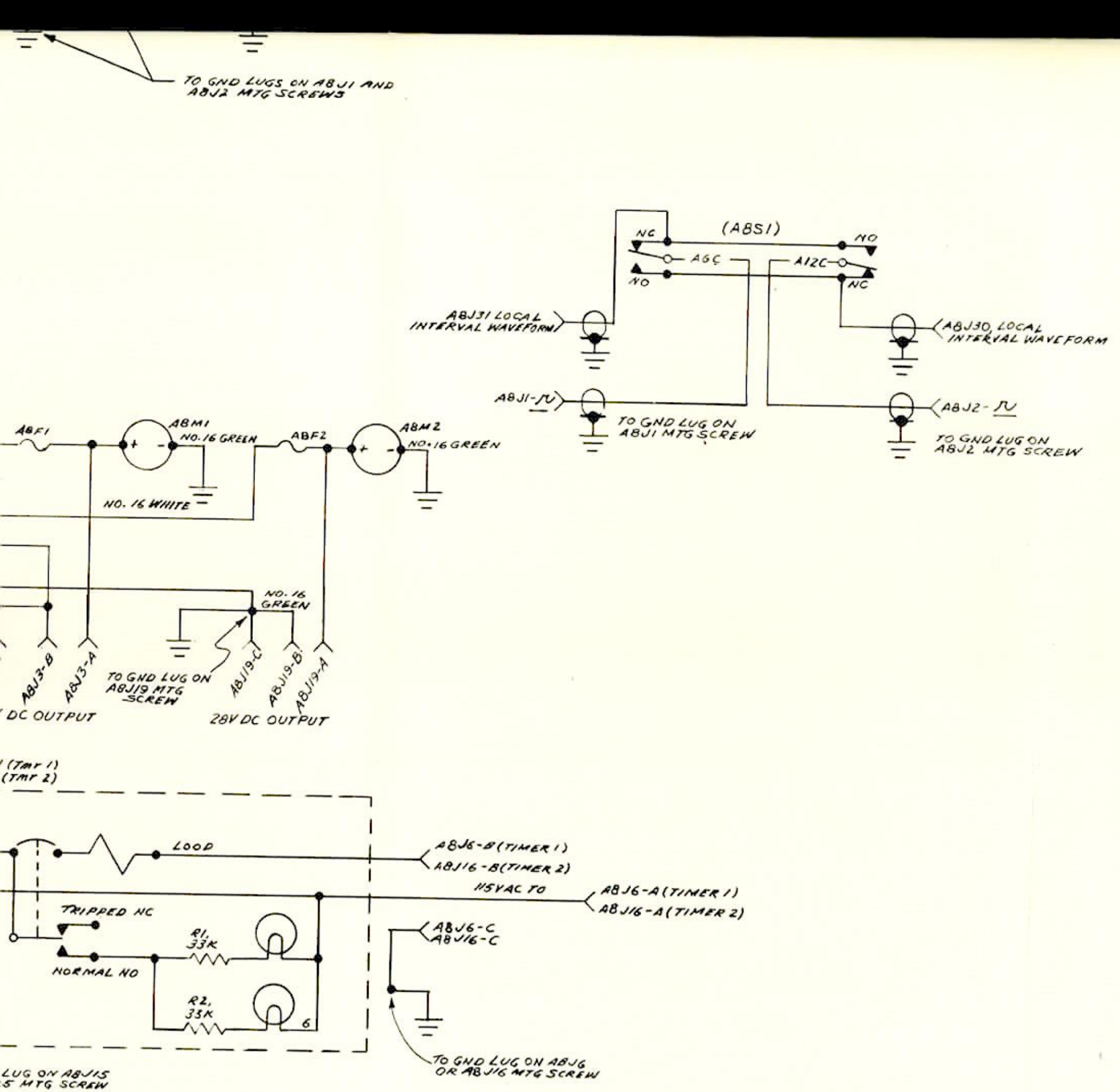
ABJ2-BB

ABJ2-EE

GND LUG ON
J2 MTG SCREW







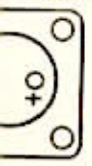
re 7 33. Loran-C Timer Set Control Schematic Diagram

OM SWITCH ABS
ALL BE MADE WITH
IMINIZED MYLA
ISTED PAIR WIT

WIRE USED FOR RUNS
L BE TYPE E TEFLON

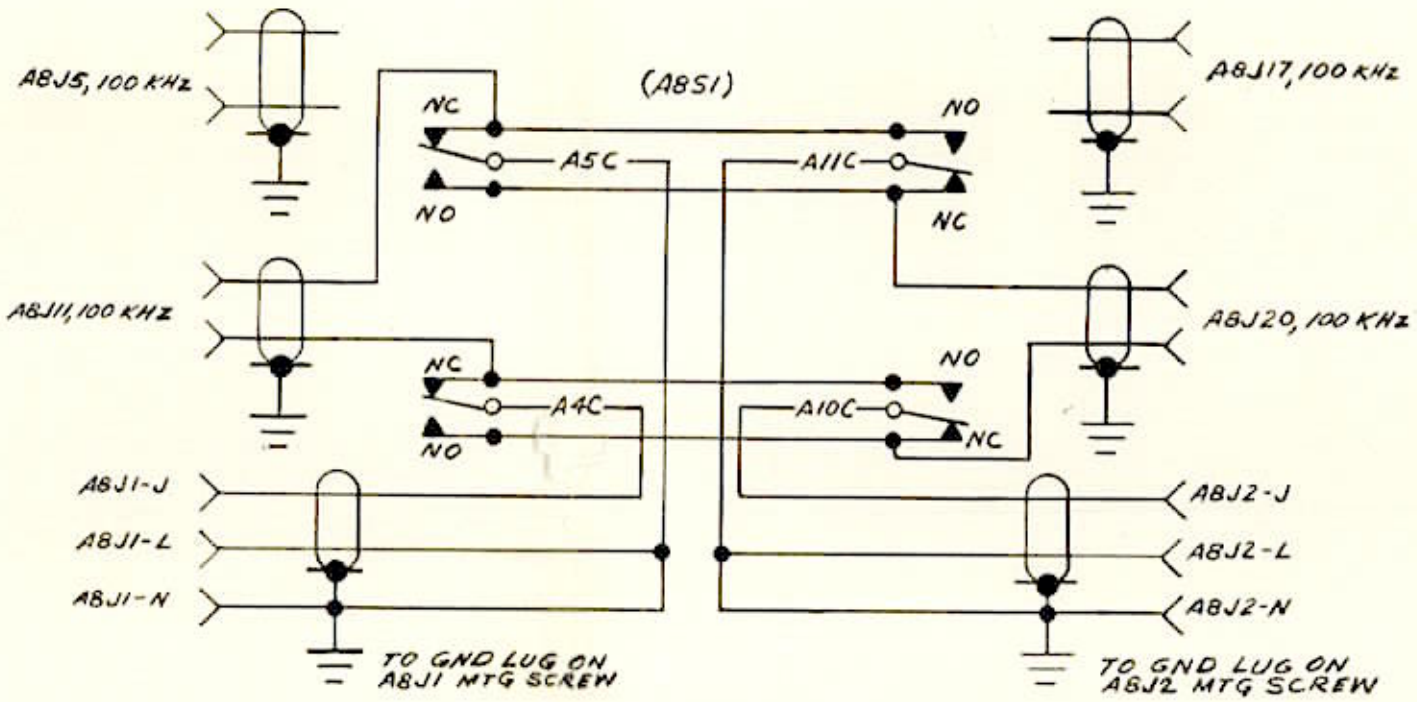
METERS ABMI AN
CTED TO NEARES
ONNECTIONS.

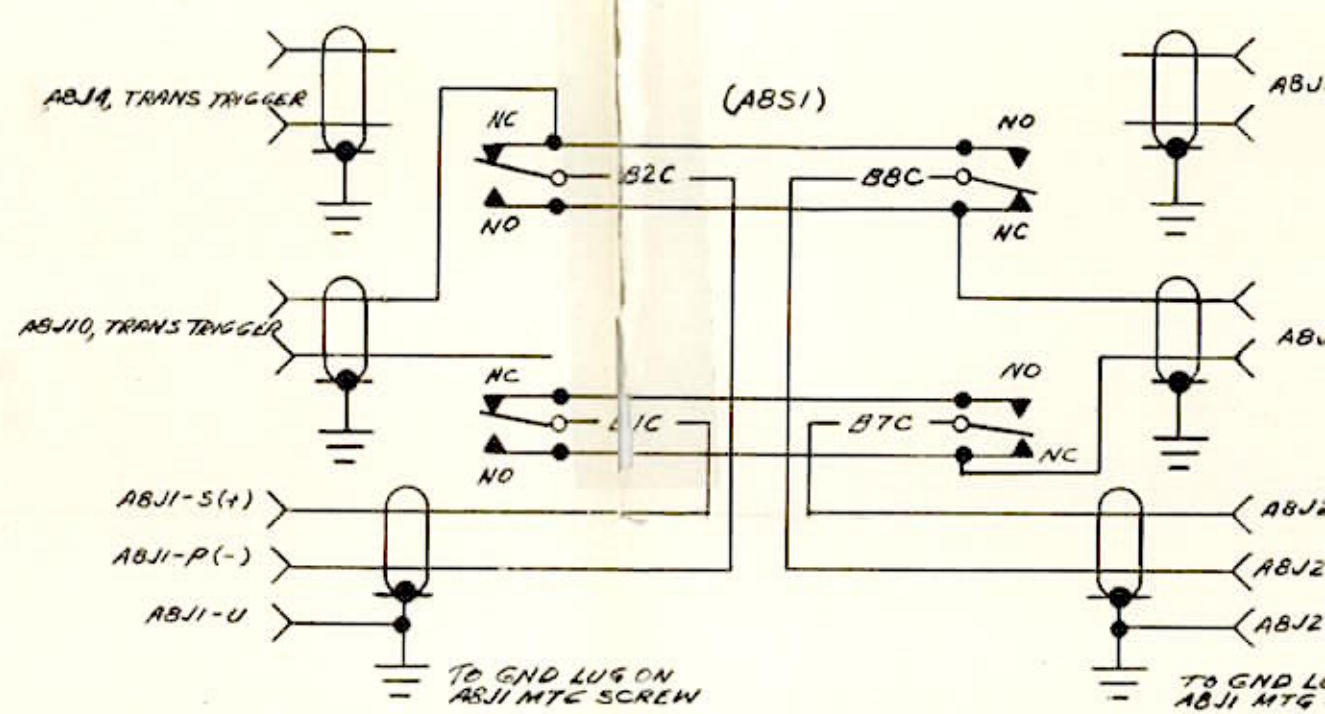
RS (VIEW FROM RE AR
FOLLOWS:

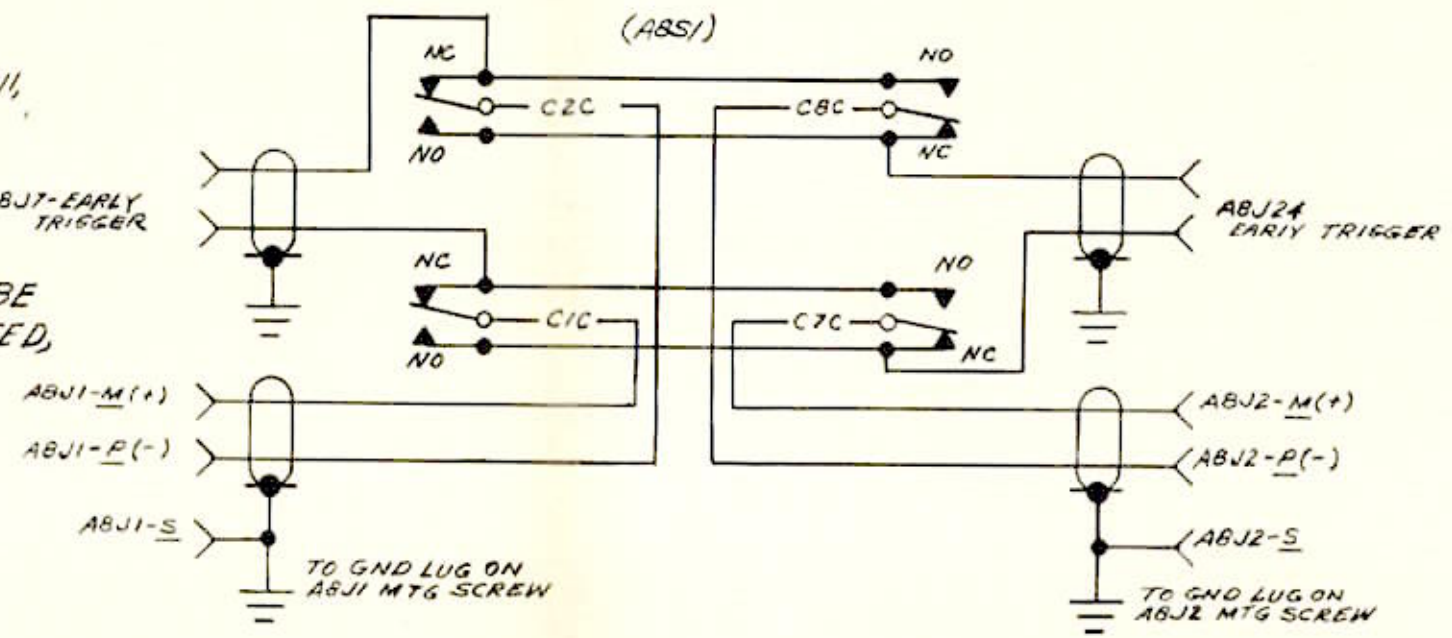


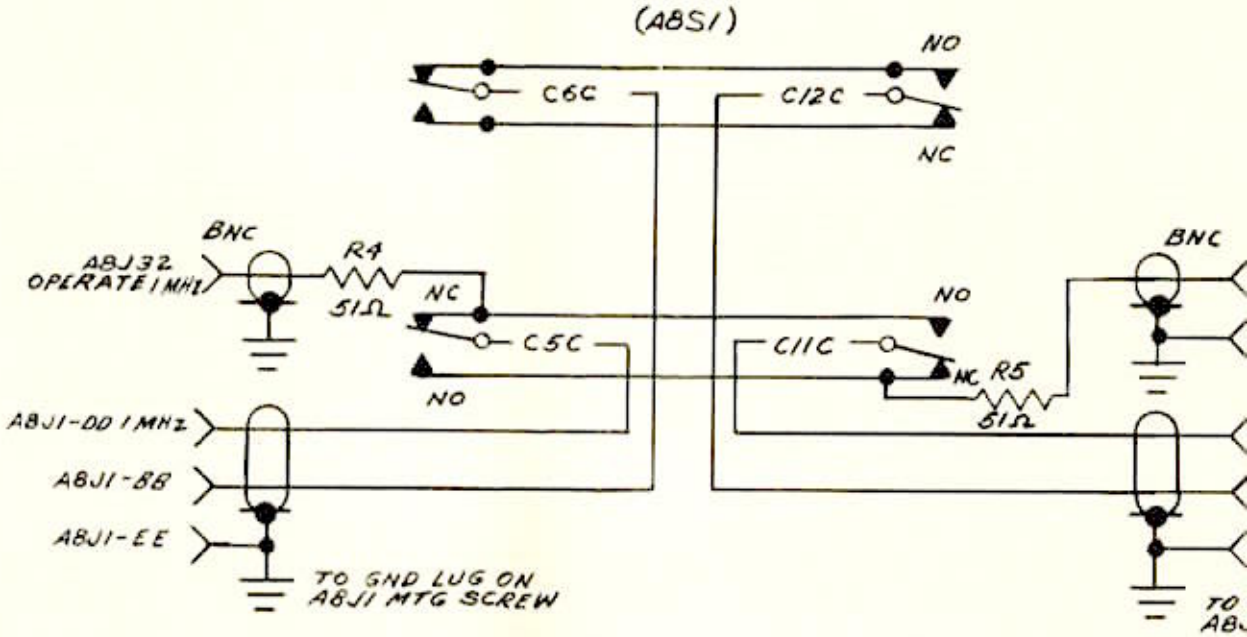
NS BETWEEN ABJ -ABJ11,
BJ10, AND ABJ18 -ABJ21
THE WIRING SID OF
S.

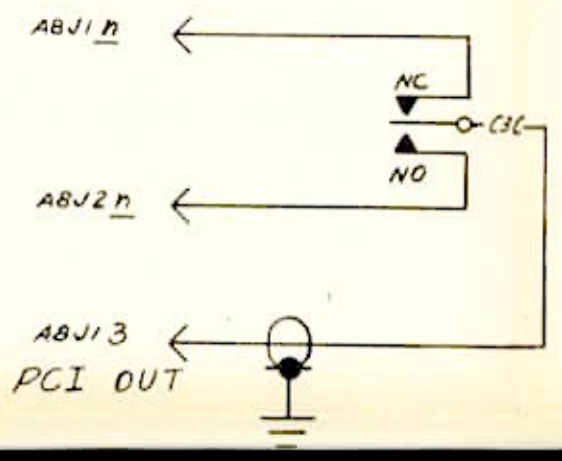
CONNECTIONS SHALL BE
8B/U TEFLON INSULATED,
E COAXIAL CABLE.

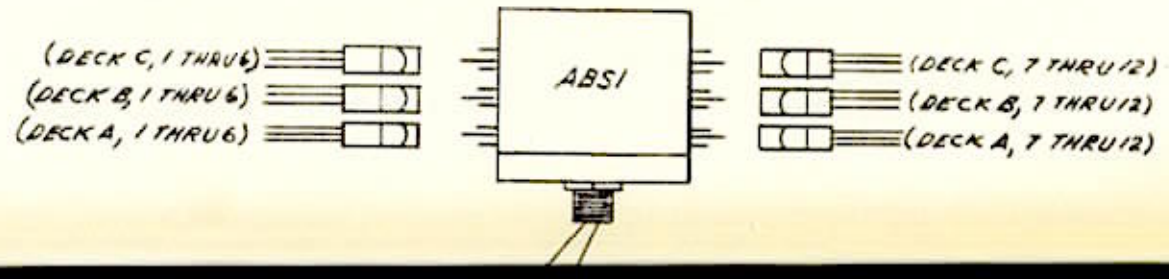






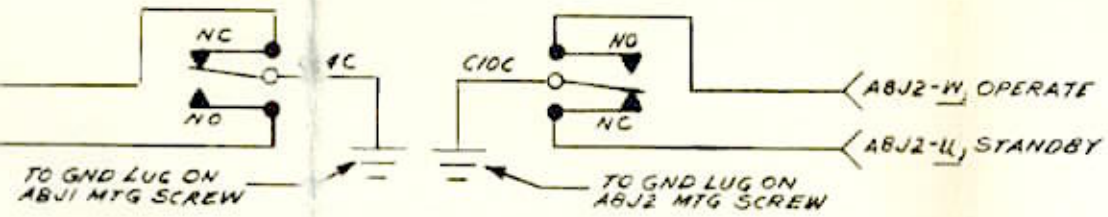


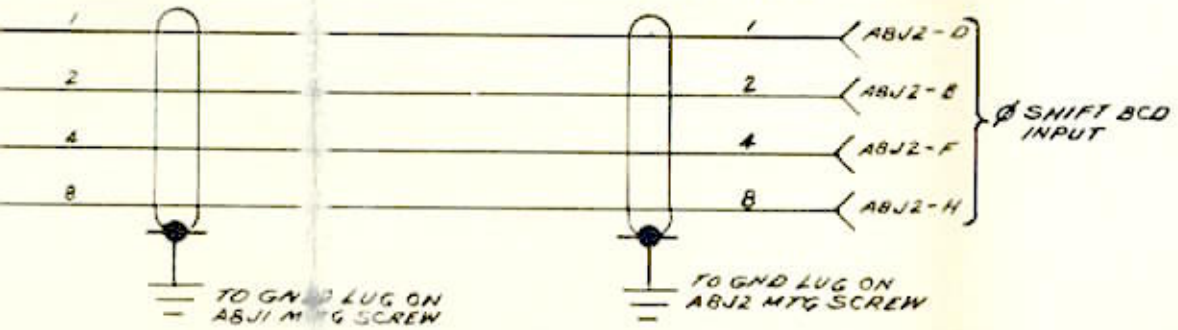


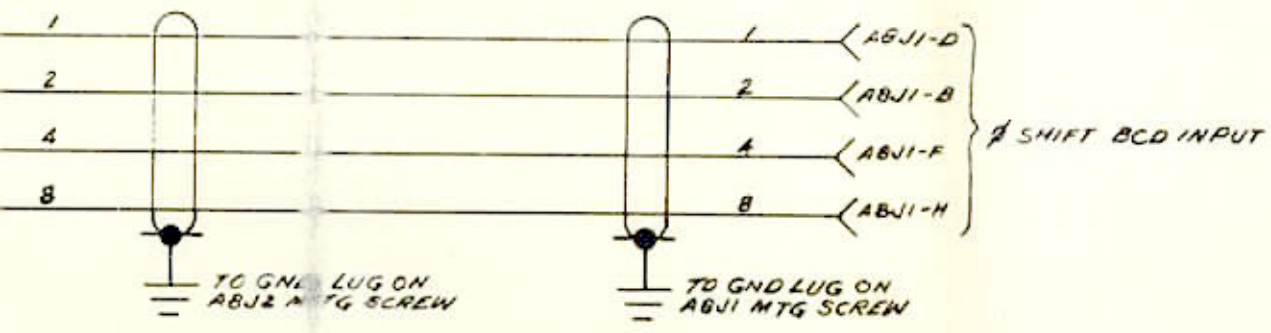


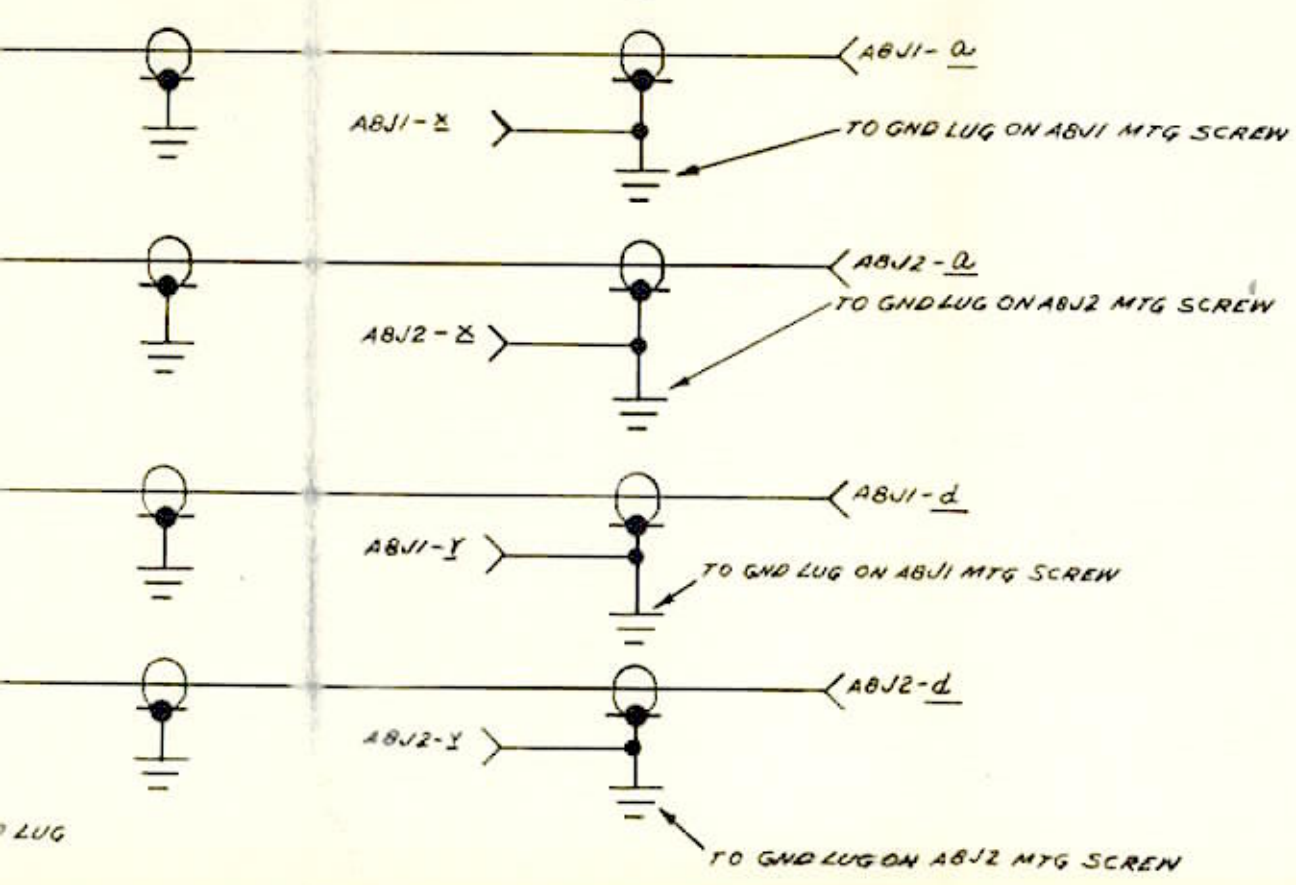


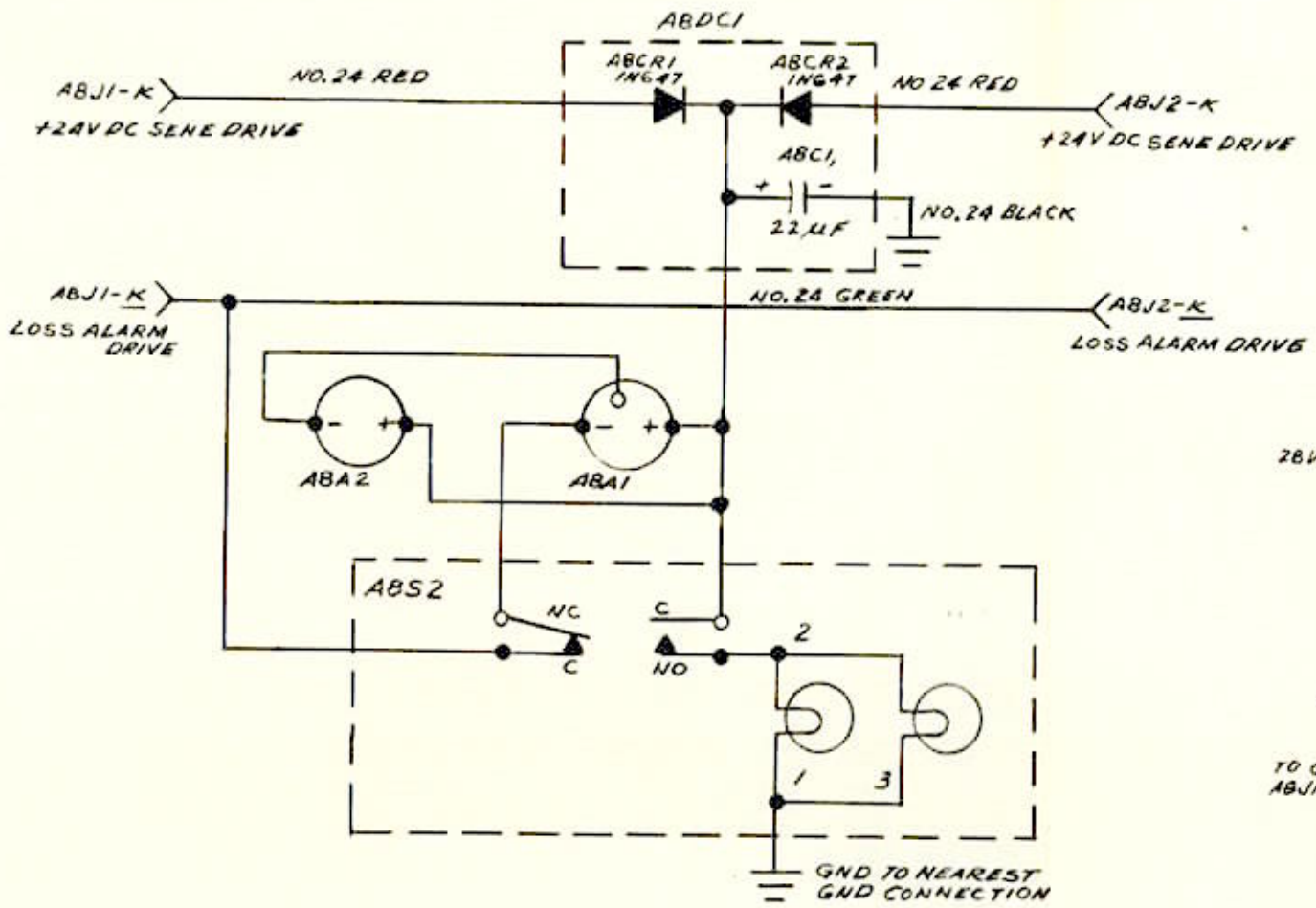
(ABS1)

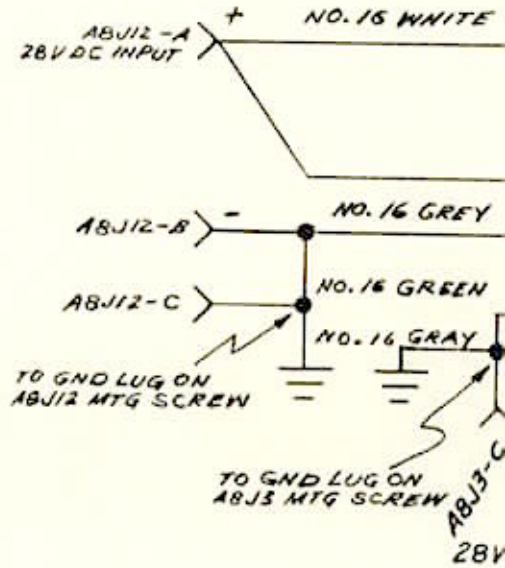

NC
NO
C
C10C
NO
NC
ABJ2-W OPERATE
ABJ2-U STANDBY
TO GND LUG ON ABJ1 MTG SCREW
TO GND LUG ON ABJ2 MTG SCREW

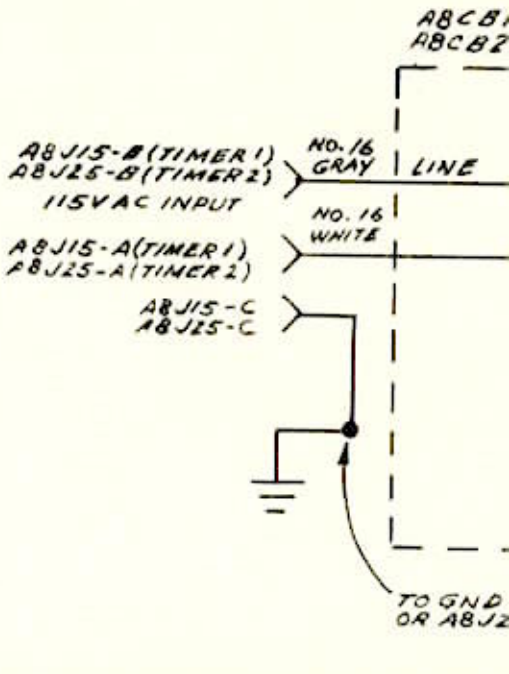

1
2
4
8
ABJ2-D
ABJ2-B
ABJ2-F
ABJ2-H
Ø SHIFT BCD INPUT
TO GND LUG ON ABJ1 MTG SCREW
TO GND LUG ON ABJ2 MTG SCREW


1
2
4
8
ABJ1-D
ABJ1-B
ABJ1-F
ABJ1-H
Ø SHIFT BCD INPUT
TO GND LUG ON ABJ2 MTG SCREW
TO GND LUG ON ABJ1 MTG SCREW


ABJ1-a
ABJ1-X
TO GND LUG ON ABJ1 MTG SCREW
ABJ2-a
ABJ2-X
TO GND LUG ON ABJ2 MTG SCREW
ABJ1-d
ABJ1-Y
TO GND LUG ON ABJ1 MTG SCREW
ABJ2-d
ABJ2-Y
TO GND LUG ON ABJ2 MTG SCREW


ABDC1
ABCR1 1N647
ABCR2 1N647
ABJ1-K
+24V DC SENE DRIVE
NO. 24 RED
NO 24 RED
ABJ2-K
+24V DC SENE DRIVE
ABC1,
22 µF
NO. 24 BLACK
ABJ1-K
LOSS ALARM DRIVE
NO. 24 GREEN
ABJ2-K
LOSS ALARM DRIVE
ABA2
ABA1
ABS2
NC
C
NO
2
1
3
GND TO NEAREST GND CONNECTION


ABJ12-A
28V DC INPUT
+
NO. 16 WHITE
ABJ12-B
-
NO. 16 GREY
ABJ12-C
NO. 16 GREEN
NO. 16 GRAY
TO GND LUG ON ABJ12 MTG SCREW
TO GND LUG ON ABJ3 MTG SCREW
ABJ3-C
28V


ABCB1
ABCB2
ABJ15-B(TIMER 1)
ABJ25-B(TIMER 2)
115VAC INPUT
NO. 16 GRAY
LINE
NO. 16 WHITE
ABJ15-A(TIMER 1)
ABJ25-A(TIMER 2)
ABJ15-C
ABJ25-C
TO GND
OR ABJ2

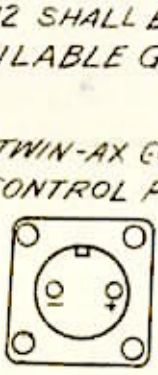
NOTES:

1. ALL CONNECTIONS FRO
TO BACK PANEL SH
TYPE E TEFLON, ALU
SHIELDED, NO. 24 TW
NO. 24 DRAIN WIRE.

2. ALL NO. 24 AND NO. 16
AND JUMPERS SHAL
INSULATED.

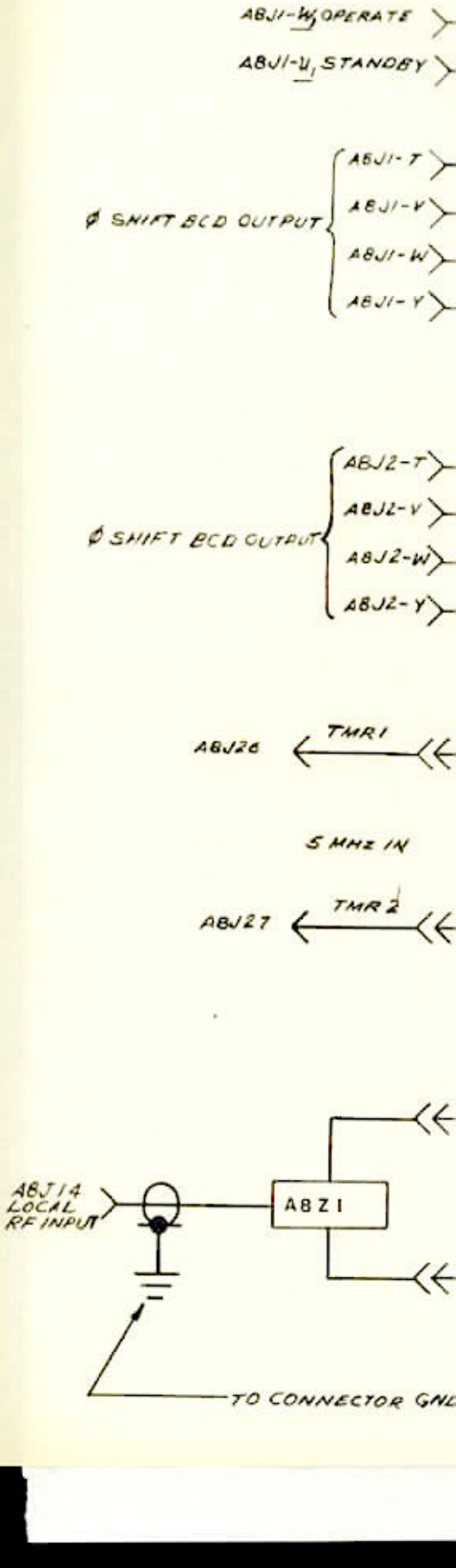
3. NEGATIVE TERMINALS ON
A8M2 SHALL BE CONNEC
AVAILABLE GROUND C

4. WIRE TWIN-AX CONNECTO
OF CONTROL PANEL) AS



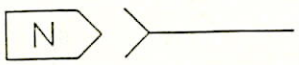
5. PARALLEL CONNECTIO
A8J17-A8J20, A8J4-A8
SHALL BE MADE ON T
THESE CONNECTORS

6. 5 MHz AND LOCAL RF
MADE USING RG-17
50 OHM, MINIATURE


ABJ1-W1 OPERATE
ABJ1-V1 STANDBY
Ø SHIFT BCD OUTPUT
ABJ1-T
ABJ1-V
ABJ1-W
ABJ1-Y
Ø SHIFT BCD OUTPUT
ABJ2-T
ABJ2-V
ABJ2-W
ABJ2-Y
ABJ26
TMR1
5 MHz IN
ABJ27
TMR2
ABJ14
LOCAL
RF INPUT
AB Z1
TO CONNECTOR GND

NOTE: SOURCE/SINK DEFINED AS FOLLOWS:

1 UNIT = 1.6 mA



= N · 1.6 mA SOURCE (CURRENT FLOWS OUT OF TERMINAL)



= N · 1.6 mA SINK (CURRENT FLOWS INTO TERMINAL)

Figure 7.34. Special Symbols